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**EM78P569A**

**8-Bit OTP  
Microcontroller**

**Product  
Specification**

**DOC. VERSION 5.0**

**ELAN MICROELECTRONICS CORP.**

September 2009

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## APPENDIX

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### Specification Revision History

Doc. Version	Revision Description	Date
3.7	Modified the Multiplier function	
3.8	1. Moved the DARES bit from Bit 7 to Bit 3. 2. Changed the instruction "MUL" → "INT A".	
3.9	1. Updated the Application Note. 2. Added 17.91MHz main CLK.	
4.0	1. Added data RAM address auto-increase function. 2. Added mclk/2 signal output (output shared with PC0). 3. Added carry bit calculation function (ADD, SUB).	
4.1	Modified the relation between VERSEL (code option) and PLUS (RA Page 2).	
4.2	Modified the code option definition.	
4.3	Added the OSC stable and reset timing diagram.	
4.4	Removed the IDLE mode. Modified the operating temperature.	
4.5	Removed the code option "MER".	
4.6	Modified the application relation between the operation voltage and the main clock.	2008/08/08
4.7	Added important message in the User Application Notes.	2008/11/24
4.8	1. Modified the wake-up and wake-up source list, Ports 80~83 location 2. Modified IOC6, Page 1 descriptoin. 3. Removed the mistake on IOCE, Page 1, Bits 0~3.	2009/02/26
4.9	"EM78P569" Renamed to "EM78P569A".	2009/06/05
5.0	<a href="#">Modify operation voltage for each MCU clock in Section 1, Feature</a>	2009/09/07



## 1 General Description

The EM78P569A is an 8-bit RISC type microprocessor designed and developed with low-power and high-speed CMOS technology. It has an on-chip 16K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides protection bits to prevent external access or intrusion of your OTP memory code. One-time programmable Code option bits are also available to meet your requirements.

This integrated single IC has an on-chip Watchdog Timer (WDT), program OTP-ROM, data RAM, LCD driver, programmable real time clock/counter, internal interrupt, power down mode, built-in 3-wire SPI, dual PWM (Pulse Width Modulation), 6-channel 10-bit A/D converter, 10-bit D/A converter, and tri-state I/O.

## 2 Features

- CPU configuration
  - 16K×13 bits on-chip OTP ROM
  - 1K×8 bits on-chip data RAM
  - 16 level stacks for subroutine nesting
- I/O port configuration
  - 51 bidirectional tri-state I/O ports
  - Input port interrupt function
- Operating voltage range
  - Operating voltage: 2.4V~5.5V at main CLK of less than 3.58 MHz

Main CLK	Min. Operating Voltage
Under 3.58 MHz	2.4V
7.16 MHz	3.2V
10.74 MHz	3.8V
14.4 MHz	4.2V
17.9 MHz	4.5V
- Operating Frequency
  - 8 levels Normal mode frequency: 447.8kHz, 895.7kHz, 1.79 MHz, 3.58 MHz, 7.16 M, 10.75 MHz, 14.3 MHz ,and 17.9 MHz

Mode	CPU Status	Main Clock	32.768kHz Clock Status
Sleep Mode	Turned off	Turned off	Turned off
Green Mode	Turned on	Turned off	Turned on
Normal Mode	Turned on	Turned on	Turned on
- Peripheral configuration
  - 8-bit real Timer Clock/Counter (TCC)
  - Two 8-bit counters: Counter 1 and Counter 2
  - Dual clock operation: Internal PLL main clock, External 32.768kHz
- 12 Interrupt sources: 4 external, 8 internal
- Multiplier
  - 8×8 multiplier
  - 8×8 accumulated multiplication-addition multiplier with sign and address auto-increment function
- SPI
  - Serial peripheral interface (SPI) available
  - Interrupt flag available for the read buffer full
  - Programmable baud rates of communication
  - 3-wire synchronous communication (pin-shared with I/O)
- PWM
  - Dual Pulse Width Modulation (PWM ) with 10-bit resolution
  - Programmable period (or baud rate)
  - Programmable duty cycle
- ADC
  - Operating voltage: 2.5V~5.5V
  - 6-channel 10-bit successive approximation A/D converter
  - Internal VDD or external reference
- DAC
  - Operating voltage: 2.5V~5.5V under VDD reference  
2.8V~5.5V under 2.5V reference
  - 10-bit R-2R D/A converter
  - Internal VDD or 2.5V reference
- POR: 2.0V Power-on reset
- LCD
  - Common driver pins: 4
  - Segment driver pins: 32
  - 1/3 bias
  - 1/4 duty, 1/2 duty
  - 16-level LCD contrast control by software
- Single Instruction cycle commands
- Special feature
  - On-chip Programmable free running watchdog timer
- Package type
  - 100-pin QFP
  - 73-pin Die

### 3 Application

Communication or general purpose

### 4 Pin Configuration

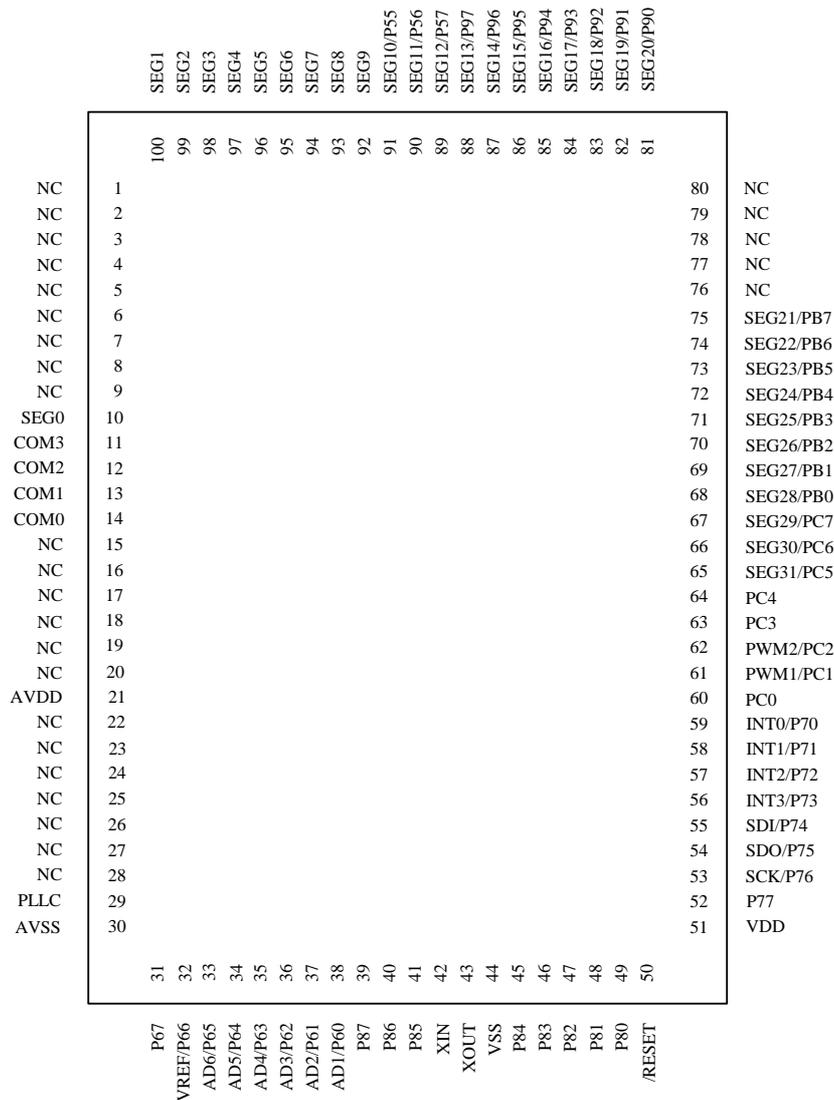


Figure 4-1 73-Pin Die or 100-Pin QFP

OTP Pin Name	Mask ROM Pin Name
VDD	AVDD
VPP	/RESET
DINCK	P65
ACLK	P64
PGMB	P63
OEB	P62
DATA	P73
GND	AVSS

## 5 Functional Block Diagram

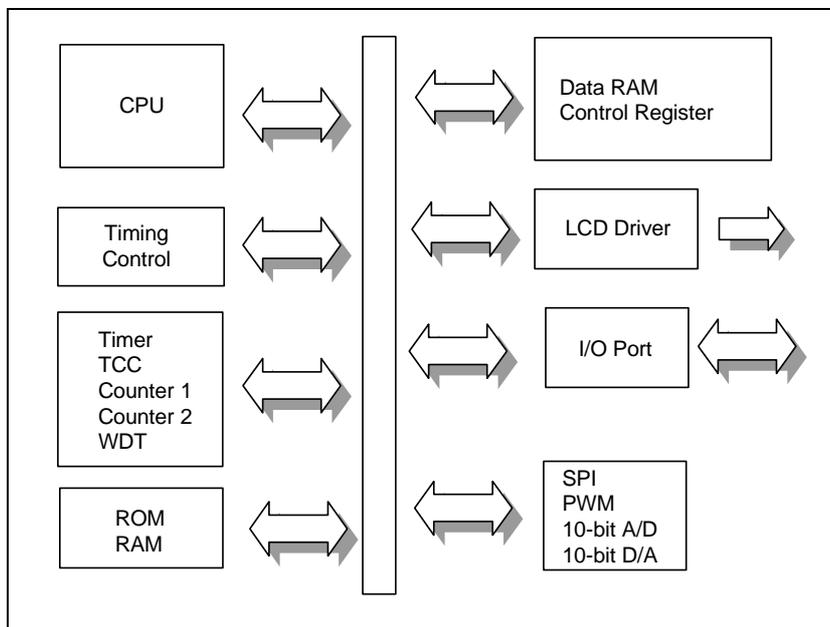


Figure 5-1a Block Diagram 1

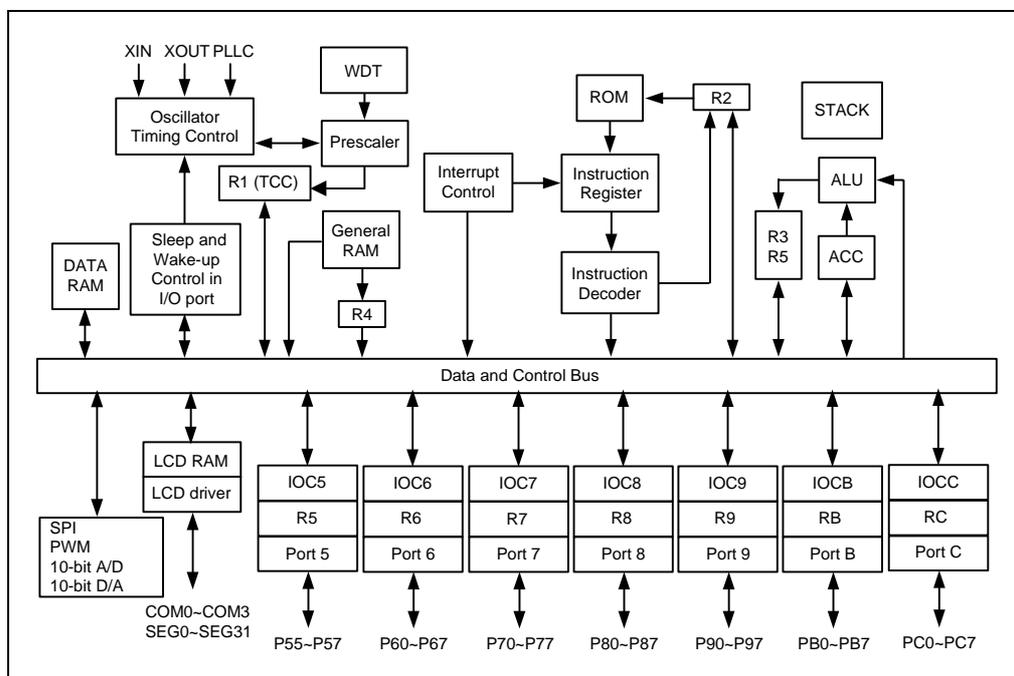


Figure 5-1b Block Diagram 2

## 6 Pin Description

Pin	I/O	Description
<b>Power</b>		
VDD AVDD	Power	Digital power Analog power
VSS AVSS	Power	Digital ground Analog ground
<b>Clock</b>		
XIN	I	Input pin for 32.768kHz oscillator
XOUT	O	Output pin for 32.768kHz oscillator
PLLCC	I	Phase loop lock capacitor. Connect a 0.047μF~ 0.1μF capacitor to the ground.
<b>LCD</b>		
COM0 ~ COM3	O	LCD drivers common driver pins
SEG0 ~ SEG9 SEG10 ~ SEG12 SEG13 ~ SEG20 SEG21 ~ SEG28 SEG29 ~ SEG31	O (I/O: Port 5) O (I/O: Port 9) O (I/O: Port B) O (I/O: Port C)	LCD drivers Segment driver pins SEG10 to SEG31 are shared with I/O Port.
<b>10-bit 6 Channel A/D</b>		
AD1	I (P60)	ADC Input Channel 1. Pin is shared with Port 60
AD2	I (P61)	ADC Input Channel 2. Pin is shared with Port 61
AD3	I (P62)	ADC Input Channel 3. Pin is shared with Port 62
AD4	I (P63)	ADC Input Channel 4. Pin is shared with Port 63
AD5	I (P64)	ADC Input Channel 5. Pin is shared with Port 64
AD6	I (P65)	ADC Input Channel 6. Pin is shared with Port 65
VREF	I (P66)	ADC reference input. Pin is shared with Port 66
<b>10-bit D/A</b>		
DAO	O (P67)	DAO is 10-bit DA output pin is shared with Port 67
<b>SPI</b>		
SCK	I/O (Port 76)	Master: output pin, Slave: input pin. Pin is shared with Port 76.
SDO	O (Port 75)	Output pin for serial data transferring. Pin is shared with Port 75.
SDI	I (Port 74)	Input pin for receiving data. Pin is shared with Port 74.
<b>PWM</b>		
PWM1	O (PC1)	Pulse Width Modulation Output Channel 1
PWM2	O (PC2)	Pulse Width Modulation Output Channel 2

Pin	I/O	Description
<b>I/O</b>		
P55~P57	I/O	Each bit in Port 5 can be Input or Output port. Port 5 (7:5) are shared with LCD Segment signal.
P60 ~P67	I/O	Each bit in Port 6 can be Input or Output port.
P70 ~ P77	I/O	Each bit in Port 7 can be Input or Output port. Port 7 (4~6) are shared with SPI interface pins Internal pull-high function. Interrupt function.
P80 ~ P87	I/O	Each bit in Port 8 can be Input or Output port. Internal pull-high. Port 85 ~ P87 are shared with ADC input pins Port 8 (0~3) has wake-up functions (set by RE PAGE 0)
P90 ~ P97	I/O	Each bit in Port 9 can be Input or Output port. Port 9 are shared with LCD Segment signal.
PB0 ~ PB7	I/O	Each bit in Port B can be Input or Output port. Port B are shared with LCD Segment signal.
PC0 ~ PC7	I/O	Each bit in Port C can be Input or Output port. Port C (0~1) are shared with PWM output pins. Port C (7:5) are shared with LCD Segment signal.
SCLKO	O	MCLK/2's CLK output (25% duty cycle)
INT0	Port 70	Interrupt sources. Once Port 70 encounters a falling edge or rising edge signal (controlled by CONT register), it will generate an interrupt.
INT1	Port 71	Interrupt source which has the same interrupt flag. When any pin from Port 71 encounters a falling edge signal, it will generate an interrupt.
INT2	Port 72	Interrupt source that has the same interrupt flag. When any pin from Port 72 encounters a falling edge signal, it will generate an interrupt.
INT3	Port 73	Interrupt source that has the same interrupt flag. When any pin from Port 73 encounters a falling edge signal, it will generate an interrupt.
/RESET	I	Low reset

## 7 Functional Description

### 7.1 Operational Registers

#### 7.1.1 R Page Registers Configuration

Addr	R Page Registers			
	R Page 0	R Page 1	R Page 2	R Page 3
00	Indirect addressing	–	–	–
01	TCC	–	–	–
02	PC	–	–	–
03	Page, Status	–	–	–
04	RAM bank, RSR	–	–	–
05	Port 5 I/O data, Program ROM page	LCD RAM address	SPI control	PWM control
06	Port 6 I/O data	LCD data buffer	SPI data buffer	Duty of PWM1
07	Port 7 I/O data	Data RAM bank	–	PWM1 control Duty of PWM1
08	Port 8 I/O data	Data RAM address	–	Period of PWM1
09	Port 9 I/O data	Data RAM data buffer	–	Duty of PWM2
0A	PLL, Main clock, WDTE	DAC input data buffer	Multiplier control	PWM2 control Duty of PWM2
0B	Port B I/O data	ADC output data buffer	Multiplicand Y	Period of PWM2
0C	Port C I/O data	Counter 1 data	Mul result MR (0~7)	–
0D	LCD control	Counter 2 data	Mul result MR (8~15)	–
0E	Wake-up control, Interrupt flag	–	Mul result MR (16~23)	–
0F	Interrupt flag	–	–	–
10	16 bytes	–	–	–
:	Common registers	–	–	–
1F		–	–	–
20	Bank 0~Bank 3	–	–	–
:	Common registers	–	–	–
3F	(32×8 for each bank)	–	–	–

### 7.1.2 IOC Page Registers Configuration

Addr	IOC Page Registers	
	IOC Page0	IOC Page1
00	–	–
01	–	–
02	–	–
03	–	–
04	–	–
05	Port 5 I/O control, LCD bias control	–
06	Port 6 I/O control	Port 6 switches
07	Port 7 I/O control	Port 7 pull high
08	Port 8 I/O control	Port 8 pull high
09	Port 9 I/O control	Port 9 switches
0A	–	–
0B	Port B I/O control	ADC control
0C	Port C I/O control	Ports 5, 8, B,C switch
0D	–	Clock source (CN1,CN2) Prescaler (CN1,CN2)
0E	Interrupt mask	–
0F	Interrupt mask	–
10	–	–
:	–	–
1F	–	–
20	–	–
:	–	–
3F	–	–

## 7.2 Operational Registers Detailed Description

### 7.2.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

#### Example:

```
Mov    A, @0x20    ; store an address at R4 for indirect
                    ; addressing
Mov    0x04, A
Mov    A, @0xAA    ; write Data 0xAA to R20 at Bank 0 through R0
Mov    0x00, A
```

### 7.2.2 R1 (TCC)

TCC (Timer Clock/Counter) data buffer. Increased by 16.384kHz or by the instruction cycle clock (controlled by CONT register).

Written and read by the program as any other register.

### 7.2.3 R2 (Program Counter)

The structure is depicted in Figure 7-1 and it generates  $16k \times 13$  on-chip Program OTP-ROM addresses to the relative programming instruction codes.

"JMP" instruction allows direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC & PC+1, and then pushes them into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with its contents at the top of stack.

"MOV R2, A" allows loading of an address from A register to PC, and the contents of the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address to be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address to be added to the current PC, and the contents of the ninth and tenth bits don't change. The most significant bit (A10~A13) will be loaded with the contents of Bits PS0~PS3 in the status register (R5 PAGE0) upon the execution of a "JMP", "CALL", "ADD R2, A", or "MOV R2, A" instruction.

If an interrupt is triggered, the program ROM will jump to Address 0x08 at Page 0. The CPU will store the ACC, R3 status, and R5 PAGE automatically, and they will be restored after RETI instruction.

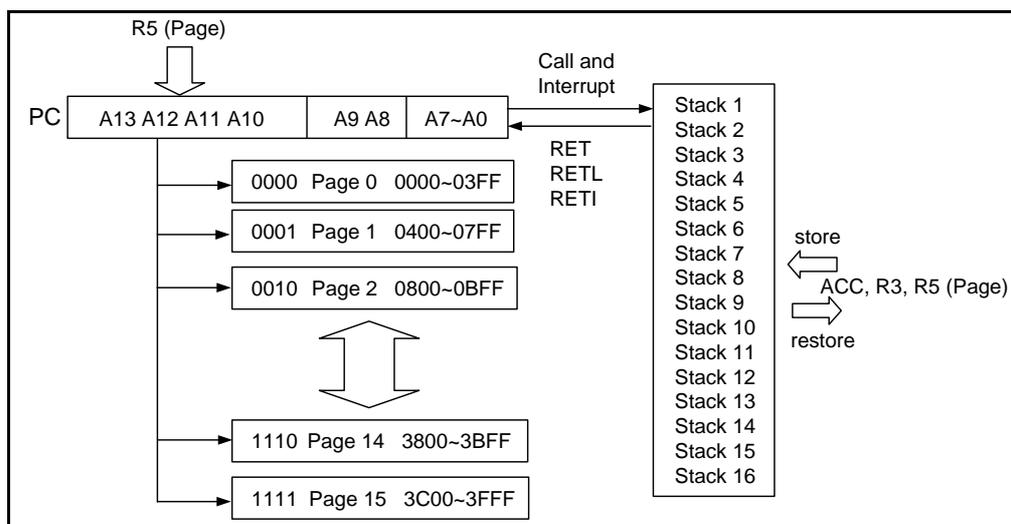


Figure 7-1 Program Counter Organization

### 7.2.4 R3 (Status, Page Selection)

#### ■ Status Flag, Page Select Bits

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>RPAGE1</b>	<b>RPAGE0</b>	<b>IOCPAGE</b>	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R	R	R/W	R/W	R/W

**Bit 0 (C):** Carry flag

**Bit 1 (DC):** Auxiliary carry flag

**Bit 2 (Z):** Zero flag

**Bit 3 (P):** Power down bit

Set to "1" during power-on or by a "WDTC" command and reset to "0" by a "SLEP" command.

**Bit 4 (T):** Time-out bit

Set to "1" by the "SLEP" and "WDTC" commands or during power up, and reset to "0" by WDT timeout.

Event	T	P	Remarks
WDT wake-up from Sleep mode	0	0	–
WDT time out (not Sleep mode)	0	1	–
/RESET wake-up from Sleep mode	1	0	–
Power up	1	1	–
Low pulse on /RESET	x	x	–

x: don't care

**Bit 5 (IOCPAGE):** Change IOC5 ~ IOCE to another page

**0:** IOC Page 0

**1:** IOC Page 1

Refer to Section 7.1.2 for the detailed IOC PAGE register configuration.

**Bit 6 ~ Bit 7 (RPAGE0 ~ RPAGE1):** Change R5 ~ RE to another page

Refer to Section 7.1.2 for detailed IOC PAGE register configuration.

	R Page # Selected
(0, 0)	R Page 0
(0, 1)	R Page 1
(1, 0)	R Page 2
(1, 1)	R Page 3

### 7.2.5 R4 (RAM Selection for Common Registers R20 ~ R3F)

#### ■ RAM Selection Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

**Bit 0 ~ Bit 5 (RSR0 ~ RSR5):** Indirect addressing for common Registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

**Bit 6 ~ Bit 7 (RB0 ~ RB1):** Bank select bits for common registers R20 ~ R3F

These select bits are used to determine which bank is activated among the four banks of the 32 registers (R20 to R3F).

See Section 7.1.2 for the detailed IOC PAGE register configuration.

### 7.2.6 R5 (Port 5 I/O Data, Program Page Select, LCD Address, SPI Control, PWM Control)

#### ■ Page 0 (Port 5 I/O Data Register, Program Page Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	-	PS3	PS2	PS1	PS0
R/W	R/W	R/W		R/W-0	R/W-0	R/W-0	R/W-0

**Bit 0 ~ Bit 3 (PS0 ~ PS3):** Program page select bits

PS3	PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3
:	:	:	:	:
:	:	:	:	:
1	1	1	0	Page 14
1	1	1	1	Page 15

Use the Page instruction to change page in order to maintain your program page.

**Bit 4:** Undefined. Do not use

**Bit 5 ~ Bit 7 (P55 ~ P57):** 8-bit Port 5 (5~7) I/O data register

Use the IOC register to define each bit as input or output.

■ **Page 1 (LCD Address)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA9	DA8	-	-	LCDA3	LCDA2	LCDA1	LCDA0
R/W	R/W			R/W-0	R/W-0	R/W-0	R/W-0

**Bit 0 ~ Bit 3 (LCDA0 ~ LCDA3):** LCD address for LCD RAM read or write

The address of the LCD RAM corresponds to the Common and Segment signals as shown in the table.

COM3 ~ COM0	LCD Address (LCDA3 ~ LCDA0)
SEG1, SEG0	00H
SEG3, SEG2	01H
SEG5, SEG4	02H
SEG7, SEG6	03H
SEG9, SEG8	04H
SEG11, SEG10	05H
SEG13, SEG12	06H
SEG15, SEG14	07H
SEG17, SEG16	08H
SEG19, SEG18	09H
SEG21, SEG20	0AH
SEG23, SEG22	0BH
SEG25, SEG24	0CH
SEG27, SEG26	0DH
SEG29, SEG28	0EH
SEG31, SEG30	0FH

**Bit 4 ~ Bit 5:** Not used

**Bit 6 ~ Bit 7 (DA8~DA9):** DA8 and DA9 are DAC MSB when R7 Page 1 Bit 3 (DARES) is set or unused when DAREF is cleared to 0. When using 10 bits resolution DAC, DAO output voltage will be unchanged after writing data to these two bits. The DAO pin will change after writing new data to DAC low 8 bits data buffer (RA Page 1).

■ Page 2 (SPI Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBF	SPIE	SRO	SE	SCES	SBR2	SBR1	SBR0
R/W-0							

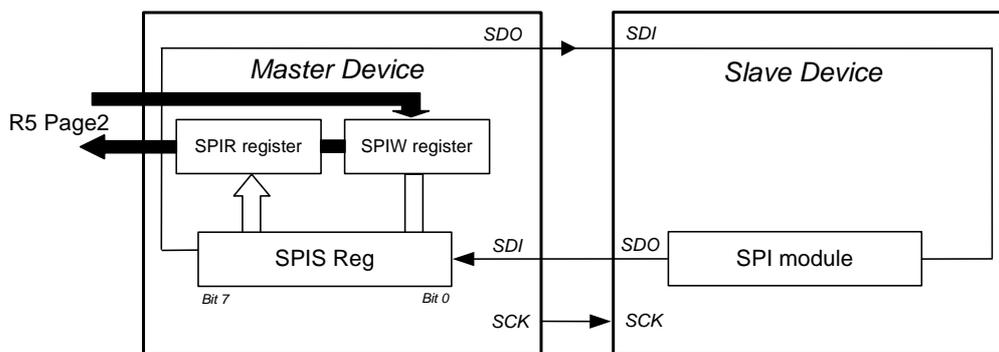


Figure 7-2a Single SPI Master / Slave Communication

Figure 7-2 shows how SPI communicates with other device by SPI module. If SPI is a master controller, it sends clock through the SCK pin. An 8-bit data is transmitted and received at the same time. If SPI, however, is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted on a basis of both the clock rate and the selected edge.

Bit 0 ~ Bit 2 (SBR0 ~ SBR2): SPI baud rate selection bits

SBR2	SBR1	SBR0	Mode	Baud Rate
0	0	0	Master	Fosc
0	0	1	Master	Fosc/2
0	1	0	Master	Fosc/4
0	1	1	Master	Fosc/8
1	0	0	Master	Fosc/16
1	0	1	Master	Fosc/32
1	1	1	Slave	–
1	1	0	Master	16.384k

**NOTE**  
Fosc = CPU instruction clock

**For example:**

If PLL is enabled and the main clock selected as 3.5826 MHz, the instruction clock is  $3.5826\text{MHz}/2 \rightarrow F_{osc}=3.5862 \text{ MHz} / 2$

If PLL is enabled and the main clock selected as 3.5826 MHz, the instruction clock is  $0.895\text{MHz}/2 \rightarrow F_{osc}=0.895 \text{ MHz} / 2$

If PLL is disabled, the instruction clock is  $32.768\text{kHz} / 2 \rightarrow F_{osc}=32.768\text{kHz} / 2$ .

**Bit 3 (SCES):** SPI clock edge selection bit

**0:** Data shifts out on a rising edge, and shifts in on a falling edge. Data is hold during a low level.

**1:** Data shifts out on a falling edge, and shifts in on a rising edge. Data is hold during a high level.

**Bit 4 (SE):** SPI shift enable bit

**0:** Reset as soon as the shifting is complete, and the next byte is ready to shift.

**1:** Start to shift, and keep on 1 while the current byte is still being transmitted.

**NOTE**

*This bit has to be reset by software.*

**Bit 5 (SRO):** SPI read overflow bit

**0:** No overflow

**1:** A new data is received while the previous data is still being hold in the SPIB register. In this situation, the data in the SPIS register will be destroyed. To avoid setting this bit, it is better for users to read the SPIB register even if transmission is implemented only.

**NOTE**

*This can only occur in slave mode.*

**Bit 6 (SPIE):** SPI enable bit

**0:** Disable SPI mode

**1:** Enable SPI mode

**Bit 7 (RBF):** SPI read buffer full flag

**0:** Receiving is not finished yet, SPIB is empty.

**1:** Receiving is finished, SPIB is full.



**SPIR reg.:** Read buffer

The buffer will be updated when the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared when the SPIR register is read.

**SPIW reg.:** Write buffer

The buffer will ignore any write until the 8-bit shifting is completed. The SE bit will be kept at "1" if the communication is still in process. This flag must be cleared as the shifting is completed. You can determine if the next write attempt is available.

**SBR2 ~ SBR0:** Programming of the clock frequency/rates and sources.

**Clock Select:** Select either the internal instruction clock or the external 16.338kHz clock as the shifting clock.

**Edge Select:** Selecting the appropriate clock edges by programming the SCES bit.

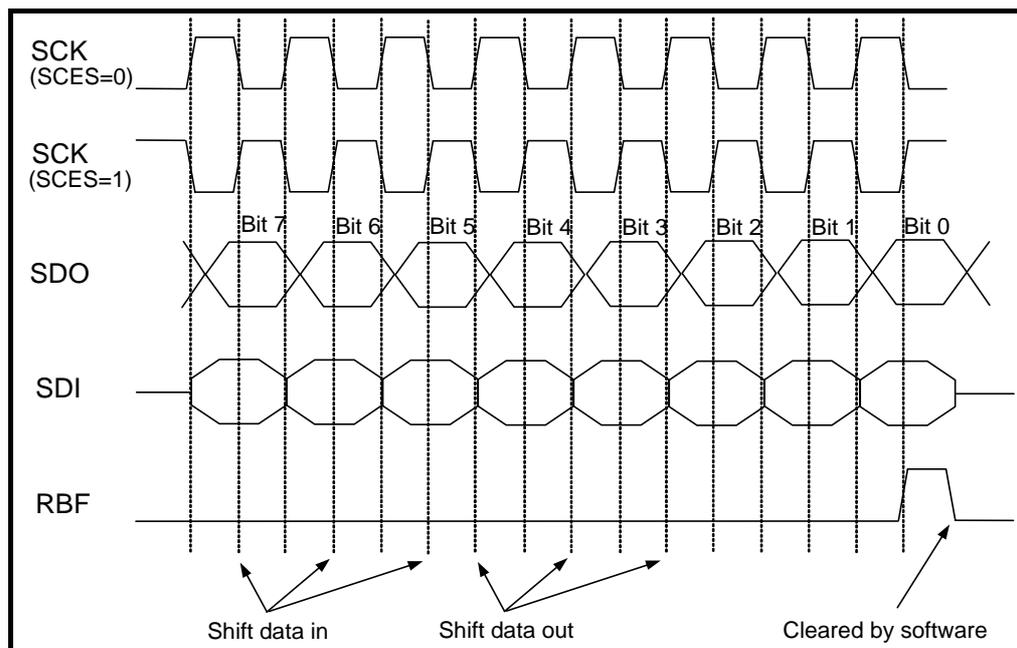


Figure 7-2c SPI Timing Diagram

■ Page 3 (PWMCON)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0
R/W-0							

**Bit 0 ~ Bit 1 (T1P0 ~ T1P1):** TMR1 clock prescale option bits

T1P1	T1P0	Prescale
0	0	1:2 (Default)
0	1	1:8
1	0	1:32
1	1	1:64

**Bit 2 ~ Bit 3 (T2P0 ~ T2P1):** TMR2 clock prescale option bits

T2P1	T2P0	Prescale
0	0	1:2 (Default)
0	1	1:8
1	0	1:32
1	1	1:64

**Bit 4 (T1EN):** TMR1 enable bit  
**0:** TMR1 is off (default value)  
**1:** TMR1 is on

**Bit 5 (T2EN):** TMR2 enable bit  
**0:** TMR2 is off (default value)  
**1:** TMR2 is on

**Bit 6 (PWM1E):** PWM1 enable bit  
**0:** PWM1 is off (default value), and its related pin carries out the PC1 function.  
**1:** PWM1 is on, and its related pin is automatically set as output.

**Bit 7 (PWM2E):** PWM2 enable bit  
**0:** PWM2 is off (default value), and its related pin carries out the PC2 function.  
**1:** PWM2 is on, and its related pin is automatically set as output.

### 7.2.7 R6 (Port 6 I/O Data, LCD Data, SPI Data Buffer, PWM1 Duty)

■ Page 0 (Port 6 I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60
R/W							

**Bit 0 ~ Bit 8 (P60 ~ P67):** 8-bit Port 6 I/O data register

Use the IOC register to define each bit as input or output.

**■ Page 1 (LCD Data)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0
R/W							

**Bit 0 ~ Bit 7 (LCDD0 ~ LCDD7):** LCD data buffer for LCD RAM read or write

LCD Data vs. COM-SEG		LCD Address (LCDA3 ~ LCDA0)
LCDD7 ~ LCDD4	LCDD3 ~ LCDD0	
COM3 ~ COM0	COM3 ~ COM0	
SEG1	SEG0	00H
SEG3	SEG2	01H
SEG5	SEG4	02H
SEG7	SEG6	03H
SEG9	SEG8	04H
SEG11	SEG10	05H
SEG13	SEG12	06H
SEG15	SEG14	07H
SEG17	SEG16	08H
SEG19	SEG18	09H
SEG21	SEG20	0AH
SEG23	SEG22	0BH
SEG25	SEG24	0CH
SEG27	SEG26	0DH
SEG29	SEG28	0EH
SEG31	SEG30	0FH

**■ Page 2 (SPI Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPIB7	SPIB6	SPIB5	SPIB4	SPIB3	SPIB2	SPIB1	SPIB0
R/W							

**Bit 0 ~ Bit 7 (SPIB0 ~ SPIB7):** SPI data buffer

If you write data to this register, the data will be written to the SPIW register. If you read this data, it will read the data from the SPIR register. Refer to Figure 7-2b, *SPI Structure* for further details.

**■ Page 3 (DT1L: Least Significant Byte of Duty Cycle of PWM1)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1[7]	PWM1[6]	PWM1[5]	PWM1[4]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
R/W-0							

A specified value keeps the PWM1 output to remain at high until the value matches with TMR1.

## 7.2.8 R7 (Port 7 I/O Data, Data RAM Bank, PWM1 Duty, ADC Output and Resolution)

### ■ Page 0 (Port 7 I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70
R/W							

**Bit 0 ~ Bit 7 (P70 ~ P77):** 8-bit Port 7 (0~7) I/O data register

Use the IOC register to define each bit as input or output.

### ■ Page 1 (ADC Output Data (8~9), AD Resolution Control, Data RAM Bank Selection Bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	AD9	AD8	DARES	ADRES	RAM_B1	RAM_B0
		R	R	R/W-0	R/W-0	R/W-0	R/W-0

**Bit 0~Bit 1 (RAM\_B0~RAM\_B1):** Data RAM bank selection bits

Each bank consisted of Address 0 ~ Address 255, and has a total of 256 (0.25k) bytes RAM size.

Data RAM bank selection: (Total RAM = 1K)

RAM_B1	RAM_B0	Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

**Bit 2 (ADRES):** Resolution selection for ADC

**0:** ADC is 8-bit resolution

When the 8-bit resolution is selected, the most significant (MSB) 8-bit data output of the internal 10-bit ADC will be mapped to RB Page 1. The R7 Page 1 Bits 4 ~5 therefore, will be of no use.

**1:** ADC is 10-bit resolution

When the 10-bit resolution is selected, 10-bit data output of the internal 10-bit ADC will be mapped exactly to RB Page 1 and R7 Page 1 Bits 4 ~5.

#### NOTE

For program compatibility, if ADC is used, set this bit to "1" because 8-bit ADC resolution mode is not supported in the mask version of EM78569A.

**Bit 3: Resolution Selection for DAC**

**0:** DAC is 8-bit resolution

**When the 8-bit resolution is selected, the most significant (MSB) 8-bit data output of the internal 10-bit DAC will be mapped to RA Page 1. Therefore, R5 Page 1 Bits 6 ~7 will be of no use.**

**1:** DAC is 10-bit resolution

**When 10-bit resolution is selected, 10-bit data output of the internal 10-bit DAC will be mapped exactly to RA Page 1 and R5 Page 1 Bits 6 ~7.**

**Bit 4 ~ Bit 5 (AD8 ~ AD9):** Most significant 2 bits of 10-bit ADC conversion output data  
Combining these two bits with RB PAGE1 will result to a complete 10-bit ADC conversion output data.

**Bit 6 ~Bit 7:** NOT defined. **Do not use.**

■ **Page 2 (NOT defined. Do not use)**

■ **Page 3 (DT1H: Most Significant Byte (Bit 1 ~ Bit 0) of PWM1 Duty Cycle)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PWM1[9]	PWM1[8]
						R/W-0	R/W-0

**Bit 0 ~ Bit 1 (PWM1[8] ~ PWM1[9]):** Most Significant Byte of PWM1 Duty Cycle  
A specified value keeps the PWM1 output to remain at high until the value matches with TMR1.

**Bit 2 ~ Bit 7: (Not defined. Do not use)**

### 7.2.9 R8 (Port 8 I/O Data, Data RAM Address, PWM1 Period)

■ **Page 0 (Port 8 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P87	P86	P85	P84	P83	P82	P81	P80
R/W							

**Bit 0 ~ Bit 7 (P80 ~ P87):** 8-bit Port 8 (0~7) I/O data register  
Use the IOC register to define each bit as input or output.

■ Page 1 (“VERSEL = 0”: Data RAM Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
R/W-0							

**Bit 0 ~ Bit 7 (RAM\_A0 ~ RAM\_A7):** data RAM address

The available data RAM bank selection is from R7 Page 1 Bit 0 ~ Bit 1 (RAM\_B0 ~ RAM\_B1).

**NOTE**  
When “VERSEL = 1”, Data RAM Address Buffer is mapped to RB Page 2.

■ Page 2 (NOT defined. Do not use)

■ Page 3 (PRD1: PWM1 Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
R/W-0							

The content of this register is a period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

### 7.2.10 R9 (Port 9 I/O Data, Data RAM Data Buffer, PWM2 Duty)

■ Page 0 (Port 9 I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90
R/W							

**Bit 0 ~ Bit 7 (P90 ~ P97):** 8-bit Port 9 (0~7) I/O data register

Use the IOC register to define each bit as input or output.

■ Page 1 (Data RAM Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
R/W							

**Bit 0 ~ Bit 7 (RAM\_D0 ~ RAM\_D7):** Data RAM’s data

The address for data RAM is accessed from R8 Page 1. The data RAM bank is selected by R7 Page 1 Bit 0 ~ Bit 1 (RAM\_B0 ~ RAM\_B1).

■ Page 2 (NOT defined. Do not use)

**■ Page 3 (DT2L: Least Significant Byte ( Bit 7 ~ Bit 0 ) of PWM2 Duty Cycle)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2[7]	PWM2[6]	PWM2[5]	PWM2[4]	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]
R/W-0							

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2.

**7.2.11 RA (PLL, Main Clock Selection, Watchdog Timer, DAC Output Data Buffer, PWM2 Duty)**
**■ Page 0 (PLL Enable Bit, Main Clock Select Bits, Watchdog Timer Enable Bit)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PLLEN	CLK2	CLK1	CLK0	-	-	WDTEN
R/W-0	R/W-0	R/W-0	R/W-1	R/W-1			R/W-0

**Bit 0 (WDTEN):** Watchdog control bit

0: Disable

1: Enable

Use the WDTC instruction to clear the watchdog counter. The counter's clock source is 32768/2 Hz. If the prescaler is assigned to TCC, the Watchdog will time out by  $(1/32768) \times 2 \times 256 = 15.625$  ms. If the prescaler is assign to WDT, the time out will be longer, depending on the prescaler ratio.

**Bit 1 ~ Bit 2:** Not defined. Do not use.

**Bit 3 ~ Bit 5 (CLK0 ~ CLK2):** Main clock selection bits

You can choose different frequency for the main clocks; CLK0, CLK1, and CLK2. All available clock selections are listed below.

PLLEN	CLK2	CLK1	CLK0	Sub Clock	Main Clock	CPU Clock
1	0	0	0	32.768kHz	447.829kHz	447.829kHz (Normal mode)
1	0	0	1	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	0	32.768kHz	1.791 MHz	1.791 MHz (Normal mode)
1	0	1	1	32.768kHz	3.582 MHz	3.582 MHz (Normal mode)
1	1	0	0	32.768kHz	7.165 MHz	7.165 MHz (Normal mode)
1	1	0	1	32.768kHz	10.747 MHz	10.747 MHz (Normal mode)
1	1	1	0	32.768kHz	14.331 MHz	14.331 MHz (Normal mode)
1	1	1	1	32.768kHz	17.91 MHz	17.91 MHz (Normal mode)
0	Don't care	Don't care	Don't care	32.768kHz	Don't care	32.768kHz (Green mode)

**Bit 6 (PLEN):** PLL's power control bit which is a CPU mode control register

**0:** Disable PLL

**1:** Enable PLL

If PLL is enabled, the CPU will operate at Normal mode (high frequency). Otherwise, it will run at Green mode (low frequency, 32768 Hz).

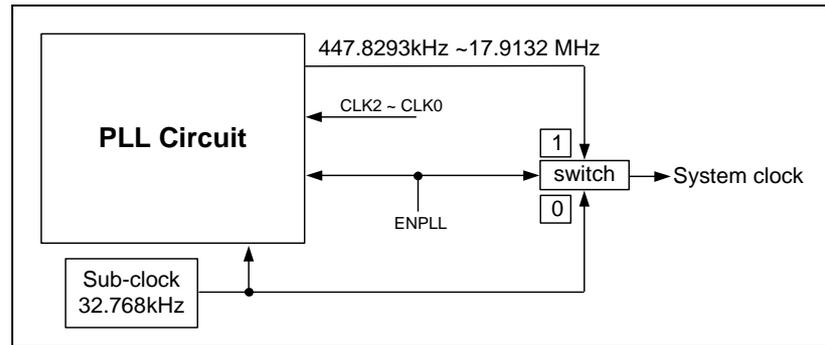


Figure 7-3a Correlation between 32.768kHz and PLL

**Bit 7:** Unused register (**keep this bit to “0” to avoid unexpected errors**)

The status after wake-up and the wake-up sources are listed below.

Wake-up Signal	Sleep Mode
	RA (7, 6)=(0, 0) + SLEP
TCC time out IOCF Bit 0=1	No function
Counter 1 time out IOCF Bit 1=1	No function
Counter 2 time out IOCF Bit 2=2	No function
WDT time out	Reset and jump to Address 0
Port 8 (0~3) RE Page 0 Bit 0 or Bit 1 or Bit 2 or Bit 3 = 1	Reset and Jump to Address 0
Port 7 (0~3) IOCF Bit 3 or Bit 4 or Bit 5 =1	Reset and Jump to Address 0

**NOTE**

- Port 70's wake-up function is controlled by IOCF Bit 3. It is falling edge or rising edge triggered (controlled by CONT register Bit 7).
- Port 7 (1~3) wake-up functions are controlled by IOCF Bits (4, 5, 7). They are falling edge triggered.
- Port 80~Port 83 wake-up function are controlled by RE Page 0 Bit 0 ~ Bit 3. They are falling edge triggered.

**■ Page 1 (DAC Output Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
R/W-1							

**Bit 0 ~ Bit 7 (DA0 ~ DA7):** These 8 bits are full DAC data buffer when 8-bit resolution is selected (R7 Page 1 Bit 7 DAREF = 0), or the least significant 8-bit data when 10-bit resolution (DAREF = 1) is selected.

**■ Page 2 (Multiplier Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INS	-	INDR	PLUS	MROPT3	MROPT2	MROPT1	MROPT0
W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bit 0 ~ Bit 3 (MROPT0 ~ MROPT3):** Multiplier operation mode control

MROPT3-MROPT0	Mode	Description
0 0 0 0	$MR = \text{sign}(X) * \text{sign}(Y)$	Sign-sign multiplication
0 0 0 1	$MR = \text{sign}(X) * \text{unsign}(Y)$	Sign-unsign multiplication
0 0 1 0	$MR = \text{unsign}(X) * \text{sign}(Y)$	Unsign-sign multiplication
0 0 1 1	$MR = \text{unsign}(X) * \text{unsign}(Y)$	Unsign-unsign multiplication
1 0 0 0	$MR = MR + \text{sign}(X) * \text{sign}(Y)$	Sign-sign accumulated multiplication addition
1 0 0 1	$MR = MR + \text{sign}(X) * \text{unsign}(Y)$	Sign-unsign accumulated multiplication addition
1 0 1 0	$MR = MR + \text{unsign}(X) * \text{sign}(Y)$	Unsign-sign accumulated multiplication addition
1 0 1 1	$MR = MR + \text{unsign}(X) * \text{unsign}(Y)$	Unsign-unsign accumulated multiplication addition
1 1 0 0	$MR = MR - \text{sign}(X) * \text{sign}(Y)$	Sign-sign accumulated multiplication subtraction
1 1 0 1	$MR = MR - \text{sign}(X) * \text{unsign}(Y)$	Sign-unsign accumulated multiplication subtraction
1 1 1 0	$MR = MR - \text{unsign}(X) * \text{sign}(Y)$	Unsign-sign accumulated multiplication subtraction
1 1 1 1	$MR = MR - \text{unsign}(X) * \text{unsign}(Y)$	Unsign-unsign accumulated multiplication subtraction
0 1 0 0 ~ 0 1 1 1	Unused	-



**Bit 4 (PLUS):** Base on “VERSEL,” this bit’s definition is different. If VERSEL = 0, data RAM and multiplicand Y\_address buffer is independent. When VERSEL = 1, both data RAM and multiplicand Y\_address are directed to RB Page 2 for buffering.

VERSEL	PLUS	Data RAM Address Buffer	Multiplicand Y_Address Buffer	Effect
0	0	R8 Page 1	RB Page 2	Data RAM's address will not auto-increase after an access. Y_address will not auto-increase after running instruction “INT A”.
0	1	R8 Page 1	RB Page 2	Data RAM's address will not auto-increase after an access. Y_address will auto-increase after running instruction “INT A”.
1	0	RB Page 2	RB Page 2	Data RAM's address will auto-increase after an access. Y_address will not auto-increase after running instruction “INT A”.
1	1	RB Page 2	RB Page 2	Data RAM's address will auto-increase after an access. Y_address will auto-increase after running instruction “INT A”.

**Bit 5 (INDR):** Indirect address pointer enable control

**0:** Disable

**1:** Enable

When (INDR, PLUS) = (1, 1), the address pointer and address auto-increment functions are enabled. When these functions are enabled, RB Page 2 acts as address pointer and it will automatically increment by one after “INT A” instruction execution. That is to say, RB Page 2 = RB Page 2 + 1. The multiplicand Y data is stored in R9 Page 1 data RAM buffer.

Bit 5 (INDR)	Bit 4 (PLUS)	Function
1	0	<ul style="list-style-type: none"> <li>• Enable indirect address pointer</li> <li>• RB Page 2 acts as Multiplicand Y data address pointer of multiplier</li> <li>• Multiplicand Y data is stored in R9 Page 1 of multiplier</li> <li>• Disable Multiplicand Y data address auto-increment of multiplier</li> </ul>
1	1	<ul style="list-style-type: none"> <li>• Enable indirect address pointer</li> <li>• RB Page 2 acts as Multiplicand Y data address pointer of multiplier</li> <li>• Multiplicand Y data is stored in R9 Page 1 of multiplier</li> <li>• Enable Multiplicand Y data address auto-increment of multiplier</li> </ul>
0	x	<ul style="list-style-type: none"> <li>• Disable indirect address pointer</li> <li>• Disable Multiplicand Y data address auto-increment of multiplier</li> <li>• RB Page 2 acts as Multiplicand Y data buffer of multiplier</li> <li>• Multiplicand Y data is stored in RB Page 2 of multiplier</li> </ul>

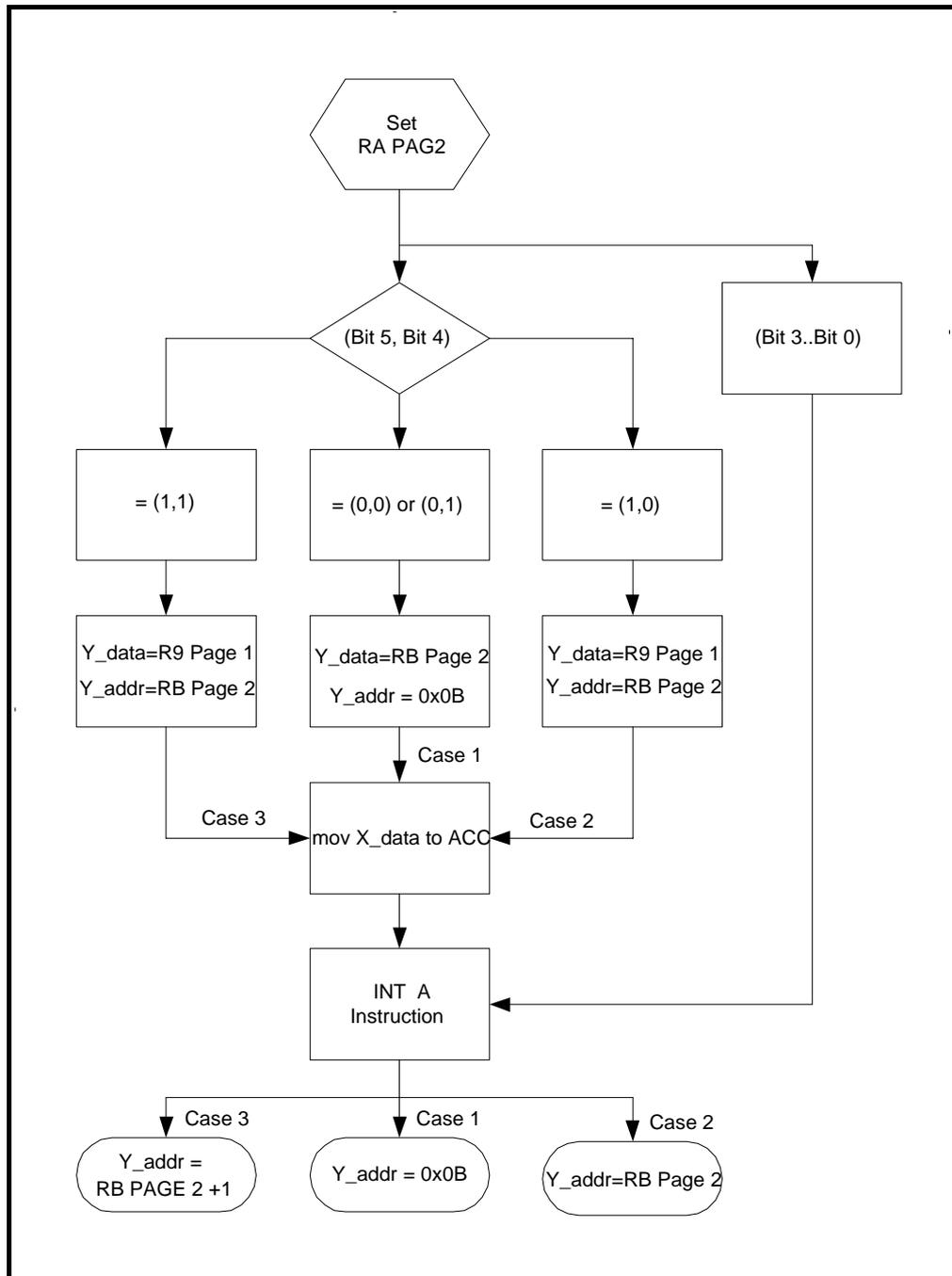


Figure 7-3b Multiplier Control Flow Chart

**Bit 6:** Undefined. Do not use this bit.

**Bit 7 (INS):** Instructions "ADD" and "SUB" calculation selections. **This bit is a write only bit.**

This bit is defined according to "VERSEL" status. If "VERSEL" = 0, this bit is undefined. If "VERSEL" = 1, this bit will affect the results of "ADD" and "SUB" instructions.

VERSEL (Code Option)	INS (RA Page 2 Bit 7)	Instruction	Execute
0	X	ADD A , R	$A + R \rightarrow A$
		ADD R , A	$A + R \rightarrow R$
		ADD A , K	$A + K \rightarrow A$
		SUB A , R	$R - A \rightarrow A$
		SUB R , A	$R - A \rightarrow R$
		SUB A , K	$K - A \rightarrow A$
1	0	ADD A , R	$A + R \rightarrow A$
		ADD R , A	$A + R \rightarrow R$
		ADD A , K	$A + K \rightarrow A$
		SUB A , R	$R - A \rightarrow A$
		SUB R , A	$R - A \rightarrow R$
		SUB A , K	$K - A \rightarrow A$
1	1	ADD A , R	$A + R + C \rightarrow A$
		ADD R , A	$A + R + C \rightarrow R$
		ADD A , K	$A + K + C \rightarrow A$
		SUB A , R	$R - A - /C \rightarrow A$
		SUB R , A	$R - A - /C \rightarrow R$
		SUB A , K	$K - A - /C \rightarrow A$

■ Page 3 (DT2H: Most Significant Byte (Bit 1 ~ Bit 0) of PWM2 Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PWM2[9]	PWM2[8]
						R/W-0	R/W-0

**Bit 0 ~ Bit 1 (PWM2[8] ~ PWM2[9]):** Most Significant Byte of PWM1 Duty Cycle

A specified value keeps the PWM1 output to remain high until the value matches with TMR1.

**Bit 2 ~ Bit 7:** Not defined. Do not use.

### 7.2.12 RB (Port B I/O Data, ADC Output Data Buffer, PWM2 Period)

■ Page 0 (Port 9 I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W							

**Bit 0 ~ Bit 7 (PB0 ~ PB7):** 8-bit Port B I/O data register

Use the IOC register to define each bit as input or output.

■ **Page 1 (ADC Output Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R	R	R	R	R	R	R	R

**Bit 0 ~ Bit 7 (AD0 ~ AD7):** These 8 bits are full ADC data buffer when 8-bit resolution is selected (R7 Page 1 Bit 2 ADREF = 0), or the least significant 8-bit data when 10-bit resolution (ADREF = 1) is selected.

■ **Page 2 (Multiplicand Y Data Buffer and Data RAM's Data Buffer)**

Base on "VERSEL," this page has different definition.

● **When VERSEL = 0:**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MULY7	MULY6	MULY5	MULY4	MULY3	MULY2	MULY1	MULY0
R/W-0							

**Bit 0 ~ Bit 7 (MULY0 ~ MULY7):** Multiplicand Y data buffer of multiplier

The multiplier performs multiplication with  $X*Y$ . The multiplier data Buffer X is ACC and the multiplicand data Buffer Y is RB Page 2. The maximum 24-bit multiplication result (MR) is stored in RC Page 2 ~ RE Page 2. That is to say,  $MR = X*Y$ .

● **When VERSEL = 1:**

Under this status, RB Page 2 is defined as multiplicand Y data buffer and Data RAM address buffer.

**Example 1 :** Read data from continuous data RAM address:

```

MOV      A , @0b00111111
AND      0x03 , A
BS       0x03 , 7      ; Set R register to Page 2
CLR      0x0B          ; Set RAM address = 0
BS       0x0A , 4      ; Enable address auto-increase function
BC       0x03 , 7
BS       0x03 , 6      ; Set R register to Page 1
MOV      A , @0b11111100
AND      0x07 , A      ; Set RAM Bank 0
MOV      A , 0x09      ; Read Data RAM Address 0x00 data
MOV      A , 0x09      ; Read Data RAM Address 0x01 data
MOV      A , 0x09      ; Read Data RAM Address 0x02 data
:
:

```

**Example 2 : Continuous multiplication and addition operation:**

```

MOV    A , @0b00111111
AND    0x03 , A
BS     0x03 , 7      ; Set R register to Page 2
CLR    0x0C
CLR    0x0D
CLR    0x0E      ; Clear MR = 0
BS     0x0A , 5      ; Enable multiplier's indirect address mode
BS     0x0A , 4      ; Enable address auto-increase function
CLR    0x0B      ; Set Address = 0
MOV    A , @0x55
INT    A          ; Multiplication instruction, operate MR ←
                  0x55(A) x (Address 0' data)
INT    A          ; MR ← 0x55(A) x (Address 1' data) + MR
INT    A          ; MR ← 0x55(A) x (Address 2' data) + MR
      :
      :

```

■ **Page 3 (PRD2: Period of PWM2)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
R/W-0							

The content of this register is a period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

**7.2.13 RC (Port C I/O Data, Counter 1 Data, LSB Multiplication Result)**

■ **Page 0 (Port 9 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W							

**Bit 0 ~ Bit 7 (PC0 ~ PC7):** 8-bit Port C (0~7) I/O data register  
 Use the IOC register to define each bit as input or output.

■ **Page 1 (Counter 1 Data Register)**

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0							

**Bit 0 ~ Bit 7 (CN10 ~ CN17):** Counter1 buffer for read and write.

Counter 1 is an 8-bit up-counter with 8-bit prescaler that you can use with the RC Page 1 to preset and read its counter (write → preset). After an interrupt, it will reload the preset value.

**Write Example:**

```
MOV      0x0C, A          ; Write the data at accumulator to Counter 1
                          ; (preset)
```

**Read Example:**

```
MOV      A, 0x0C         ; Read the data at Counter 1 to accumulator
```

■ **Page 2 (LSB 8-bit Multiplication Result)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
R/W							

**Bit 0 ~ Bit 7 (MR0 ~ MR7):** Multiplication result data

The multiplier performs multiplication with X\*Y. The multiplier data Buffer X is ACC (accumulator) and the multiplicand data Buffer Y is RB Page 2. The LSB 8-bit of maximum 24-bit multiplication result (MR) is stored in RC Page 2.

RC Page 2 = MR (0~7) = LSB 8-bit (X\*Y)

■ **Page 3 (NOT defined. Do not use)**

**7.2.14 RD (LCD Control, Counter 2 Data, MID Multiplication Result)**

■ **Page 0 (LCD Driver Control Bits)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	<i>VERSEL</i>	<i>PHO</i>	1	-	LCD_C1	LCD_C0	LCD_M
	<i>R/W-0</i>	<i>R/W-0</i>	R/W-0		R/W-0	R/W-0	R/W-0

**Bit 0 (LCD\_M):** LCD operation method including duty and frame frequency

**Bit 1 ~ Bit 2 (LCD\_C0 ~ LCD\_C1): LCD display control**

LCD_C1	LCD_C0	LCD_M	LCD Display Control	Duty	Bias
0	0	0	Change duty	1/4	1/3
		1	Disable (turn off LCD)	1/2	1/3
0	1	:	Blanking	:	:
1	1	:	LCD display enable	:	:

**NOTE:** To change the display duty, the LCD\_C1 & LCD\_C0 must be set to "00"

The controller can drive the LCD directly. The LCD block is made up of common driver, segment driver, display LCD RAM, common output pins, segment output pins, and LCD operating power supply. The basic structure contains a timing control. This timing control uses the basic frequency of 32.768kHz to generate the proper timing for different duty and display access.

RD Page 0 Bit 0 ~ Bit 2 are LCD control bits for LCD driver. These LCD control bits determine the duty, the number of common and the frame frequency. The LCD display (disable, enable, blanking) is controlled by Bit 1 and Bit 2. The driving duty is determined by Bit 0. The display data is stored in the LCD RAM of which address and data access are controlled by Registers R5 Page 1 and R6 Page 1.

User can regulate the LCD display contrast through IOC5 Page 0 Bit 0 ~ Bit 3 (BIAS0 ~ BIAS3). Up to 16 levels of contrast setting are provided for convenient and better display.

**Bit 3:** Undefined. Do not use.

**Bit 4:** Always set this bit to "1"

**Bit 5 (PHO):** PC0 status select.

**0:** PC0 is defined as normal I/O.

**1:** PC0 is assigned to Phase 1 output (VERSEL must = 1)

**Bit 6 (VERSEL):** Version select

Function	VERSEL = 0	VERSEL = 1
Data RAM address	R8 Page 1	RB Page 2
Data RAM address auto-increase	Not supported	Enable
"ADD" & "SUB" include "carry" bit	Not supported	Determined by RA Page 2 Bit 7
Phase CLK output	Not supported	Phase1 CLK out from PC0 (determined by PHO)

**Bit 7:** Undefined. Do not use.

**NOTE**

*Bit 5 and Bit 6 are only used with EM78P569A Developing Tool (ICE569). In OTP and mask chip, these two bits are mapped to the code option. Set these two bits to a fixed value initially and do not change the value in the program design. Furthermore, set Bit 4 to "1." The AD function is different between ICE 569 and EM78P569A*

**■ Page 1 (Counter 2 Data Register)**

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W-0							

**Bit 0 ~ Bit 7 (CN20 ~ CN27):** Counter 2 buffer for read and write

Counter 2 is an 8-bit up-counter with 8-bit prescaler that you can use with the RD Page 1 to preset and read the counter (write → preset). After an interrupt, it will reload the preset value.

**Write Example:**

```
MOV      0x0D, A      ; Write the data at accumulator to Counter 2
                        ; (preset)
```

**Read Example:**

```
MOV      A, 0x0D      ; Read the data at Counter 2 to accumulator
```

**■ Page 2 (MID 8-bit Multiplication Result)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8
R/W							

**Bit 0 ~ Bit 7 (MR8 ~ MR15):** Multiplication result data

The multiplier performs multiplication with  $X*Y$ . The multiplier data Buffer X is ACC (accumulator) and the multiplicand data Buffer Y is RB Page 2. The MID 8-bit of maximum 24-bit multiplication result (MR) is stored in RD Page 2.

RD Page 2 = MR (8~15) = MID 8-bit ( $X*Y$ )

**■ Page 3 (NOT defined. Do not use)**
**7.2.15 RE (Interrupt Flag, Wake-up Control, MSB Multiplication Result)**
**■ Page 0 (Interrupt flag, Wake-up Control Bits)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2	RBF	ADI	PWM1	/WUP83	/WUP82	/WUP81	/WUP80
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bit 0 (/WUP80):** Port 80 wake-up control,

**0:** Disable

**1:** Enable P80 pin wake-up function



- Bit 1 (/WUP81):** 81 wake-up control
  - 0:** Disable
  - 1:** Enable P81 pin wake-up function
- Bit 2 (/WUP82):** Port 82 wake-up control,
  - 0:** Disable
  - 1:** Enable P82 pin wake-up function
- Bit 3 (/WUP83):** Port 83 wake-up control,
  - 0:** Disable
  - 1:** Enable P83 pin wake-up function
- Bit 4 (PWM1):** PWM1 (Pulse Width Modulation Channel 1) interrupt flag  
 Set when a selected period is reached. Reset by software.
- Bit 5 (ADI):** ADC interrupt flag after a sampling
- Bit 6 (RBF):** SPI data transfer complete interrupt  
 If the SPI RBF meets rising edge signal (RBF is set to "1" when data transfer is completed), the CPU will set this bit.
- Bit 7 (PWM2):** PWM2 (Pulse Width Modulation Channel 2) interrupt flag  
 Set when a selected period is reached. Reset by software.

■ **Page 1 (NOT defined. Do not use)**

■ **Page 2 (MSB 8-bit Multiplication Result)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MR23	MR22	MR21	MR20	MR19	MR18	MR17	MR16
RW-0							

**Bit 0 ~ Bit 7 (MR23 ~ MR16):** Multiplication result data

The multiplier performs multiplication with  $X*Y$ . The multiplier data Buffer X is ACC (accumulator) and the multiplicand data buffer Y is RB Page 2. The MSB 8-bit of the maximum 24-bit multiplication result (MR) is stored in RE Page 2.  
 RE Page 2 = MR (16~23) = MSB 8-bit ( $X*Y$ )

■ **Page 3 (NOT defined. Do not use)**

### 7.2.16 RF (Interrupt Status)

■ (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT3	-	INT2	INT1	INT0	CNT2	CNT1	TCIF
R/W-0*		R/W-0*	R/W-0*	R/W-0*	R/W-0*	R/W-0*	R/W-0*

\* 0: No interrupt occurs    1: Interrupt requested

**Bit 0 (TCIF):** TCC timer overflow interrupt flag  
Set when TCC timer overflows

**Bit 1 (CNT1):** Counter 1 timer overflow interrupt flag  
Set when Counter 1 timer overflows

**Bit 2 (CNT2):** Counter 2 timer overflow interrupt flag  
Set when Counter 2 timer overflows

**Bit 3 (INT0):** External INT0 pin interrupt flag  
If Port 70 is a falling edge/rising edge (controlled by CONT register) trigger signal, CPU will set this bit.

**Bit 4 (INT1):** External INT1 pin interrupt flag  
If Port 71 is a falling edge trigger signal, the CPU will set this bit.

**Bit 5 (INT2):** External INT2 pin interrupt flag  
If Port 72 is a falling edge trigger signal, the CPU will set this bit.

**Bit 6:** Undefined. Do not use.

**Bit 7 (INT3):** External INT3 pin interrupt flag  
If Port 73 is a falling edge trigger signal, the CPU will set this bit.

**NOTE**  
*IOCF is the interrupt mask register for Read and Clear*

Trigger edge is as summarized below.

Signal	Trigger
TCC	Time out
Counter 1	Time out
Counter 2	Time out
INT0	Falling Rising edge
INT1	Falling edge
INT2	Falling edge
INT3	Falling edge

### 7.2.17 R10~R3F (General Purpose Register)

R10~R3F (Banks 0 ~ 3): All are general purpose registers.

## 7.3 Special Purpose Registers

### 7.3.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

### 7.3.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P70EG	INT	TS	RETBK	PAB	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

**Bit 3 (PAB):** Prescaler assigned bit

**0:** TCC

**1:** WDT

**Bit 4 (RETBK):** Return value back-up control for interrupt routine

**0:** Disable

**1:** Enable

When this bit is set to "1," the CPU will store the ACC, R3 status, and R5 PAGE automatically after an interrupt is triggered. It will be restored after execution of Instruction RETI. When this bit is set to "0," you need to store ACC, R3, and R5 Page in the user program.

**Bit 5 (TS):** TCC signal source

**0:** Internal instruction cycle clock

**1:** 16.384kHz

- Bit 6 (INT):** INT enable flag  
**0:** Interrupt masked by DISI or hardware interrupt  
**1:** Interrupt enabled by ENI/RETI instructions
- Bit 7 (P70EG):** Interrupt edge type of P70  
**0:** P70's interrupt source is a rising edge signal  
**1:** P70's interrupt source is a falling edge signal

The CONT register is readable (CONTR) and writable (CONTW).

■ **Timer Clock/Counter (TCC) and Watchdog Timer (WDT)**

An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only, i.e., one at a time. The counter is determined by the status of Bit 3 (PAB) of the CONT register. See the table on CONT register prescaler ratio under Bit 0 ~ Bit 2 at the beginning of this section.

Both TCC and prescaler are cleared each time a Write instruction to TCC is executed.

The prescaler can also be cleared by the WDTC and SLEP instructions when it is assigned to WDT mode. However, if the prescaler is assigned to TCC mode, it cannot be cleared by SLEP instructions.

The following is the TCC/WDT block diagram.

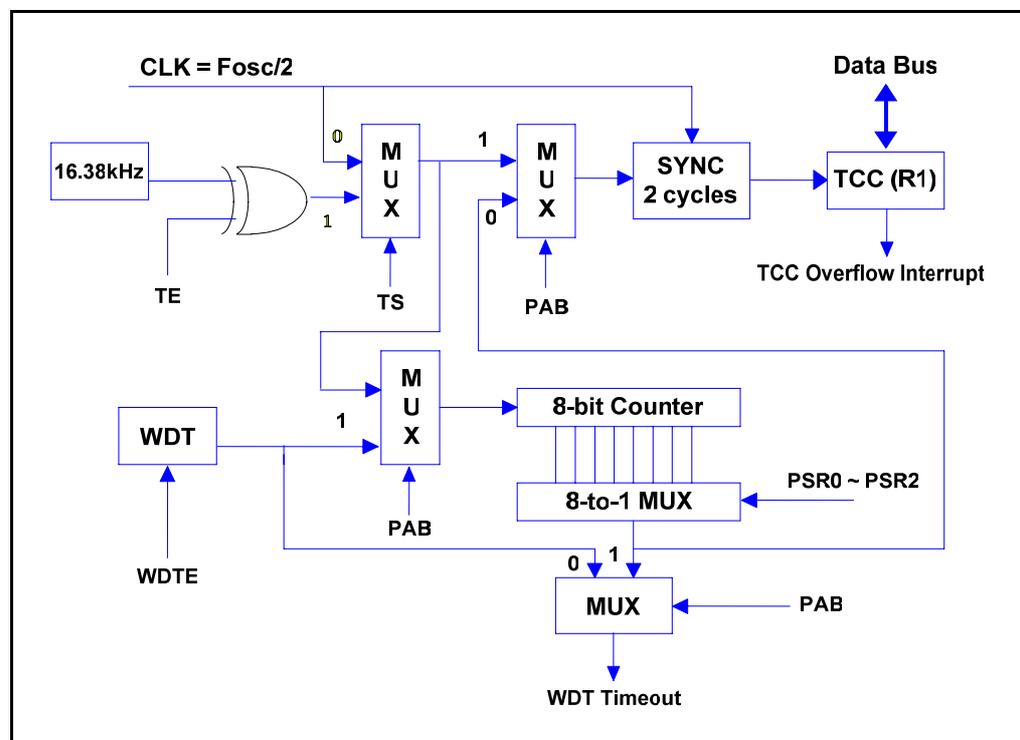


Figure 7-4 TCC/WDT Block Diagram

### 7.3.3 IOC5 (Port 5 I/O Control, LCD Bias Control)

■ Page 0 (LCD Bias Control Bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	-	BIAS3	BIAS2	BIAS1	BIAS0
R/W-1	R/W-1	R/W-1	-	R/W-0	R/W-0	R/W-0	R/W-0

**Bit 0 ~ Bit 3 (BIAS0 ~ BIAS3):** LCD operation voltage selection.  $V1 = VDD * (1 - n/60)$

BIAS3	BIAS2	BIAS1	BIAS0	Vop (=VDD-VLCD)	Example (VDD = 3V)
0	0	0	0	$VDD * (1-0/60)$	3V
0	0	0	1	$VDD * (1-1/60)$	2.95V
0	0	1	0	$VDD * (1-2/60)$	2.90V
0	0	1	1	$VDD * (1-3/60)$	2.85V
0	1	0	0	$VDD * (1-4/60)$	2.80V
:	:	:	:	:	:
1	1	0	1	$VDD * (1-13/60)$	2.35V
1	1	1	0	$VDD * (1-14/60)$	2.30V
1	1	1	1	$VDD * (1-15/60)$	2.25V

**Bit 4:** Undefined. Do not use.

**Bit 5 ~ Bit 7 (IOC55 ~ IOC57):** Port 5 (5~7) I/O direction control register

0: Set the relative I/O pin as output

1: Set the relative I/O pin into high impedance

• LCD Waveform for 1/3 Bias, 1/2 Duty

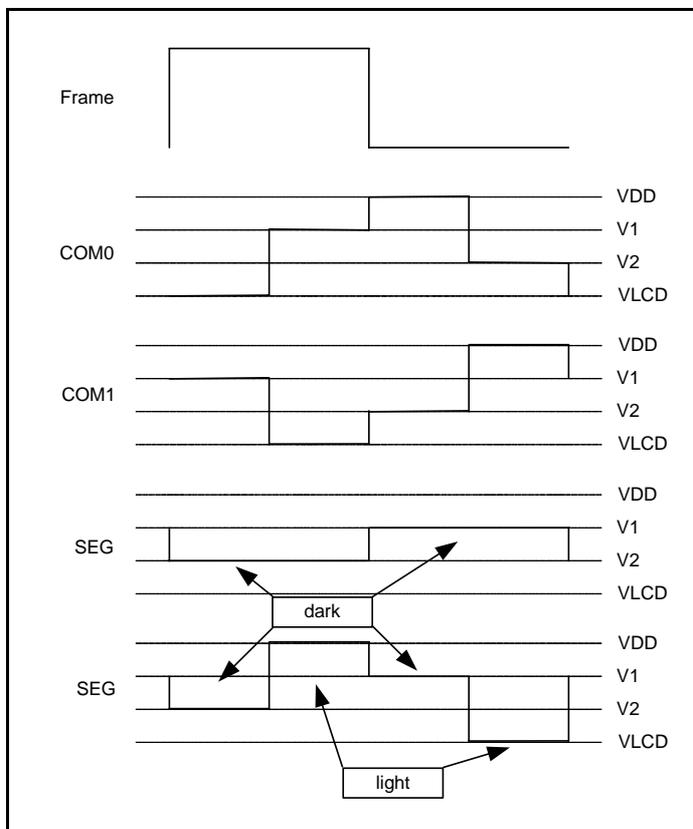


Figure 7-5a LCD Waveform for 1/3 Bias, 1/2 Duty

• LCD Waveform for 1/3 Bias, 1/4 Duty

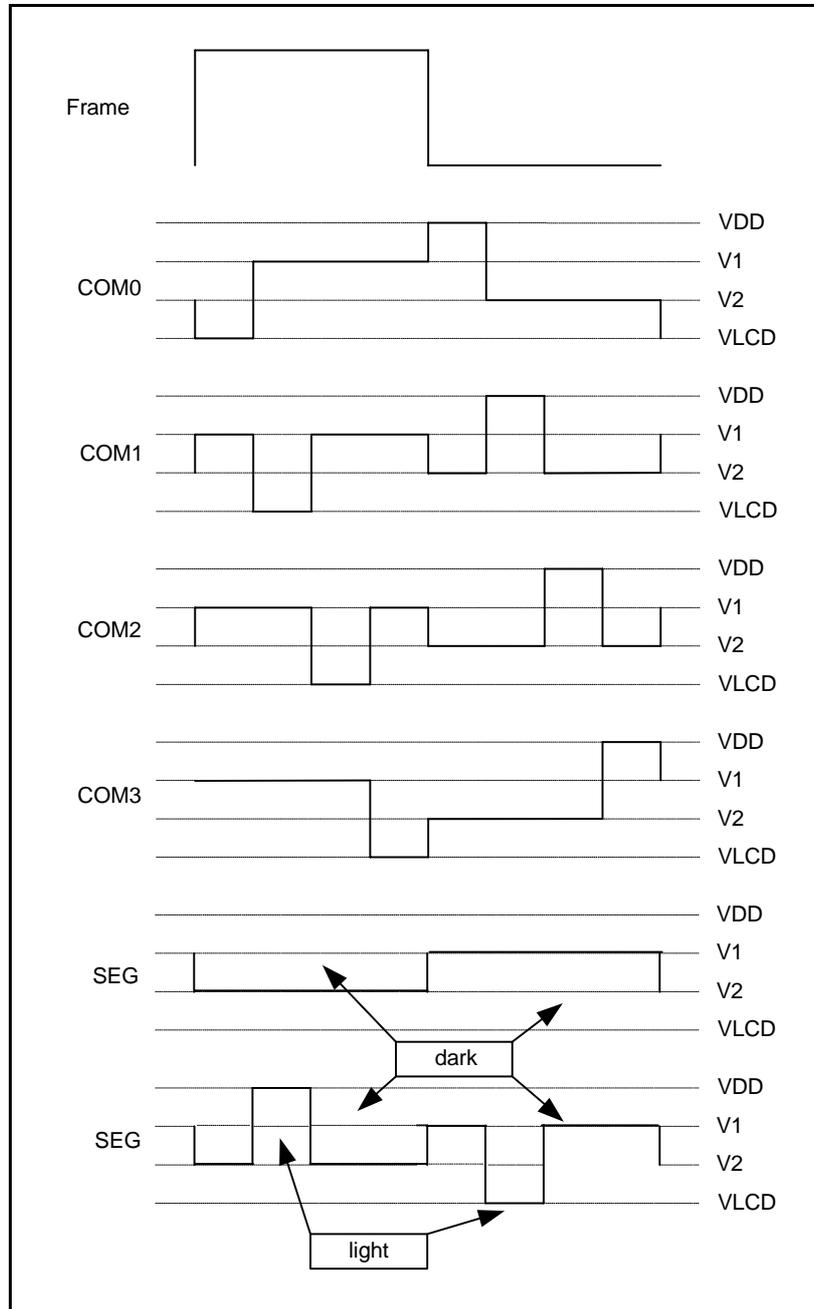


Figure 7-5b LCD Waveform for 1/3 Bias, 1/4 Duty

### 7.3.4 IOC6 (Port 6 I/O Control, P6\* Pins Switch Control)

#### ■ Page 0 (Port 6 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W-1							

**Bit 0 ~ Bit 7 (IOC60 ~ IOC67):** Port 6 (0~7) I/O direction control register

**0:** set the relative I/O pin as output

**1:** put the relative I/O pin into high impedance

#### ■ Page 1 (P6 Pins Switch Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	P66S	P65S	P64S	P63S	P62S	P61S	P60S
-	R/W-0						

#### NOTE

*Before using Bit 1 ~ Bit 6, set IOCC Page 1 Bit 0 (MS) = 1 to enable the port switching function*

**Bit 0 (P60S):** Select normal I/O Port 60 pin or Channel 1 input AD1 pin of ADC

**0:** P60 (I/O Port 60) pin is selected

**1:** AD1 (Channel 1 input of ADC) pin is selected

**Bit 1 (P61S):** Select normal I/O Port 61 pin or Channel 2 input AD2 pin of ADC

**0:** P61 (I/O Port 61) pin is selected

**1:** AD2 (Channel 2 input of ADC) pin is selected

**Bit 2 (P62S):** Select normal I/O Port 62 pin or Channel 3 input AD3 pin of ADC

**0:** P62 (I/O Port 62) pin is selected

**1:** AD3 (Channel 3 input of ADC) pin is selected

**Bit 3 (P63S):** Select normal I/O Port 63 pin or Channel 4 input AD4 pin of ADC

**0:** P63 (I/O Port 63) pin is selected

**1:** AD4 (Channel 4 input of ADC) pin is selected

**Bit 4 (P64S):** Select normal I/O Port 64 pin or Channel 5 input AD5 pin of ADC

**0:** P64 (I/O Port 64) pin is selected

**1:** AD5 (Channel 5 input of ADC) pin is selected

**Bit 5 (P65S):** Select normal I/O Port 65 pin or Channel 6 input AD6 pin of ADC

**0:** P65 (I/O Port 65) pin is selected

**1:** AD6 (Channel 6 input of ADC) pin is selected

**Bit 6 (P66S):** Select normal I/O Port 66 pin or external reference voltage input of ADC

**0:** P66 (I/O Port 66) pin is selected and the ADC reference voltage comes from internal VDD

**1:** VREF (external reference voltage input of ADC) pin is selected

This bit will switch the AD converter reference voltage from internal or external voltage source. If this bit is switched to internal, then the reference voltage will be VDD and Port 66 is used as a normal I/O Port. If it is switched to external reference voltage, then the voltage will be connected to VREF pin.

**Bit 7:** Undefined. Do not use.

### 7.3.5 IOC7 (Port 7 I/O Control, Port 7 Pull-high Control)

#### ■ Page 0 (Port 7 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
R/W-1							

**Bit 0 ~ Bit 7 (IOC70 ~ IOC77):** Port 7 (0~7) I/O direction control register

**0:** Set the relative I/O pin as output

**1:** Set the relative I/O pin into high impedance

#### ■ Page 1 (Port 7 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70
R/W-0							

**Bit 0 ~ Bit 7 (PH70 ~ PH77):** Port 7 Bit 0~Bit 7 pull-high control register

**0:** Disable pull-high function

**1:** Enable pull-high function

### 7.3.6 IOC8 (Port 8 I/O Control, Port 8 Pull-high Control)

#### ■ Page 0 (Port 8 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
R/W-1							

**Bit 0 ~ Bit 7 (IOC80 ~ IOC87):** Port 8 I/O direction control register

**0:** Set the relative I/O pin as output

**1:** Set the relative I/O pin into high impedance

■ Page 1 (Port 8 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80
R/W-0							

**Bit 0 ~ Bit 7 (PH80 ~ PH87):** Port 8 Bit 0~Bit 7 pull high control register

**0:** Disable pull-high function

**1:** Enable pull-high function

### 7.3.7 IOC9 (Port 9 I/O Control, Port 9 Switches)

■ Page 0 (Port 9 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1							

**Bit 0 ~ Bit 7 (IOC90 ~ IOC97):** Port 9 I/O direction control register

**0:** Set the relative I/O pin as output

**1:** Set the relative I/O pin into high impedance

■ Page 1 (Port 9 Switches)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97S	P96S	P95S	P94S	P93S	P92S	P91S	P90S
R/W-0							

**Bit 0 (P90S):** Switch to I/O Port 90 or LCD segment signal

**0:** (P90 pin is selected): Normal Port 90

**1:** (SEG20 pin): Segment output

**Bit 1 (P91S):** Switch to I/O Port 91 or LCD segment signal

**0:** (P91 pin is selected): Normal Port 91

**1:** (SEG19 pin): Segment output

**Bit 2 (P92S):** Switch to I/O Port 92 or LCD segment signal

**0:** (P92 pin is selected): Normal Port 92

**1:** (SEG18 pin): Segment output

**Bit 3 (P93S):** Switch to I/O Port 93 or LCD segment signal

**0:** (P93 pin is selected): Normal Port 93

**1:** (SEG17 pin): Segment output

**NOTE**

*P90~P93 are defined as AD input and shared with AD input channel*

**Bit 4 (P94S):** Switch to I/O Port 94 or LCD segment signal

0: (P94 pin is selected): Normal Port 94

1: (SEG16 pin): Segment output

**Bit 5 (P95S):** Switch to I/O Port 95 or LCD segment signal

0: (P95 pin is selected): Normal Port 95

1: (SEG15 pin): Segment output

**Bit 6 (P96S):** Switch to I/O Port 96 or LCD segment signal

0: (P96 pin is selected): Normal Port 96

1: (SEG14 pin): Segment output

**Bit 7(P97S):** Switch to I/O Port 97 or LCD segment signal

0: (P97 pin is selected): Normal Port 97

1: (SEG13 pin): Segment output

### 7.3.8 IOCA (Reserved)

■ Page 0 (NOT defined. Do not use)

■ Page 1 DAC Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
×	VREF	×	×	DAST/P67	×	×	×
-	R/W-0	-	-	R/W-0	-	-	-

**Bit 0~Bit 2:** Undefined. Do not use these three bits.

**Bit 3 (DAST/P67):** DAC enable control or P67 switch

0: Switch DAO/P67 pin as normal I/O P67

1: Enable DAC, enable DAC output buffer B1 and DAC output to DAO/P67 pin

When this bit is set through software, the DA converter will start converting and output result to DAO/P67 pin. If you clear this bit, the DA converter will stop and DAO/P67 pin will become normal I/O P67.

**Bit 4 ~ Bit 5** Undefined. Do not use these two bits.

**Bit 6 (VREF):** Reference voltage selection bit for DA converter circuit

DAC reference setting is shown below. Also refer to Figure 7-6 for DAC circuit diagram.

VREF	DAST/P67	Function
×	0	Disable 2.5V, disable DAC
1	1	Select 2.5V ref, enable 2.5V ref, enable DAC, enable output to DAO/P67 pin
0	1	Select VDD, disable 2.5V, enable DAC, enable output to DAO/P67 pin

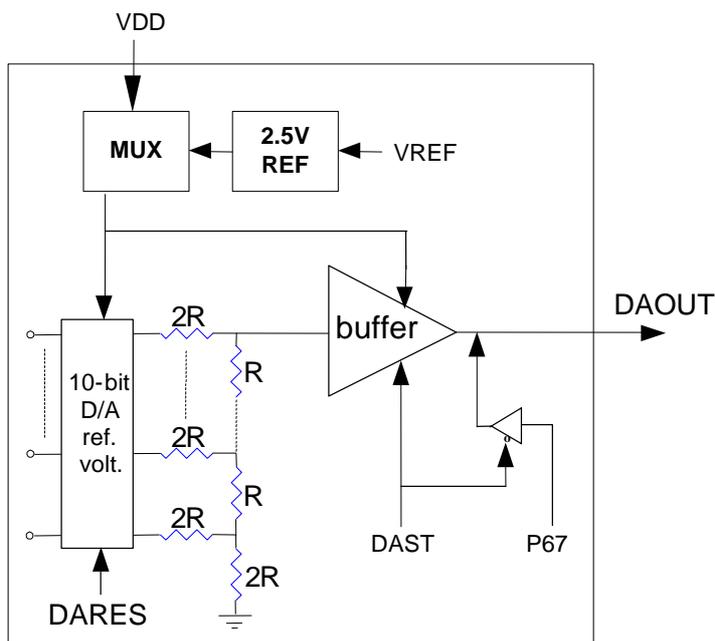


Figure 7-6 D/A Converter (DAC) Circuit Diagram

### 7.3.9 IOCB (Port B I/O Control, ADC Control)

#### ■ Page 0 (Port B I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
R/W-1							

**Bit 0 ~ Bit 7 (IOCB0 ~ IOCB7):** Port B I/O direction control register

**0:** Set the relative I/O pin as output

**1:** Set the relative I/O pin into high impedance

#### ■ Page 1 (ADC Control Bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN2	IN1	IN0	ADCLK1	ADCLK0	ADPWR	X	ADST
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	-	R/W-0

**Bit 0 (ADST):** AD converter start to sample  
By setting to "1," the AD will start to sample data. This bit is automatically cleared by hardware after a sampling.

**Bit 1:** Undefined. Do not use this bit.

**Bit 2 (ADPWR):** AD converter power control

**0:** Disable

**1:** Enable

**Bit 3 ~ Bit 4 (ADCLK0 ~ ADCLK1):** AD circuit sampling clock source

- For PLL Clock = 895.658kHz ~ 17.9 MHz (CLK2~CLK0 = 001 ~ 110)

ADCLK1	ADCLK0	Sampling Rate	Operation Voltage
0	0	74.6K	≥ 3.5V
0	1	37.4K	≥ 3.0V
1	0	18.7K	≥ 2.5V
1	1	9.3K	≥ 2.5V

- For PLL Clock = 447.829kHz (CLK2~CLK0 = 000)

ADCLK1	ADCLK0	Sampling Rate	Operation Voltage
0	0	37.4K	≥ 3.0V
0	1	18.7K	≥ 3.0V
1	0	9.3K	≥ 2.5V
1	1	4.7K	≥ 2.5V

This is a CMOS multi-channel 10-bit successive approximation A/D converter.

- **Features (74.6kHz Maximum Conversion Speed at 5V)**

- Adjusted full scale input
- External reference voltage input or internal (VDD) reference voltage
- 6 analog inputs multiplexed into one A/D converter
- Power down mode for power saving
- A/D conversion complete interrupt
- Interrupt register, A/D control & status register, and A/D data register

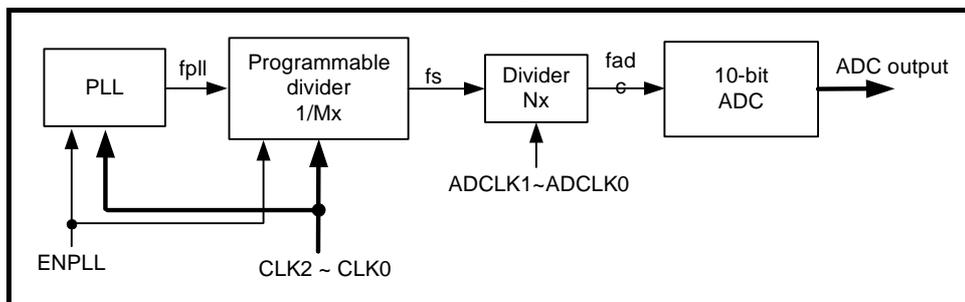


Figure 7-7a ADC Sampling Clock Control Logic

Fpll	Mx	Fs	Fadcon = fadc / 12			
			Nx = 1	Nx = 2	Nx = 4	Nx = 8
14.331MHz	16	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
10.747MHz	12	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
7.165MHz	8	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
3.582MHz	4	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
1.791MHz	2	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
895.658kHz	1	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
447.829kHz	1	447.829kHz	37.391kHz	18.659kHz	9.329kHz	4.665kHz

**Bit 5 ~ Bit 7 (IN0~ IN2):** AD converter Input channel select

These three bits can choose one of the three AD inputs.

IN2	IN1	IN0	Input
0	0	0	AD1
0	0	1	AD2
0	1	0	AD3
0	1	1	AD4
1	0	0	AD5
1	0	1	AD6

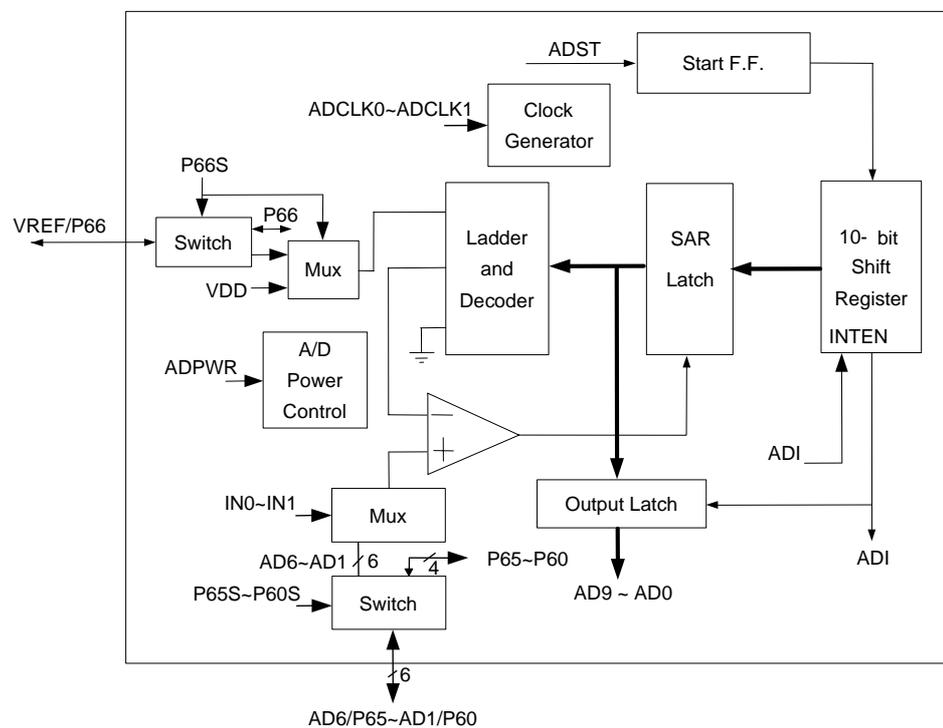


Figure 7-7b A/D Converter (ADC) with IOCC PAGE1 Bit 0 = 1 Setting

### 7.3.10 IOCC (Port C I/O Control)

#### ■ Page 0 (Port C I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCC7	IOCC6	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0
R/W-1							

**Bit 0 ~ Bit 7 (IOCC0 ~ IOCC7):** Port C I/O direction control register

**0:** Set the relative I/O pin as output

**1:** Set the relative I/O pin into high impedance

■ Page 1 (Port Switch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7S	PC6S	PC5S	PBSH	PBSL	P5SH	-	MS
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W/0

**Bit 0 (MS): P6\* Switch Mode Select**

**0:** (Default unknown)

**1:** ADC Input Mode Select

**NOTE**

*Always set this bit to "1." Otherwise, partial ADC function cannot be used.*

**Bit 1:** Unused. Not allowed for use.

**Bit 2 (P5SH):** Switch I/O Port 5 high nibble (5~7) or LCD segment signal

**0:** (P55 ~ P57 pins are selected) : normal Port 5 high nibble (5~7)

**1:** (SEG10 ~ SEG12 pins are selected) : Segment output

**Bit 3 (PBSL):** Switch I/O Port B low nibble (0~3) or LCD segment signal

**0:** (PB0 ~ PB3 pins are selected) : normal Port B low nibble (0~3)

**1:** (SEG28 ~ SEG25 pins are selected) : Segment output

**Bit 4 (PBSH):** Switch I/O Port B high nibble (4~7) or LCD segment signal

**Bit 5 (PC5S):** Switch I/O Port C5 or LCD segment signal

**0:** (PC5 pin is selected) : normal Port C5

**1:** (SEG31 pin is selected) : Segment output

**Bit 6 (PC6S):** Switch I/O Port C6 or LCD segment signal

**0:** (PC6 pin is selected) : normal Port C6

**1:** (SEG30 pin is selected) : Segment output

**Bit 7 (PC7S):** Switch I/O Port C7 or LCD segment signal

**0:** (PC7 pin is selected) : normal Port C7

**1:** (SEG29 pin is selected) : Segment output

### 7.3.11 IOCD (Clock Source, Prescaler of CN1 and CN2)

■ Page 0 (NOT defined. Do not use)

■ Page 1 (Clock Source and Prescaler for Counter 1 and Counter 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	C2_PSC2	C2_PSC1	C2_PSC0	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bit 0 ~ Bit 2 (C1\_PSC0 ~ C1\_PSC2): Counter 1 prescaler ratio**

C1_PSC2	C1_PSC1	C1_PSC0	Counter 1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

**Bit 3 (CNT1S): Counter 1 clock source**

0: 16.384kHz

1: System clock

**Bit 4 ~ Bit 6 (C2\_PSC0 ~ C2\_PSC2): Counter 2 prescaler ratio**

C2_PSC2	C2_PSC1	C2_PSC0	Counter 2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

**Bit 7 (CNT2S): Counter 2 clock source**

0: 16.384kHz

1: System clock

### 7.3.12 IOCE (Interrupt Mask)

#### ■ Page 0 (Interrupt Mask)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2	RBF	ADI	PWM1	-	-	-	-
R/W-0	R/W-0	R/W-0	R/W-0	-	-	-	-

**Bits 0 ~ 3: (NOT defined. Do not use)**

**Bit 4 (PWM1):** PWM1 interrupt enable bit

**0:** Disable interrupt

**1:** Enable interrupt

**Bit 5 (ADI):** ADC conversion complete interrupt mask

**0:** Disable interrupt

**1:** Enable interrupt

Four registers are provided for the A/D converter. Use 1-bit of Interrupt Control Register (IOCE Page 0 Bit 5) for A/D conversion complete interrupt. The status and control register of A/D (IOCB Page 1 and RE Page 0 Bit 5) responses to the A/D conversion status or takes control of A/D. The A/D Data Register (RB Page 1) stores the A/D conversion result.

ADI bit in IOCE Page 0 register is the end of A/D conversion complete interrupt enable/disable function. It enables/disables the ADI flag in RE register when A/D conversion is completed. The ADI flag indicates the end of an A/D conversion. The A/D converter sets the interrupt flag, ADI in RE Page 0 register when conversion is completed. The interrupt can be disabled by setting the ADI bit in IOCE Page 0 Bit 5 to "0."

The A/D converter has six analog input Channels AD1~AD6 multiplexed into one sample and held in A/D module. Reference voltage can be driven from VREF pin or internal power. The A/D converter itself is of a 10-bit successive approximation type and produces a 10-bit result in the RB Page 1 and R7 Page 1 data register. A conversion is initiated by setting a control bit ADST in IOCB Page 1 Bit 0. Prior to conversion, the appropriate channel must be selected by setting IN0~IN1 bits in RE register and allowed for enough time to sample data. Every conversion data of the A/D needs 12-clock cycle time. The required minimum conversion time is 13  $\mu$ s (74K sample rate). The ADST bit in IOCB Page 1 Bit 0 must be set to begin conversion.

It will be automatically reset by hardware when conversion is completed. At the end of conversion, the START bit is cleared and the A/D interrupt is activated if the ADI in IOCE PAGE 0 Bit 5 = 1. ADI will be set when conversion is completed. It can be reset by software.

If ADI = 0 in IOCE Page 0 Bit 5, when A/D starts conversion by setting ADST (IOCB Page 1 Bit 0) = 1, then A/D will continue conversion without stopping and the hardware won't reset the ADST bit. Under this condition, ADI is deactivated. After ADI in IOCE Page 0 Bit 5 is set, ADI in RE Page 0 Bit 5 will activate again.

For minimum operating current, all biasing circuits in the A/D module that consume DC current are powered down when ADPWR bit in IOCB Page 1 Bit 2 register is "0." When ADPWR bit is "1," the A/D converter module is in operation.

You need to set Port 60 and Port 65 as AD converter input pin or bidirectional I/O Port.

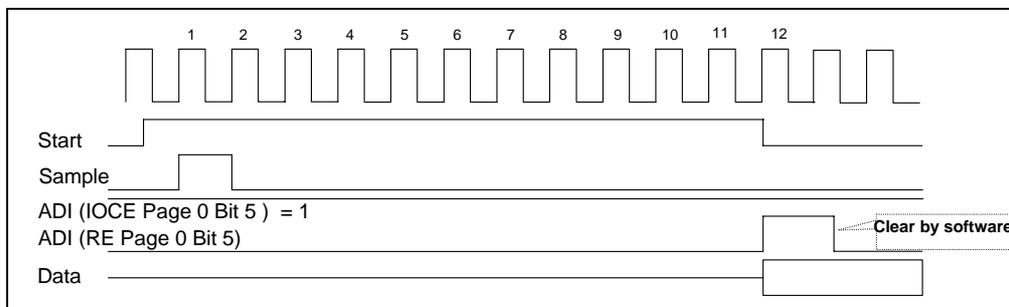


Figure 7-8 A/D Converter Timing Diagram

**Bit 6 (RBF):** SPI RBF interrupt mask

**0:** Disable interrupt

**1:** Enable interrupt

**Bit 7 (PWM2):** PWM2 interrupt enable bit

**0:** Disable interrupt

**1:** Enable interrupt

### 7.3.13 IOCF (Interrupt Mask)

#### ■ Interrupt Mask Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INT3	0	INT2	INT1	INT0	CNT2	CNT1	TCIF
R/W-0							

**Bits 0 ~ 5, 7:** Interrupt enable bit

**0:** Disable interrupt

**1:** Enable interrupt

**Bit 6:** ***(Keep these values to "0." Otherwise, it will generate unpredictable interrupts)***

The status after interrupt and the interrupt sources are listed below.

Interrupt Signal	Green Mode	Normal Mode
	RA (7,6)=(x,0) no SLEP	RA (7,6)=(x,1) no SLEP
TCC time out IOCF Bit 0=1 And "ENI"	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
Counter 1 time out IOCF Bit 1=1 And "ENI"	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
Counter 2 time out IOCF Bit 2=2 And "ENI"	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
Port 7 (0~3) IOCF Bit 3 or Bit 4 or Bit 5 =1 or Bit 7 =1 And "ENI"	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
RBF IOCE Bit 6 = 1 And "ENI"	Interrupt <ps> (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
ADI IOCE Bit 5 = 1 And "ENI"	No function	Interrupt (Jump to Address 8 at Page 0)
PWM1 IOCE Bit 4 = 1 And "ENI"	Interrupt <ps> (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
PWM2 IOCE Bit 7 = 1 And "ENI"	Interrupt <ps> (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)

**NOTE**

- The following conditions occur when master and 16.386kHz mode is selected:
- Port 70's interrupt function is controlled by IOCF Bit 3. It is a falling edge or rising edge triggered (controlled by CONT Register Bit 7).
  - Port 7 (1~3) Wake-up functions are controlled by IOCF Bits (4, 5, 7). They are falling edge triggered.
  - ADI interrupt source function is controlled by RE Page 0 Bit 5. It is a rising edge triggered after ADC sampling is completed.

### 7.4 I/O Port

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O data registers and I/O control registers are both readable and writable. The I/O interface circuits are illustrated in the following figures.

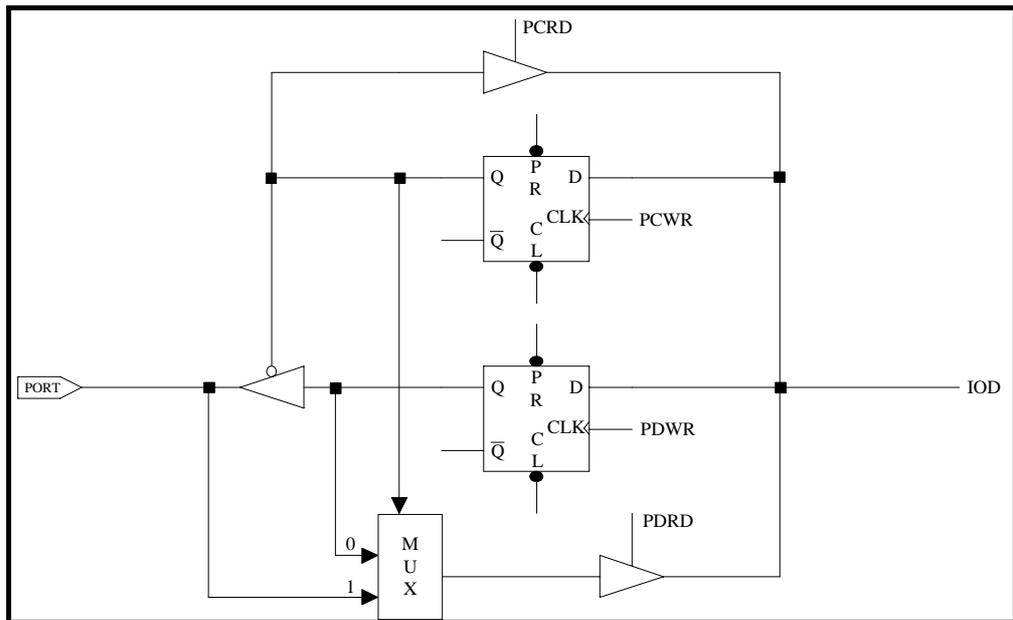


Figure 7-9a I/O Port and I/O Control Register Circuit Diagram

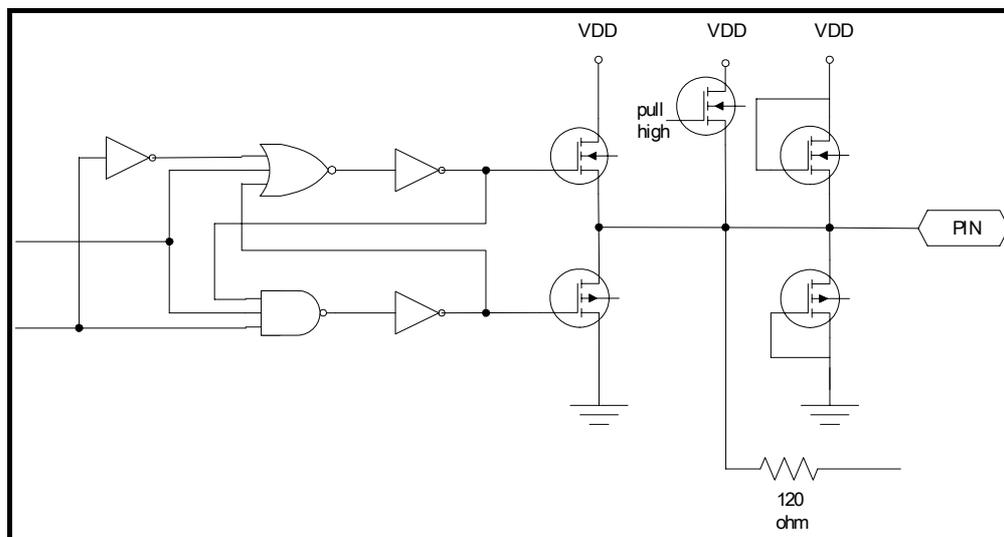


Figure 7-9b EM78P569A input/output Ports Input/Output Circuit Diagram

## 7.5 Reset

A Reset can be caused by:

- (1) Power-on reset
- (2) WDT timeout (if enabled and in Green or Normal mode)
- (3) /RESET pin pull low

Once a Reset occurs, the following functions are performed:

- The oscillator is running, or will be started
- The Program Counter (R2) is set to all "0"
- When in power-on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared
- The Watchdog timer and prescaler counter are cleared
- The Watchdog timer is disabled
- The CONT register is set to all "1"

- Other registers (Bit 7 ~ Bit 0) default values are as follows.

■ **Operation Registers**

Address	R Register Page 0	R Register Page 1	R Register Page 2	R Register Page 3	IOC Register Page 0	IOC Register Page 1
0x4	00xxxxxx					
0x5	xxxx0000	xxxx0000	00000000	00000000	111x0000	
0x6	xxxxxxxx	xxxxxxxx	xxxxxxxx	00000000	11111111	00000000
0x7	xxxxxxxx	xxxx0000		xxxxxx00	11111111	00000000
0x8	xxxxxxxx	00000000		00000000	11111111	00000000
0x9	xxxxxxxx	xxxxxxxx		00000000	11111111	00000000
0xA	00011xx0	11111111	0x000000	xxxxxx00	xxxxxxxx	<b>x0xx0xx</b>
0xB	xxxxxxxx	xxxxxxxx	xxxxxxxx	00000000	11111111	000000x0
0xC	xxxxxxxx	00000000	xxxxxxxx		11111111	00000000
0xD	xxxxx000	00000000	xxxxxxxx		xxxxxxxx	00000000
0xE	00000000		xxxxxxxx		0000xxxx	xxxxxxxx
0xF	00000000				00000000	

## 7.6 Wake-up

The controller provides Sleep mode for power conservation:

**Sleep mode, RA (7) = 0 + "SLEP" instruction**

The controller will turn off power to the CPU and crystal. You have to turn off the other circuits with power control, i.e., Keytone Control or PLL CONTROL (which has enabled/disable register) by software.

■ **Wake-up Triggers from Sleep mode**

- (1) WDT time out
- (2) External interrupt
- (3) /RESET pull-low

All these cases will reset the controller and run the program at Address 0. The status is just like the power-on reset.

## 7.7 Interrupt

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it causes the next instruction to be fetched from Address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register.

The interrupt flag bit must be cleared by software before leaving the interrupt service routine and before enabling interrupts to avoid recursive interrupts.

## 7.8 Instruction Set

The Instruction Set has the following features:

- (1) Every bit of any register can be set, cleared, or tested directly.
- (2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

### ■ Instruction Set Convention:

**R** = Register designator that specifies which one of the 64 registers (including operation and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank.

**b** = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

**k** = 8 or 10-bit constant or literal value

Binary Instruction	HEX	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 Bits 9,10 do not clear	Z,C,DC	2
<b>0 0000 0011 0000</b>	<b>0030</b>	<b>INT A</b>	<b>(MR)(+/-)(s/us X)*(s/us Y)→MR</b>	<b>None</b>	<b>1</b>

(Continuation)

Binary Instruction	HEX	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0000 01rr rrrr	00rr	MOV R,A	$A \rightarrow R$	None	1
0 0000 1000 0000	0080	CLRA	$0 \rightarrow A$	Z	1
0 0000 11rr rrrr	00rr	CLR R	$0 \rightarrow R$	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	$R-A \rightarrow A$	Z, C, DC	1
0 0001 01rr rrrr	01rr	SUB R,A	$R-A \rightarrow R$	Z, C, DC	1
0 0001 10rr rrrr	01rr	DECA R	$R-1 \rightarrow A$	Z	1
0 0001 11rr rrrr	01rr	DEC R	$R-1 \rightarrow R$	Z	1
0 0010 00rr rrrr	02rr	OR A,R	$A \vee R \rightarrow A$	Z	1
0 0010 01rr rrrr	02rr	OR R,A	$A \vee R \rightarrow R$	Z	1
0 0010 10rr rrrr	02rr	AND A,R	$A \& R \rightarrow A$	Z	1
0 0010 11rr rrrr	02rr	AND R,A	$A \& R \rightarrow R$	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	$A \oplus R \rightarrow A$	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	$A \oplus R \rightarrow R$	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	$A + R \rightarrow A$	Z, C, DC	1
0 0011 11rr rrrr	03rr	ADD R,A	$A + R \rightarrow R$	Z, C, DC	1
0 0100 00rr rrrr	04rr	MOV A,R	$R \rightarrow A$	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	$R \rightarrow R$	Z	1
0 0100 10rr rrrr	04rr	COMA R	$/R \rightarrow A$	Z	1
0 0100 11rr rrrr	04rr	COM R	$/R \rightarrow R$	Z	1
0 0101 00rr rrrr	05rr	INCA R	$R+1 \rightarrow A$	Z	1
0 0101 01rr rrrr	05rr	INC R	$R+1 \rightarrow R$	Z	1
0 0101 10rr rrrr	05rr	DJZA R	$R-1 \rightarrow A$ , skip if zero	None	2 if skip
0 0101 11rr rrrr	05rr	DJZ R	$R-1 \rightarrow R$ , skip if zero	None	2 if skip
0 0110 00rr rrrr	06rr	RRCA R	$R(n) \rightarrow A(n-1)$ $R(0) \rightarrow C, C \rightarrow A(7)$	C	1
0 0110 01rr rrrr	06rr	RRC R	$R(n) \rightarrow R(n-1)$ $R(0) \rightarrow C, C \rightarrow R(7)$	C	1
0 0110 10rr rrrr	06rr	RLCA R	$R(n) \rightarrow A(n+1)$ $R(7) \rightarrow C, C \rightarrow A(0)$	C	1
0 0110 11rr rrrr	06rr	RLC R	$R(n) \rightarrow R(n+1)$ $R(7) \rightarrow C, C \rightarrow R(0)$	C	1
0 0111 00rr rrrr	07rr	SWAPA R	$R(0-3) \rightarrow A(4-7)$ $R(4-7) \rightarrow A(0-3)$	None	1
0 0111 01rr rrrr	07rr	SWAP R	$R(0-3) \leftrightarrow R(4-7)$	None	1
0 0111 10rr rrrr	07rr	JZA R	$R+1 \rightarrow A$ , skip if zero	None	2 if skip
0 0111 11rr rrrr	07rr	JZ R	$R+1 \rightarrow R$ , skip if zero	None	2 if skip
0 100b brrr rrrr	0xxx	BC R,b	$0 \rightarrow R(b)$	None	1
0 101b brrr rrrr	0xxx	BS R,b	$1 \rightarrow R(b)$	None	1
0 110b brrr rrrr	0xxx	JBC R,b	if $R(b)=0$ , skip	None	2 if skip
0 111b brrr rrrr	0xxx	JBS R,b	if $R(b)=1$ , skip	None	2 if skip

(Continuation)

Binary Instruction	HEX	Mnemonic	Operation	Status Affected	Instruction Cycle
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None	1
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z	1
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC	1
1 1110 0000 0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1 1110 100k kkkk	1E8k	PAGE k	K → R5(4:0)	None	1
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC	1

**NOTE**

- For ADD and SUB instruction execution, refer to RA Page 2 Bit 7 (Section 7.2.11).
- Instruction cycle = 2 main CLK.

## 7.9 Code Option

### ■ Code Option Register

Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PHO	VERSEL	1		-				0			/POT0

**Bit 0 (/POT0):** Program ROM protect option  
If the bit is set to “1,” the program memory can be accessed; else if this bit is cleared, the program memory cannot be accessed.

**Bit 3:** Always clear this bit to “0”

**Bit 9:** This bit must be set to “1”

**Bit 10 (VERSEL):** Version select.

Function	VERSEL = 0	VERSEL = 1
Data RAM address	R8 Page 1	RB Page 2
Data RAM address auto-increase	Not supported	Enable
“ADD” & “SUB” include “carry” bit	Not supported	Determined by RA Page 2 Bit 7

**Bit 11 (PHO):** Port C0 status select.

**0:** Port C0 defined as normal I/O

**1:** Port C0 defined as Phase 1 output

The following figure shows the relation between main CLK and Phase 1 CLK.

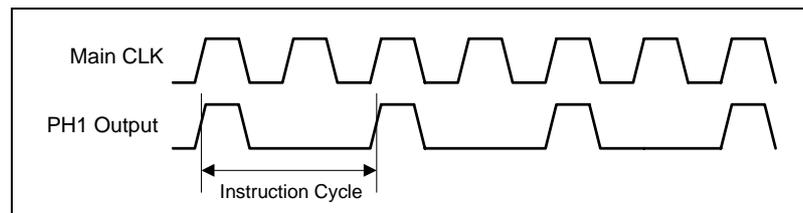


Figure 7-10 Correlation between Main CLK and PH1 Output

## 7.10 Dual Sets of PWM (Pulse Width Modulation)

### 7.10.1 Overview

In PWM mode, both PWM1 and PWM2 pins generate up to 10-bit resolution PWM output (see following figure for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the period. Figure 7-11b depicts the relationships between a period and a duty cycle.

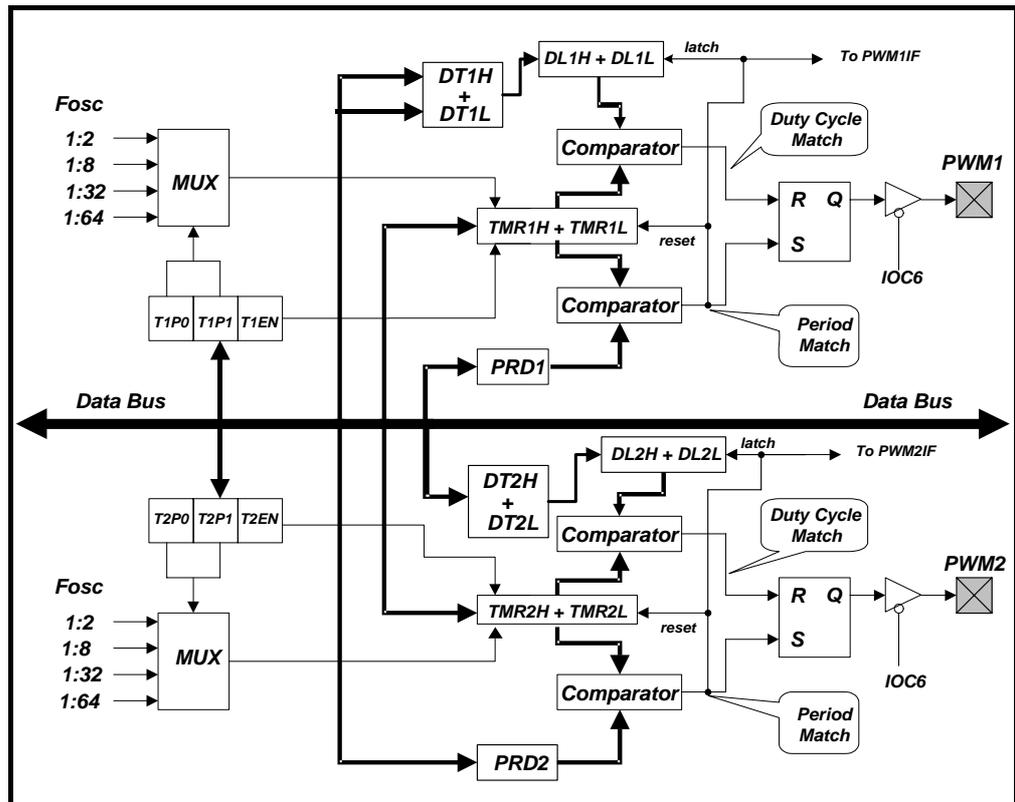


Figure 7-11a Dual PWMs Functional Block Diagram

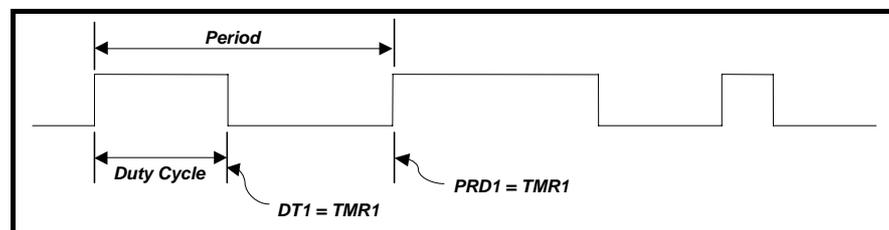


Figure 7-11b PWM Output Timing

### 7.10.2 Increment Timer Counter (TMRX: TMR1H/TWR1L or TMR2H/TWR2L)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written, and cleared at any reset conditions. If employed, they can be turned down for power saving mode by setting T1EN bit [PWMCON<4>] or T2EN bit [PWMCON<5>] to “0.”

### 7.10.3 PWM Period (PRDX: PRD1 or PRD2)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared.
- The PWMX pin is set to “1.”
- The PWM duty cycle is latched from DT1/DT2 to DTL1/DTL2.

**NOTE**

*The PWM output will not be set if the duty cycle is “0.”*

- The PWMXIF pin is set to “1.”

The PWM period is calculated using the following formula:

$$Period = (PRDX + 1) \times 4 \times \left( \frac{1}{F_{osc}} \right) \times (TMRX \text{ prescale value})$$

where  $F_{osc}$  is the system clock

### 7.10.4 PWM Duty Cycle (DTX: DT1H/ DT1L and DT2H/ DT2L; DTL: DL1H/DL1L and DL2H/DL2L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DTL until the current value of DLX is equal to TMRX.

The PWM duty cycle is calculated using the following formula:

$$Duty \ Cycle = (DTX) \times \left( \frac{1}{F_{osc}} \right) \times (TMRX \text{ prescale value})$$

### 7.10.5 Comparator X

Changing the output status while a match occurs, the TMRXIF flag will be set at the same time.

### 7.10.6 PWM Programming Procedures/Steps

Load PRDX with the PWM period.

- Load DTX with the PWM Duty Cycle.
- Enable the interrupt function by writing IOCF PAFE0, if required.
- Set PWMX pin to be output by writing a desired value to IOCC Page 0.
- Load a desired value to R5 PAGE3 with TMRX prescaler value and enable both PWMX and TMRX.

### 7.10.7 Timer

Timer 1 (TMR1) and Timer 2 (TMR2) (TMRX) are both 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written, and cleared at any reset conditions.

Figure below shows the TMRX block diagram.

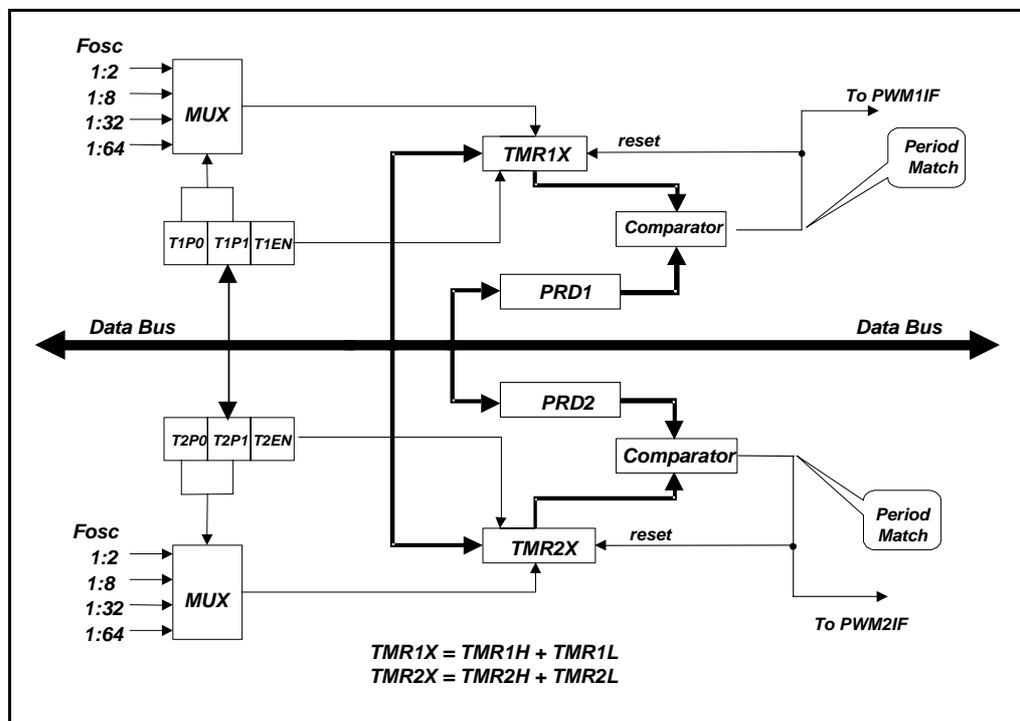


Figure 7-12 TMRX Block Diagram

The description of each signal and block are as follows:

**Fosc:** Input clock.

**Prescaler (T1P0 and T1P1/T2P1 and T2P0):** Options of 1:2, 1:8, 1:32, and 1:64 are defined by TMRX. It is cleared when any type of reset occurs.

**TMR1X and TMR2X (TMR1H/TWR1L and TMR2H/TMR2L):** Timer X register; TMRX is increased until it matches with PRDX, and then is reset to "0." TMRX cannot be read.

**PRDX (PRD1 and PRD2):** PWM period register.

**Comparator X (Comparator 1 and Comparator 2):** This resets the TMRX while a match occurs and the TMRXIF flag is set at the same time.

When defining TMRX, refer to the operation of its related registers as shown in the prescale register. It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, Bit 7 and Bit 6 of the PWMCON register must be set to “0.”

■ **Related Control Registers (R5 Page 3) of TMR1 and TMR2**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

Timer programming procedures/steps:

- Load PRDX with the TIMER period.
- Enable the interrupt function by writing IOCF Page 0, if required.
- Load a desired value to PWMCON with the TMRX prescaler value and enable both TMRX and disable PWMX.

## 8 Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.3 to 6	V
Input Voltage	Vin	-0.5 to VDD +0.5	V
Operating Temperature Range	Ta	0 to 70	°C

## 9 DC Electrical Characteristics

■ Ta = 25°C, AVDD=VDD=5V ± 5%, VSS=0V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current for input pins	IIL1	VIN = VDD, VSS	-	-	±1	μA
Input leakage current for bidirectional pins	IIL2	VIN = VDD, VSS	-	-	±1	μA
Input high voltage	VIH	-	2.5	-	-	V
Input low voltage	VIL	-	-	-	0.8	V
Input high threshold voltage	VIHT	/RESET, TCC	2.0	-	-	V
Input low threshold voltage	VILT	/RESET, TCC	-	-	0.8	V
Clock input high voltage	VIHX	OSCI	3.5	-	-	V
Clock input low voltage	VILX	OSCI	-	-	1.5	V
Output high voltage for Port 5, B, C	VOH1	IOH = -6 mA	2.4	-	-	V
Output high voltage for Ports 6, 8	VOH2	IOH = -10 mA	2.4	-	-	V
Output high voltage for Ports 7, 9	VOH3	IOH = -20 mA	2.4	-	-	V
Output low voltage for Ports 5, B, C	VOL1	IOH = 6 mA	-	-	0.4	V
Output low voltage for Ports 6, 8	VOL2	IOH = 10 mA	-	-	0.4	V

(Continuation)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output low voltage for Ports 7, 9	VOL3	IOH = 20mA	-	-	0.4	V
LCD drive reference voltage	VLCD	VDD=5V, Contrast adjust	-	4 ~ 5	-	V
Data RAM retention voltage	VDR	-	-	-	1.2	V
Pull-high current	IPH	Pull-high active input pin at VSS	-	-10	-15	μA
Power down current (Sleep mode)	ISB1	All input and I/O pin at VDD, Output pin floating, WDT disabled	-	4	8	μA
Low clock current (Green mode)	ISB2	CLK=32.768kHz, All analog circuits disabled, All input and I/O pin at VDD, Output pin floating, WDT disabled, LCD enabled	-	35	50	μA
Operating supply current (Normal mode)	ICC1	/RESET=High, CLK=3.582 MHz, All analog circuits disabled, Output pin floating	-	1	2	mA

## 10 AC Electrical Characteristics

### ■ CPU Instruction Timing (Ta = 25°C, AVDD=VDD=5V, VSS=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk	-	45	50	55	%
Instruction cycle time	Tins	32.768kHz	-	60	-	μs
		3.582 MHz	-	550	-	ns
Device delay hold time	Tdrh	-	-	16	-	ms
TCC input period	Ttcc	-	(Tins+20)/N*	-	-	ns
Watchdog timer period	Twdt	Ta = 25°C	-	16	-	ms
DAC output delay	Tda	-	-	50	-	μs

\* N = Selected prescaler ratio

### ■ ADC Characteristic (VDD = 5V, Ta = +25°C, for Internal Reference Voltage)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Upper bound offset voltage	Vofh	-	-	44	52.8	mV
Lower bound offset voltage	Vofl	-	-	32	38.4	mV

NOTE: These parameters are theoretical values only and have not been tested.

For ADC characteristics, refer to the following page.

■ **Timing Characteristic (AVDD=VDD=5V, Ta=+25°C)**

Description		Symbol	Min	Typ	Max	Unit
<b>Oscillator Timing Characteristic</b>						
OSC start up	32.768kHz	Tosc	400	–	1500	ms
	3.579 MHz PLL	–	–	5	10	µs
<b>SPI Timing Characteristic (CPU Clock 3.58 MHz and Fosc = 3.58 MHz / 2)</b>						
/SS set-up time		Tcss	560	–	–	ns
/SS hold time		Tcsh	250	–	–	–
SCLK high time		Thi	250	–	–	ns
SCLK low time		Tlo	250	–	–	ns
SCLK rising time		Tr	–	15	30	ns
SCLK falling time		Tf	–	15	30	ns
SDI set-up time to the reading edge of SCLK		Tisu	25	–	–	ns
SDI hold time to the reading edge of SCLK		Tihd	25	–	–	ns
SDO disable time		Tdis	–	–	560	ns
<b>Reset Timing Characteristic</b>						
Minimum width of reset low pulse		Trst	3	–	–	µs
Delay between reset and program start		Tdrs	–	18	–	ms

■ **Embedded LCD Driver**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ron	LCD driver ON resistance	LCD function enabled	–	2	4	KΩ
Frame	LCD frame frequency	1/2 , 1/4 duty	–	64	–	Hz

■ **OSC Stable Time vs. Power-on Reset Correlation**

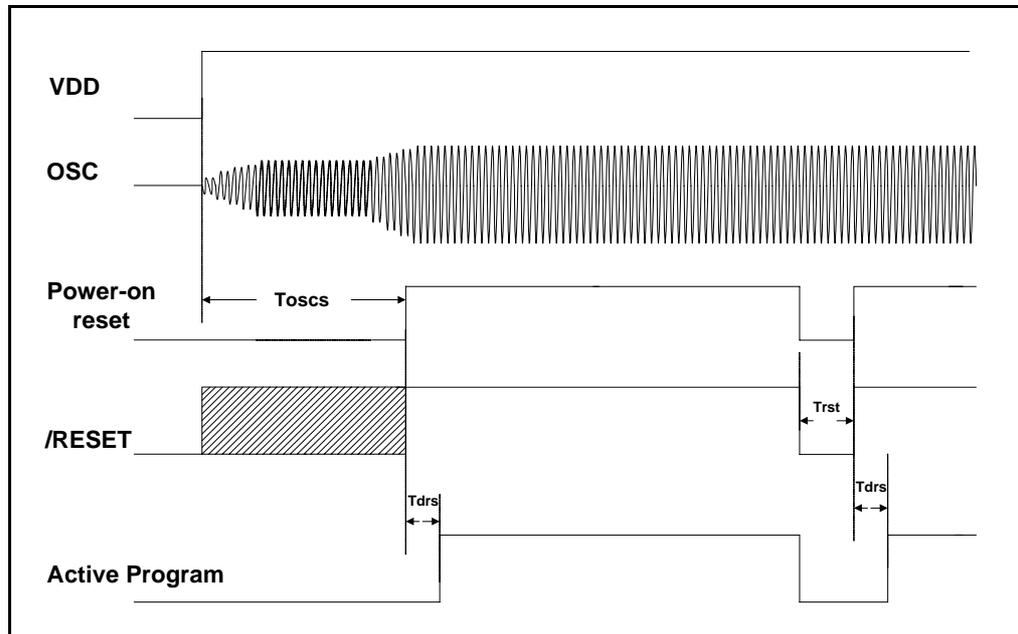
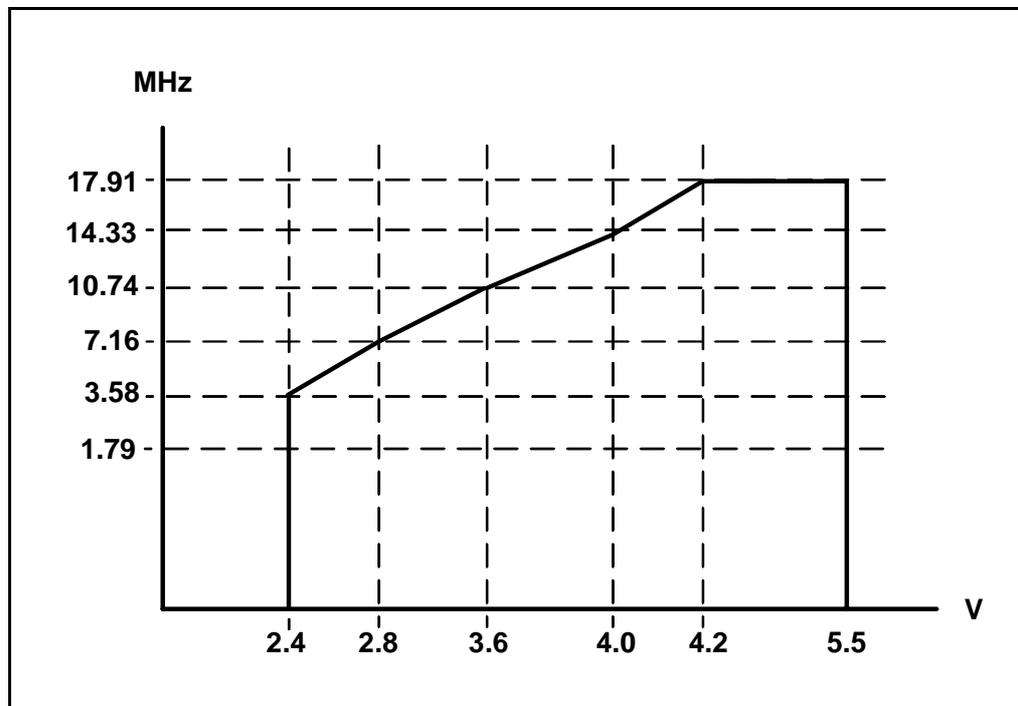


Figure 10-1a Correlation between OSC Stable Time and Power-on Reset

■ **Operating Voltage vs. Main CLK Correlation**



NOTE: EM78P569A Operation Voltage (X axis → min VDD; Y axis → main CLK).

Figure 10-1b Relationship between Operating Voltage and the Main CLK

■ EM78569 10-bit ADC Characteristic

The EM78569 has a built-in 10-bit resolution, multi-channel ADC function. Ideally, if the ADC’s reference voltage is 5V, the ADC’s LSB will be 5V/1024. But actually, for some inherent or circuit’s character, some undesirable conditions will affect the converter result. As shown in the next figure, the offset voltage will reduce the AD’s converter range. If the AD’s input voltage is less than VOFL, ADC will output “0.” However, if the input voltage is larger than (VDD – VOFH), ADC will output “1023.” In other words, the physical AD converter range will be replaced by (VDD – VOFH+LSB – VOFL+LSB). If we defined VRB = VOFL – LSB and VRT = VDD – VOFH+LSB, the physical LSB is:

$$LSB = (VRT - VRB) / 1024$$

$$LSB = \{VDD - (VOFH+VOFL)\} / 1022$$

In actual operation, user should consider the effect of the AD’s offset voltage. If the converter range is (VRT – VRB), the AD converter’s opposite result will be more precise.

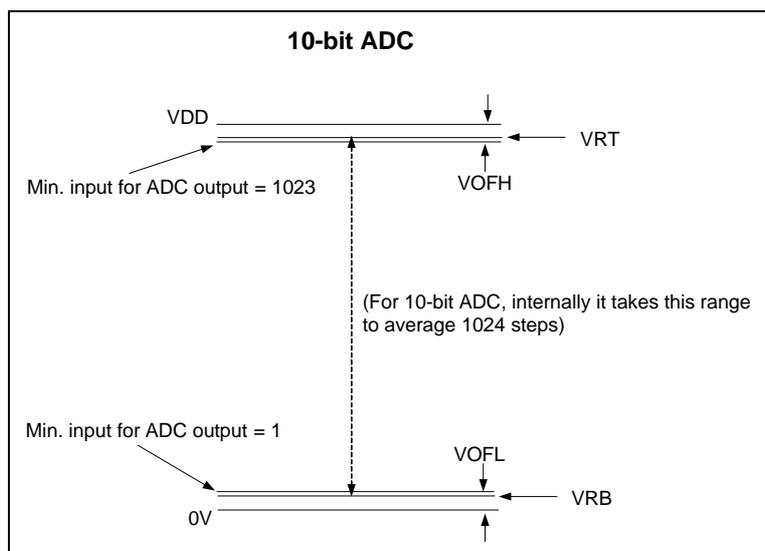
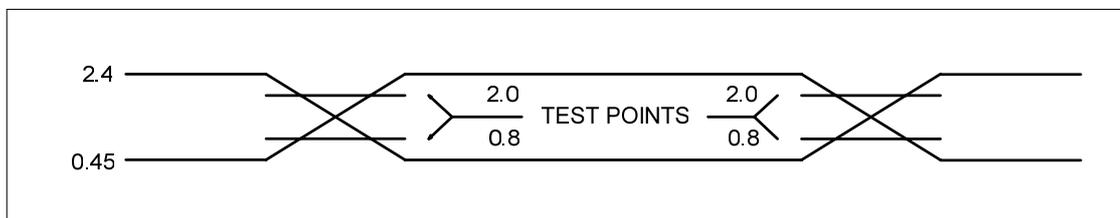


Figure 10-1c Relationship between ADC and Offset Voltage

## 11 Timing Diagrams

### ■ AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1" and 0.45V for logic "0".

Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

Figure 11-1a AC Test Timing Diagram

### ■ Reset Timing (CLK = "0")

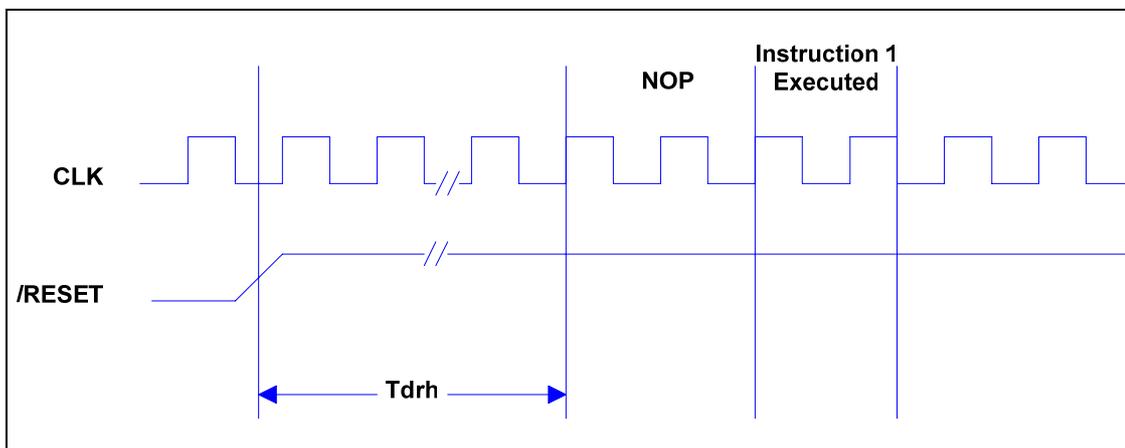


Figure 11-1b Reset Timing Diagram

### ■ TCC Input Timing (CLKS = "0")

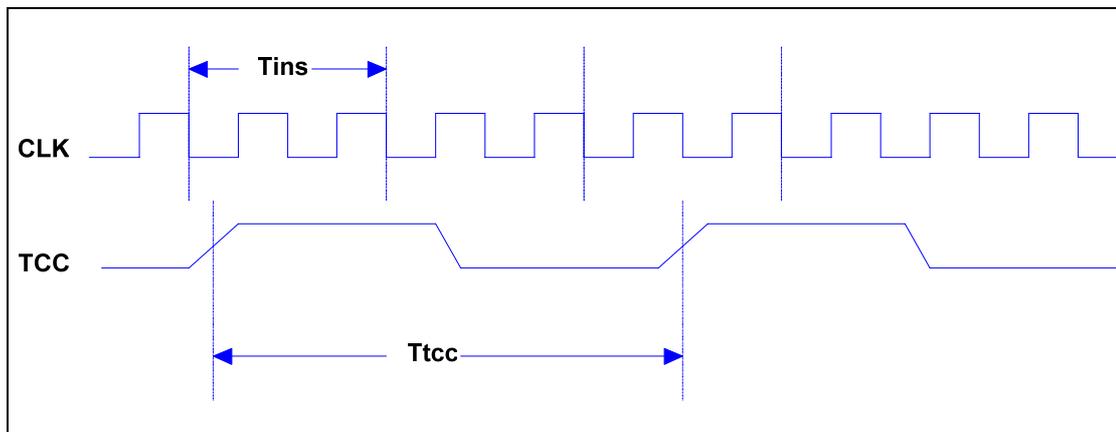


Figure 11-1c TCC Input Timing Diagram

## APPENDIX

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### A Function Control List

#### ■ ADC

- ADRES → R7 Page 1 Bit 2
- AD8~AD9 → R7 Page 1 Bit 4~Bit 5
- AD0~AD7 → RB Page 1
- AD/IO pin select → IOC6 Page 1 Bit 0~Bit 6
- AD power control → IOCB Page 1

#### ■ DAC

- DA8~DA9 → R5 Page 1 Bit 6~Bit 7
- DARES → R7 Page 1 Bit 3
- DA0~DA7 → RA Page 1 Bit 0~Bit 7
- DAST → IOCA Page 1 Bit 3
- DAREF → IOCA Page 1 Bit 6

#### ■ SPI

- SPI control → R5 Page 2
- SPI data → R6 Page 2

#### ■ LCD Driver

- LCD address → R5 Page 1 Bits 0~3
- LCD data → R6 Page 1
- LCD mode select → RD Page 0 Bits 0~Bit 2
- LCD bias → IOC5 Page 0 Bit 0~Bit 3
- LCD IO/seg pin select → IOC9 Page 1, IOCC Page 1

**■ PWM**

- PWM control → R5 Page 3
- PWM1 duty control Bit 0~Bit 7 → R6 Page 3
- PWM1 duty control Bit 8~Bit 9 → R7 Page 3 Bit 0~Bit 1
- PWM1 period control → R8 Page 3
- PWM2 duty control Bit 0~Bit 7 → R9 Page 3
- PWM2 duty control Bit 8~Bit 9 → RA Page 3 Bit 0~Bit 1
- PWM1 period control → RB Page 3

**■ Data RAM access**

*VERSEL = 0:*

- RAM bank → R7 Page 1 Bit 0~Bit 1
- RAM address → R8 Page 1
- RAM data → R9 Page 1

*VERSEL = 1:*

- RAM bank → R7 Page 1 Bit 0~Bit 1
- RAM address → RB Page 2
- RAM data → R9 Page 1

**■ Multiplier\***

- Multiplier control → RA Page 2
- Multiplication X → ACC
- Multiplication Y → RB Page 2
- Multiplication Result 0~7 → RC Page 2
- Multiplication Result 8~15 → RD Page 2
- Multiplication Result 16~23 → RE Page 2

\* Multiplier instruction is "INT A"

## B User Application Notes

### IMPORTANT!!

Before using the chip, please take a look at the following important notes to better understand the contents of this specification and ensure smooth operation of your application.

1. There are some undefined bits in the registers. The values in these bits are undetermined. These bits are not intended for user utilization and are represented by a hyphen ( - ) in their respective table in this specification or as shown in the sample table (Bit 3) below.
2. A number of the frequently used names to define the register bits (such as bit type, bit name, bit number, etc.) in this specification are shown below with its intended meanings:

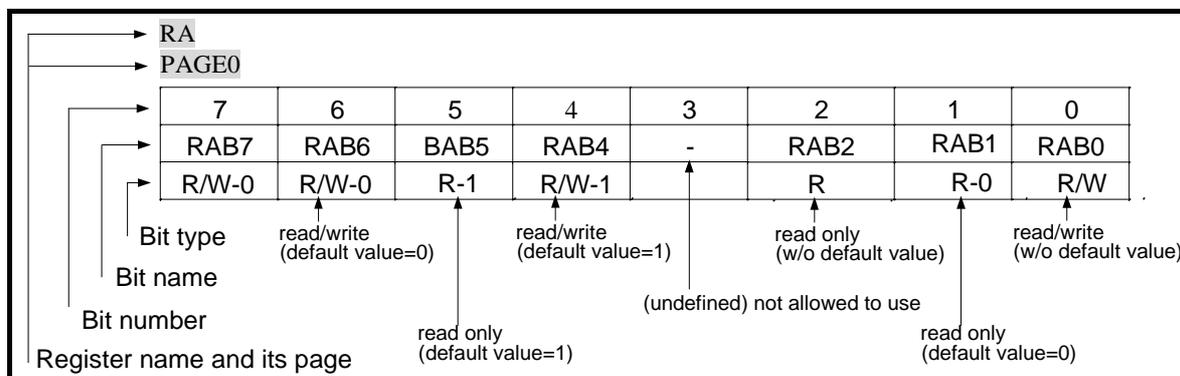


Figure B-1 Definitions of the Frequently Used Register Bit Names

3. Always set IOCC PAGE1 Bit 1 = 1. Otherwise, partial ADC function cannot be used.
4. For 8 bits resolution DAC, DAO pin will output a corresponding voltage after writing a new data to DAC data buffer (RA Page 1). For 10 bits resolution, DAO pin will initially output a constant voltage after a change at DAC most significant 2 bits (R5 Page 1 Bits 6~7). DAO will then output the correct voltage after writing data to the least significant 8 bits. In other words, **when using 10 bits resolution DAC, you must write the most significant 2 bits first, and followed by the least significant 8 bits, in such order.**
5. Base on "VERSEL" (code option) equal "0" or "1," the R8 Page 1 and RB Page 2 definitions are different, that is:
  - "VERSEL" = 0 R8 Page 1 is defined to data RAM address buffer  
RB Page 2 is defined to Multiplier Y data or Y address buffer (controlled by RA Page 2 Bit 5 "INDR").  
RA Page 2 Bit 4 (PLUS) determines whether the RAM address will auto increase or not (only for multiplier's addressing).  
RA Page 2 Bit 7 is undefined.

- “VERSEL” = 1: R8 Page 1 is undefined.

RA Page 2 Bit 4 (PLUS) determines whether the RAM address will auto increase or not (for data RAM and multiplier addressing).

RA Page 2 Bit 7 (INS) determine whether the RAM address will auto increase or not (for data RAM and multiplier addressing).

RB Page 2 is defined to Multiplier Y data, Y address, or data RAM address buffer.

6. The carry bit’s initial value is unknown. Define the initial value first before executing ADD or SUB instruction that includes the carry bit (VERSEL =1 and INS = 1)
7. In EM78569’s developing tool, “VERSEL” and “PHO” are at RD Page 2 Bit 6 and Bit 5. But in mask chip, these two bits are mapped to the code option. Set these two bits to a fixed value initially and do not change the two bits value in your program.

The differences between ICE569, EM78P569A, and EM78569

	ICE569	EM78P569A	EM78569
Stack Level	16	16	12

8. Use Counter 1 and Counter 2 when the MCU alternately runs between sub-frequency and main frequency. The alternating time difference should be longer than 200 ms between sub-frequency and main frequency. Too short alternating time difference will result to inaccurate interrupt timing on Counter 1 and Counter 2.

