
EM78P159/154N

**8-Bit Microcontroller
with OTP ROM**

Product Specification


DOC. VERSION 1.7

ELAN MICROELECTRONICS CORP.

April 2016

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**ELAN MICROELECTRONICS CORPORATION****Headquarters:**

No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
<http://www.emc.com.tw>

Hong Kong:

Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre 95
How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA:

Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Shenzhen:

Elan Microelectronics Shenzhen, Ltd.
8A Floor, Microprofit Building
Gaoxin South Road 6
Shenzhen Hi-tech Industrial Park
South Area, Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:

ELAN Microelectronics Shanghai, Ltd.
6F, Ke Yuan Building
No. 5 Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA 201203
Tel: +86 21 5080-3866
Fax: +86 21 5080-0273
elan-sh@elanic.com.cn

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Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial Release Version	2006/05/16
1.1	Modified the Reliability Test and green product	2007/01/10
1.2	Added EM78P155N package type	2007/03/29
1.3	Added 14-pin and 16-pin types into the series	2007/06/26
1.4	Added Appendix D	2007/07/06
1.5	<ol style="list-style-type: none"> 1. Modified the EM78P155NKM to EM78P132SS10J 2. Added the characteristics at 125°C 3. Modified the table of characteristics at 25°C 4. Modified the code option 5. Modified Figure5-1 	2007/12/27
1.6	<ol style="list-style-type: none"> 1. Deleted the following package types: 10-pin SSOP : M78P132SS10J/S 14-pin DIP: EM78P154NPS 14-pin SOP: EM78P154NMS 16-pin SOP: EM78P1541NAMJ/S 18-pin DIP: EM78P159NPS 18-pin SOP: EM78P159NMS 20-pin SSOP: EM78P159NASJ/S 20-pin SSOP: EM78P159NKMJ 	2011/10/04
1.7	<ol style="list-style-type: none"> 1. Modified the package type in the Features section 2. Modified Appendix A “Ordering and Manufacturing Information” 	2016/04/26



1 General Description

The EM78P159/154N are 8-bit microprocessors designed and developed with low-power, high-speed CMOS technology. The series have on-chip 1K×13-bits Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides three Protection bits to prevent intrusion of user's code in the OTP memory as well as from unwanted external accesses. Eight option bits are also available to meet user's application requirements.

With its enhanced OTP-ROM features, the EM78P159/154N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU Configuration
 - 1K×13 bits on-chip ROM
 - 48×8 bits on chip registers (SRAM, general purpose registers)
 - 5-level stacks for subroutine nesting
 - Less than 2.0 mA at 5V/4MHz
 - Typically 20 μ A, at 3V/32kHz
 - Typically 1 μ A, during sleep mode
- I/O port configuration
 - 2 bidirectional I/O ports
 - 8 Programmable pull-high I/O pins
 - 8 programmable pull-down I/O pins
 - 8 programmable open-drain I/O pins
 - 2 programmable R-option pins
- Operating voltage range:
 - 2.1V~5.5V at 0°C~70°C
 - 2.3V~5.5V at -40°C~125°C
- Operating frequency range (base on 2 clocks):
 - Crystal mode: DC~20MHz @ 5V, DC~8MHz @ 3V, DC~4MHz @ 2.1V
 - ERC mode: DC~20MHz @ 5V, DC~8MHz @ 3V, DC~4MHz @ 2.1V
 - IRC mode:
 - Oscillation mode : 4MHz, 8MHz, 1MHz, 455kHz
 - Process deviation : Typ. \pm 3%, Max \pm 5%
 - Temperature deviation : -5~8.5% (-40°C~125°C)
 - Frequency deviation : \pm 4% after auto trimming (based on Vdd = 5V, Ta = 25°C)
 - All the four main frequencies can be trimmed by programming with four calibrated bits in the ICE159N Simulator. OTP is auto trimmed by ELAN Writer (DWTR)
- Fast set-up time requires only 2ms in high Crystal and 32 CLKS in IRC mode from wake up to operating mode
- Peripheral configuration
 - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
- One security register to prevent intrusion of OTP memory codes
- One configuration register to accommodate user's requirements
- Two clocks per instruction cycle
- Power down (Sleep) mode
- Three available interrupts:
 - TCC overflow interrupt
 - Input-port status changed interrupt (wake-up from sleep mode)
 - External interrupt
- Special feature
 - Programmable free running watchdog timer
- Single instruction cycle commands
- Transient point of system frequency between HXT and LXT is 400kHz
- Package types:
 - 14-pin DIP 300mil : EM78P154NP
 - 14-pin SOP 150mil : EM78P154NM
 - 18-pin DIP 300mil : EM78P159NP
 - 18-pin SOP 300mil : EM78P159NM

3 Pin Assignment

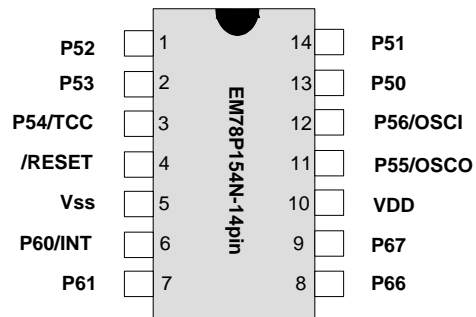


Figure 3-1 EM78P154NP/M Pin Assignment

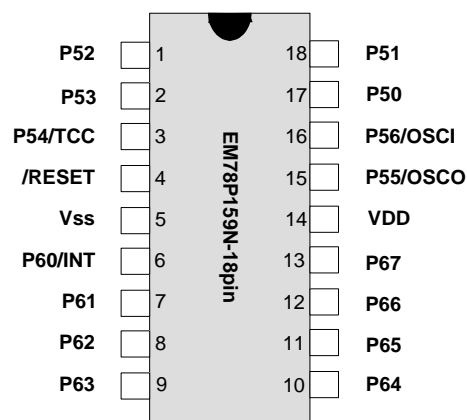


Figure 3-2 EM78P159NP/M Pin Assignment

4 Pin Description

4.1 EM78P159NP/M

Symbol	Pin No.	Type	Function
VDD	14	-	Power supply
P56/OSCI	16	I/O	General-purpose I/O pin Crystal type: Crystal input terminal or external clock input pin ERC type: RC oscillator input pin
P55/OSCO	15	I/O	General-purpose I/O pin Crystal type: Output terminal for crystal OSC or external clock input pin RC type: Instruction clock output External clock signal input
P54/TCC	3	I/O	General-purpose I/O pin Real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	4	I	Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50 ~ P53	17, 18, 1, 2	I/O	P50 ~ P53 are bidirectional I/O pins, can also be pulled-down by software P50 and P51 can also be defined as R-option pins
P60 ~ P67	6 ~ 13	I/O	P60 ~ P67 are bi-directional I/O pins. These can be pulled-high or can be open-drain by software programming P60 ~ P63 can also be pulled-down by software
/INT	6	I	External interrupt pin triggered by a falling edge
VSS	5	-	Ground

4.2 EM78P154NP and EM78P154NM

Symbol	Pin No.	Type	Function
VDD	10	-	Power supply
P56/OSCI	12	I/O	General-purpose I/O pin Crystal type: Crystal input terminal or external clock input pin ERC type: RC oscillator input pin
P55/OSCO	11	I/O	General-purpose I/O pin Crystal type: Output terminal for crystal oscillator or external clock input pin RC type: Instruction clock output External clock signal input
P54/TCC	3	I/O	General-purpose I/O pin Real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	4	I	Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50 ~ P53	13, 14, 1, 2	I/O	P50 ~ P53 are bidirectional I/O pins, can also be pulled-down by software P50 and P51 can also be defined as R-option pins
P60, P61 P66, P67	6, 7 8, 9	I/O	P60 ~ P67 are bi-directional I/O pins. These can be pulled-high or can be open-drain by software programming P60 ~ P61 can also be pulled-down by software
/INT	6	I	External interrupt pin triggered by a falling edge
VSS	5	-	Ground

5 Block Diagram

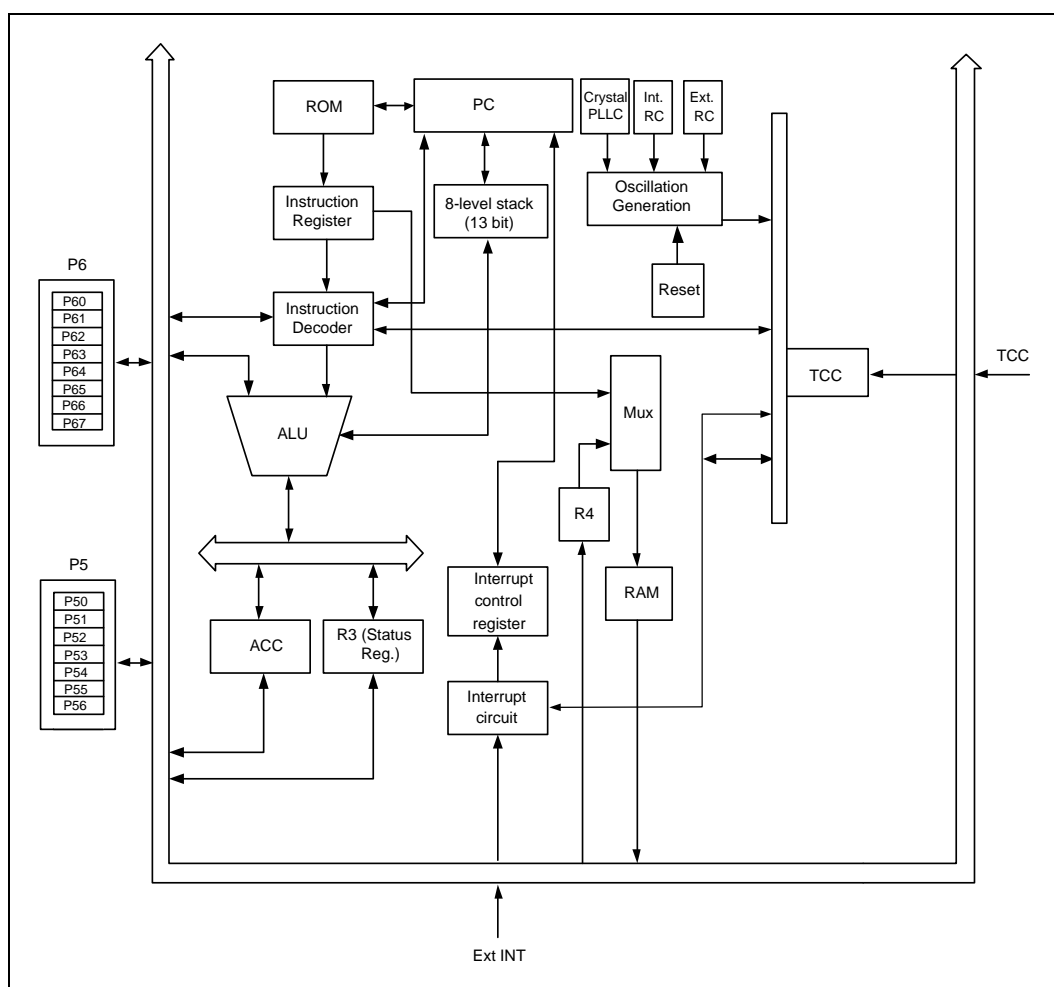


Figure 5-1 Block Diagram

6 Function Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Time Clock/Counter)

- Incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers
- Defined by resetting PAB (CONT-3)
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter) and Stack

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.

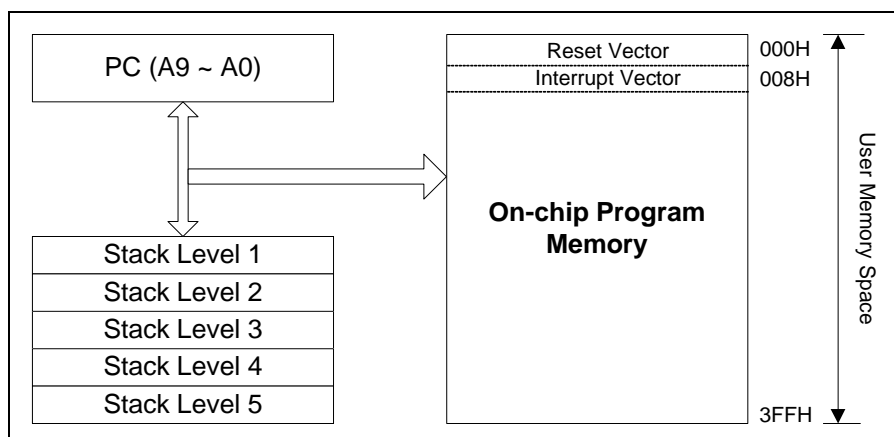


Figure 6-1 Program Counter Organization

- The configuration structure generates 1024×13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0" when under RESET condition.

- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETLk", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and succeeding bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction (except "ADD R2,A") written to R2 (e.g., "MOV R2, A", "BC R2, 6") will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for instructions that would change the contents of R2. Such instruction will require one more instruction cycle.
- The Data Memory Configuration is as follows:

Address	R PAGE Registers	IOC PAGE Registers
00	R0 (IAR)	Reserve
01	R1 (TCC)	CONT (Control Register)
02	R2 (PC)	Reserve
03	R3 (Status)	Reserve
04	R4 (RSR)	Reserve
05	R5 (Port 5)	IOC5 (I/O Port Control Register)
06	R6 (Port 6)	IOC6 (I/O Port Control Register)
07	Reserve	Reserve
08	Reserve	Reserve
09	Reserve	Reserve
0A	Reserve	IOCA (Prescaler Control Register)
0B	Reserve	IOCB (Pull-down Register)
0C	Reserve	IOCC (Open-drain Control)
0D	RD (Only for simulator)	IOCD (Pull-high Control Register)
0E	RE (Wake-up control)	IOCE (WDT Control Register)
0F	RF (Interrupt Status)	IOCF (Interrupt Mask Register)
10 : 3F	General Registers	

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP2	GP1	GP0	T	P	Z	DC	C

Bit 0 (C): Carry flag

Bit 1 (DC): Auxiliary carry flag

Bit 2 (Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 3 (P): Power down bit

Set to "1" during power on or by a "WDTC" command; and reset to "0" by a "SLEP" command.

Bit 4 (T): Time-out bit

Set to "1" with the "SLEP" and "WDTC" commands, or during power up and reset to "0" by WDT time-out.

Bits 5 ~ 7 (GP0 ~ GP2): General-purpose read/write bits

6.1.5 R4 (RAM Select Register)

Bits 0~5: are used to select registers (Address: 00~06, 0F~3F) in the indirect addressing mode.

Bits 6 ~ 7: Not used (read only). Set these bits to "1" all the time.

The "Z" flag of R3 will be set to "1" when the R4 content is equal to "3F." When $R4=R4+1$, the R4 content will select "R0."

6.1.6 R5 ~ R6 (Port 5 ~ Port 6)

R5 and R6 are I/O registers. Only the lower 7 bits of R5 are available.

6.1.7 RD (Manual Calibration Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EM78P159N	×	×	×	×	×	×	×	×
ICE159N Simulator	-	-	-	-	C3	C2	C1	C0

For EM78P159N: The register does not exist in the actual chip.

For ICE159N Simulator: C3 ~ C0 are IRC calibration bits in MCIRC mode.

Bit 3 ~ Bit 0 (C3 ~ C0): calibration bits in internal RC mode

C3	C2	C1	C0	Cycle Time (ns)	Frequency (MHz)
0	0	0	0	390.6	2.56
0	0	0	1	365.0	2.74
0	0	1	0	342.5	2.92
0	0	1	1	322.6	3.10
0	1	0	0	304.9	3.28
0	1	0	1	289.0	3.46
0	1	1	0	274.7	3.64
0	1	1	1	261.8	3.82
1	1	1	1	250.0	4.00
1	1	1	0	239.2	4.18
1	1	0	1	229.4	4.36
1	1	0	0	220.3	4.54
1	0	1	1	211.9	4.72
1	0	1	0	204.1	4.90
1	0	0	1	196.7	5.08
1	0	0	0	190.1	5.26

Note: ¹: Frequency values shown are theoretical and taken from an instance of a high frequency mode. Hence they are shown for reference only. Definite values will depend on the actual process.

²: Similar way of calculation is also applicable for Low Frequency mode.

Bits 4 ~ 7: Not used

6.1.8 RE (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	ICWE	-

Bit 0: Not used

Bit 1 (ICWE): Port 6 input status change wake-up enable bit

0: Disable Port 6 input status change wake-up

1: Enable Port 6 input status change wake-up

Bits 2 ~ 7: Not used

6.1.9 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

Note: “1” means with interrupt request “0” means no interrupt occurs

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes. Reset by software.

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on /INT pin. Reset by software.

Bits 3 ~ 7: Not used

RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE

The result of reading RF is the "logic AND" of RF and IOCF.

6.1.10 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/INT	TS	TE	PSRE	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2): TCC prescaler bits

PSR2	PSR1	PSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (PSRE): Prescaler enable bit for TCC

- 0: prescaler disable bit, TCC rate is 1:1
- 1: prescaler enable bit, TCC rate is set as Bit 2~Bit 0

Bit 4 (TE): TCC signal edge

- 0: increment if a transition from low to high takes place on the TCC pin
- 1: increment if a transition from high to low takes place on the TCC pin

Bit 5 (TS): TCC signal source

- 0: internal instruction cycle clock, P54 is a bidirectional I/O pin
- 1: transition on TCC pin

Bit 6 (/INT): Interrupt enable flag

- 0: masked by DISI or hardware interrupt
- 1: enabled by ENI/RETI instructions

Bit 7: Not used

CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC6 (I/O Port Control Register)

- 0: defines the relative I/O pin as output
- 1: puts the relative I/O pin into high impedance

Only the lower 7 bits of IOC5 can be defined. IOC5 and IOC6 registers are both readable and writable.

6.2.4 IOCA (Prescaler Counter Register)

The IOCA register is readable. The value of IOCA is equal to the contents of the Prescaler counter. It is a Down counter register.

6.2.5 IOCB (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

Bit 0 (/PD0): Control bit is used to enable the pull-down of P50 pin.

- 0: Enable internal pull-down
- 1: Disable internal pull-down

Bit 1 (/PD1): Control bit used to enable the P51 pull-down pin

Bit 2 (/PD2): Control bit used to enable the P52 pull-down pin

Bit 3 (/PD3): Control bit used to enable the P53 pull-down pin

Bit 4 (/PD4): Control bit used to enable the P60 pull-down pin

Bit 5 (/PD5): Control bit used to enable the P61 pull-down pin

Bit 6 (/PD6): Control bit used to enable the P62 pull-down pin

Bit 7 (/PD7): Control bit used to enable the P63 pull-down pin

The IOCB Register is both readable and writable.

6.2.6 IOCC (Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

Bit 0 (OD0): Control bit used to enable the P60 open-drain pin.

0: Disable open-drain output

1: Enable open-drain output

Bit 1 (OD1): Control bit used to enable the P61 open-drain output pin

Bit 2 (OD2): Control bit used to enable the P62 open-drain output pin

Bit 3 (OD3): Control bit used to enable the P63 open-drain output pin

Bit 4 (OD4): Control bit used to enable the P64 open-drain output pin

Bit 5 (OD5): Control bit used to enable the P65 open-drain output pin

Bit 6 (OD6): Control bit used to enable the P66 open-drain output pin

Bit 7 (OD7): Control bit used to enable the P67 open-drain output pin

The IOCC Register is both readable and writable.

6.2.7 IOCD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

Bit 0 (/PH0): Control bit used to enable the P60 pull-high pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 1 (/PH1): Control bit used to enable the P61 pull-high pin

Bit 2 (/PH2): Control bit used to enable the P62 pull-high pin

Bit 3 (/PH3): Control bit used to enable the P63 pull-high pin

Bit 4 (/PH4): Control bit used to enable the P64 pull-high pin

Bit 5 (/PH5): Control bit used to enable the P65 pull-high pin

Bit 6 (/PH6): Control bit used to enable the P66 pull-high pin

Bit 7 (/PH7): Control bit used to enable the P67 pull-high pin

The IOCD Register is both readable and writable.

6.2.8 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	ROC	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of P60 (/INT) pin

0: P60, bidirectional I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1."

When EIS is "0," the path of /INT is masked. When EIS is "1," the status of /INT pin can also be read by way of reading Port 6 (R6). For reference see Figure 6-3a under Section 6.4. EIS is both readable and writable.

Bit 5: Not used

Bit 4 (ROC): ROC is used for the R-option

Setting the ROC to "1" enables the status of R-option pins (P50~P51) that are read by the controller. Clearing the ROC disables the R-option function. If the R-option function is selected, the P51 pin and/or P50 pin must be connected to VSS with a 430KΩ external resistor (Rex). If the Rex is connected or disconnected, the status of P50 (P51) is read as "0"/"1." For reference, refer to Figure 6-4 under Section 6.4.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: prescaler disable bit, WDT rate is 1:1

1: prescaler enable bit, WDT rate is set as Bit 4~Bit 2

Bit 2 (PSW2) ~ Bit 0 (PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.9 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIE	ICIE	TCIE

Bit 0 (TCIE): TCIF interrupt enable bit

0: disable TCIF interrupt

1: enable TCIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: disable ICIF interrupt

1: enable ICIF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit

0: disable EXIF interrupt

1: enable EXIF interrupt

Bits 3 ~ 7: Not used

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1."

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-6 in Section 6.6 for further reference.

IOCF register is both readable and writable.

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for TCC and WDT respectively. The PSR0 ~ PSR2 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PWR0 ~ PWR2 bits of the IOCE register are used to determine the WDT prescaler. The prescaler (PSR0 ~ PSR2) will be cleared by the instruction each time it writes to TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions.

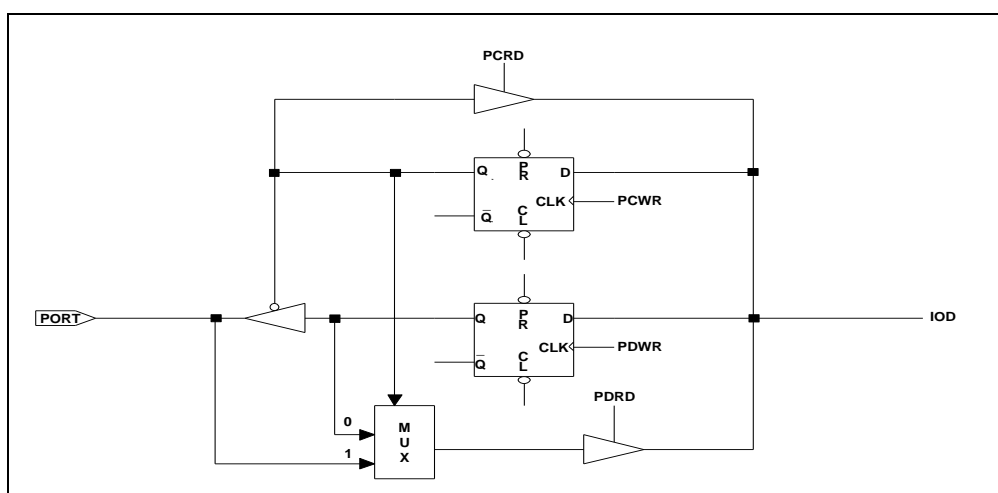
- R1 (TCC) is an 8-bit timer/counter. The TCC clock source can be internal or external clock input (edge selectable from TCC pin). If TCC signal is sourced from the internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). $CLK = F_{osc}/2$ or $CLK = F_{osc}/4$ application is determined by the Code Option bit CLK status. $CLK = F_{osc}/2$ is used if CLK bit is "0," and $CLK = F_{osc}/4$ is used if CLK bit is "1." If TCC signal source comes from external clock input, TCC is incremented by 1 at every falling edge or rising edge of the TCC pin.
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in Sleep mode). During normal operation or Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during Normal mode by software programming. Refer to WDTE bit of IOCE register in Section 5.2.8. Without prescaler, the WDT time-out period is approximately 18 ms¹ (default).

¹ Vdd = 5V, set up time period = 16.8ms ± 30%
Vdd = 3V, set up time period = 18ms ± 30%

6.4 I/O Ports

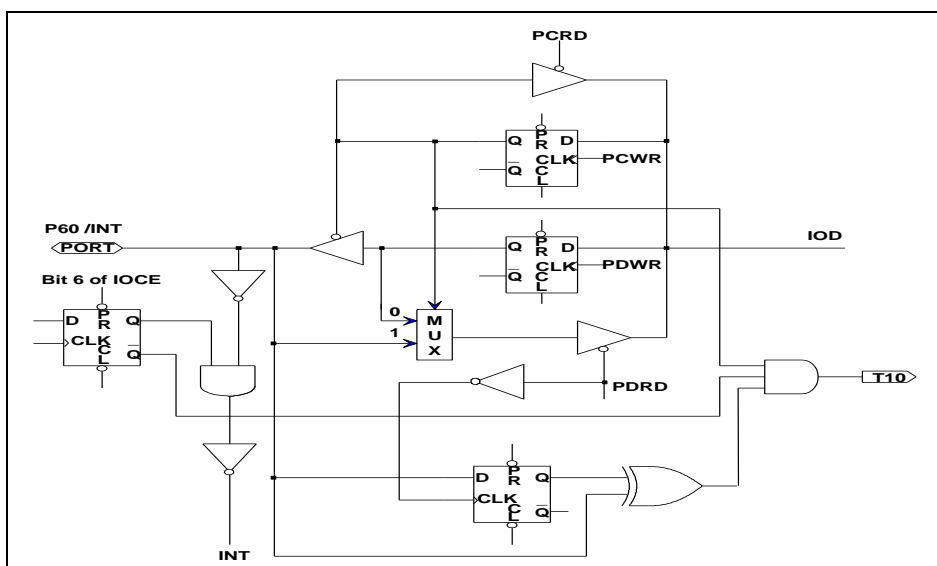
The I/O registers, both Port 5 and Port 6, are bidirectional tri-state I/O ports. Port 6 can be pulled high internally by software. In addition, Port 6 can also have an open-drain output by software and an Input status change interrupt (or wake-up) function. P50 ~ P53 and P60 ~ P63 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6). P50~P51 are the R-option pins enabled by setting the ROC bit in the IOCE register to "1." When the R-option function is used, it is recommended that P50 ~ P51 are used as output pins. When R-option is in enable state, P50 ~ P51 must be programmed as input pins. In R-option mode, the current/power consumption by Rex should be taken into consideration to conserve power.

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in the following figures (Figures 6-2, 6-3a, 6-3b, and 6-4).



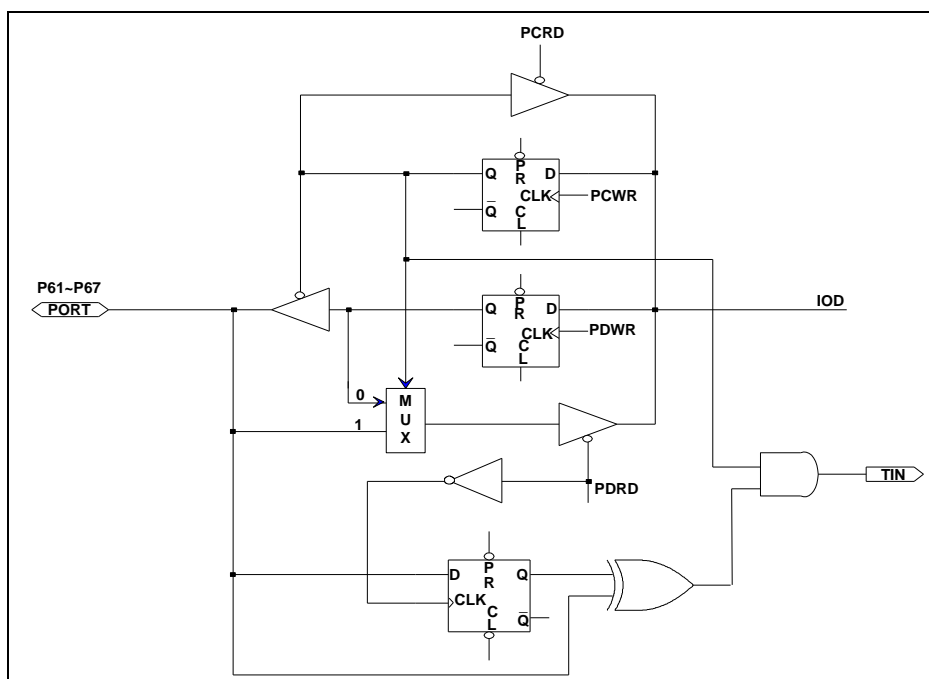
Note: Pull down is not shown in the figure.

Figure 6-2 I/O Port and I/O Control Register for Port 5 Circuit



Note: Pull-high (down) and open-drain are not shown in the figure.

Figure 6-3a I/O Port and I/O Control Register for P60 (/INT) Circuit



Note: Pull-high (down) and open-drain are not shown in the figure.

Figure 6-3b I/O Port and I/O Control Register for P61~P67 Circuit

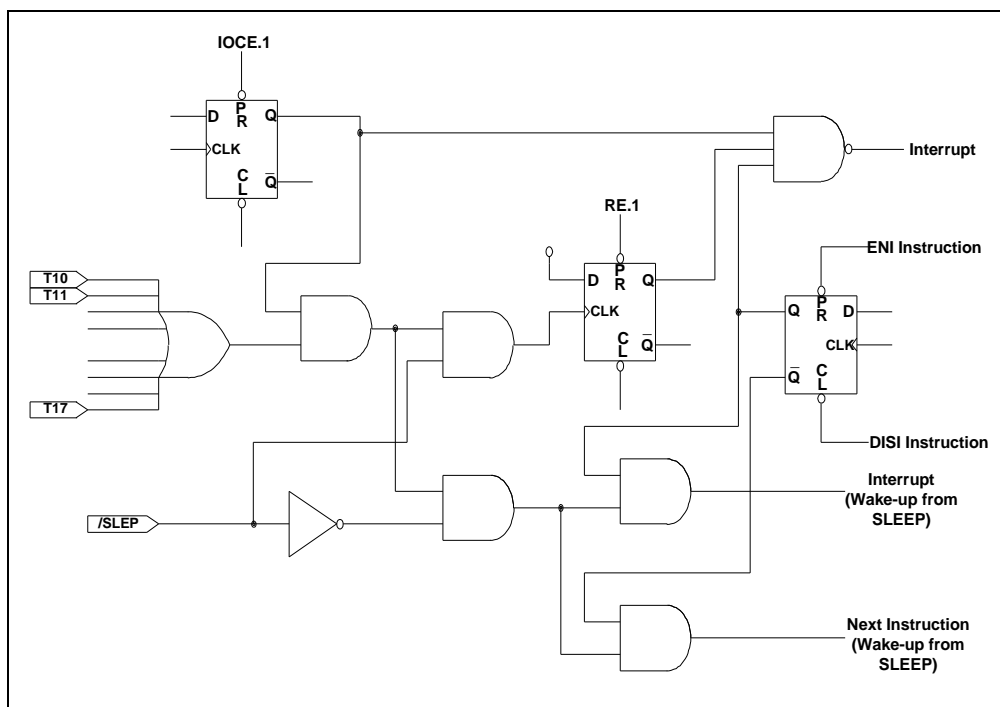


Figure 6-3c I/O Port 6 with Input Change Interrupt/Wake-up Block Diagram

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up	(II) Wake-up and interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port 6 (MOV R6, R6)	2. Read I/O Port 6 (MOV R6, R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set RE ICWE =1)	4. Enable wake-up bit (Set RE ICWE =1)
5. Execute "SLEEP" instruction	5. Enable interrupt (Set IOCF ICIE =1)
(b) After wake-up	6. Execute "SLEEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (008H)
	2. IF "DISI" → Next instruction
(III) Interrupt	
(a) Before Port 6 pin change	
1. Read I/O Port 6 (MOV R6,R6)	
2. Execute "ENI" or "DISI"	
3. Enable interrupt (Set IOCF0 ICIE =1)	
(b) After Port 6 pin changed (interrupt)	
1. IF "ENI" → Interrupt vector (008H)	
2. IF "DISI" → Next instruction	



- The CONT register bits are set to all "1" except for Bit 6 (INT flag).
- When power is switched on, the upper three bits of R3 are cleared.
- The IOCA register bits are set to all "1."
- The IOCB register bits are set to all "1."
- The IOCC register is cleared.
- The IOCD register bits are set to all "1."
- Bit 7 of the IOCE register is set to "1," and Bits 4 and 6 are cleared.
- Bits 0 ~ 2 of RF and Bits 0 ~ 2 of IOCF registers are cleared.

Sleep (power down) mode is asserted by executing the "SLEP" instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be awakened by:

- 1) External reset input on /RESET pin
- 2) WDT time-out (if enabled)
- 3) Port 6 input status changed (if enabled)

The first two cases will cause the EM78P159N series to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up). The last case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 008H after wake-up. If DISI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after wake-up.

Wake-up time is dependent on oscillator mode. In RC mode, the reset time is 32 clocks, and in High Crystal mode, reset time is 2 ms and 32 clocks. In Low Crystal mode, the reset time is 500 ms. This is applicable only for stable oscillators.

Only one of Cases 2 and 3 can be enabled before going into Sleep mode. That is,

- [a]** if Port 6 Input Status Change Interrupt is enabled before SLEP, WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78P159N series can be awakened only by Case 1 or Case 3.
- [b]** if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P159N series can be awakened only by Case 1 or Case 2. For further details, refer to Section 5.6, *Interrupt*.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78P159N series (Case [a] above), the following instructions must be executed before SLEEP:

```
WDTC                      ; Clear WDT and prescaler
MOV A, @0xxxxxxxh        ; Disable WDT and Select WDT prescaler
IOW IOCE
MOV R6, R6                ; Read Port 6
BS RE,1                  ; Enable wake up control bit
MOV A, @00000x1xb        ; Enable Port 6 input change interrupt
IOW IOCF
ENI (or DISI)             ; Enable (or disable) global interrupt
SLEEP                     ; Sleep
NOP
```

6.5.2 Summary of Registers Initialized Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	×	C56	C55	C54	C53	C52	C51	C50
		Power-on	U	1	1	1	1	1	1	1
		/RESET and WDT	U	1	1	1	1	1	1	1
		Wake-up from Pin Change	U	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	×	/INT	TS	TE	PSRE	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	*0/P	*0/P	*0/P	*0/P	*1/P	*0/P	*0/P	*0/P
0x03	R3 (SR)	Bit Name	GP2	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	**	**	P	P	P
		Wake-up from Pin Change	P	P	P	**	**	P	P	P
0x04	R4 (RSR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	U	U	U	U	U	U
		/RESET and WDT	1	1	P	P	P	P	P	P
		Wake-up from Pin Change	1	1	P	P	P	P	P	P
0x05	P5	Bit Name	×	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	U	U	U	U	U	U	U
		/RESET and WDT	0	P	P	P	P	P	P	P
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0E	RE (WUE)	Bit Name	×	×	×	×	×	×	ICWE	×
		Power-on	U	U	U	U	U	U	0	U
		/RESET and WDT	U	U	U	U	U	U	0	U
		Wake-up from Pin Change	U	U	U	U	U	U	P	U
0x0F	RF (ISR)	Bit Name	×	×	×	×	×	EXIF	ICIF	TCIF
		Power-on	U	U	U	U	U	0	0	0
		/RESET and WDT	U	U	U	U	U	0	0	0
		Wake-up from Pin Change	U	U	U	U	U	P	P	P
0x0A	IOCA	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC	Bit Name	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	WDTE	EIS	×	ROC	PSWE	PSW2	PSW1	PSW0
		Power-on	1	0	U	0	0	0	0	0
		/RESET and WDT	1	0	U	0	0	0	0	0
		Wake-up from Pin Change	1	P	U	P	P	P	P	P
0x0F	IOCF	Bit Name	×	×	×	×	×	EXIE	ICIE	TCIE
		Power-on	U	U	U	U	U	0	0	0
		/RESET and WDT	U	U	U	U	U	0	0	0
		Wake-up from Pin Change	U	U	U	U	U	P	P	P
0x10~0x3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend:

×: Not used U: Unknown or don't care P: Previous value before reset

* Jump to Address 0x08, or execute the instruction next to the "SLEP" instruction.

** Refer to tables provided in the next section (Section 6.5.3).

6.5.3 Status of RST, T, and P of the Status Register

A Reset condition is initiated by the following events

- 1) A power-on condition
- 2) A high-low-high pulse on /RESET pin, and
- 3) Watchdog timer time-out

The values of T and P listed in the table below are used to check how the processor wakes up.

■ The Values of RST, T, and P after Reset

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* P: Previous status before reset

The following table shows the events that may affect the status of T and P.

■ The Status of T and P Being Affected by Events

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up due to pin change during Sleep mode	1	0

* P: Previous status before reset

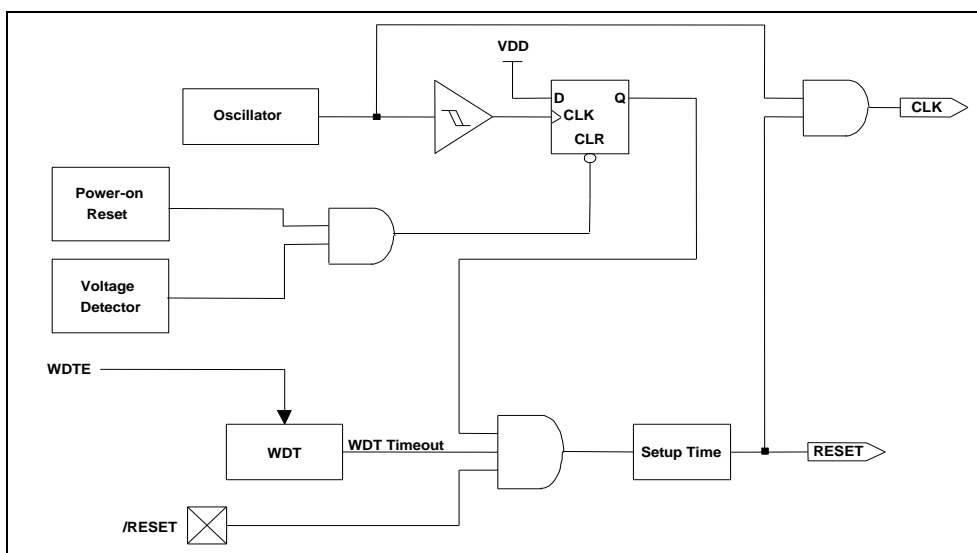


Figure 6-5 Controller Reset Block Diagram

6.6 Interrupt

The EM78P159N series has three falling-edge interrupts:

- 1) TCC overflow interrupt
- 2) Port 6 Input Status Change Interrupt
- 3) External interrupt [(P60, /INT) pin]

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6, R6") is necessary. Each Port 6 pin will have this feature if its status changes. Any pin configured as output or P60 pin configured as /INT is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the EM78P159N series from Sleep mode if Port 6 is enabled prior to going into the Sleep mode by executing SLEP. When the chip wakes-up, the controller will continue to execute the succeeding address if the global interrupt is disabled or it will branch into the interrupt vector 008H if the global interrupt is enabled.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to the figure below). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (enabled), the next instruction will be fetched from Address 001H.

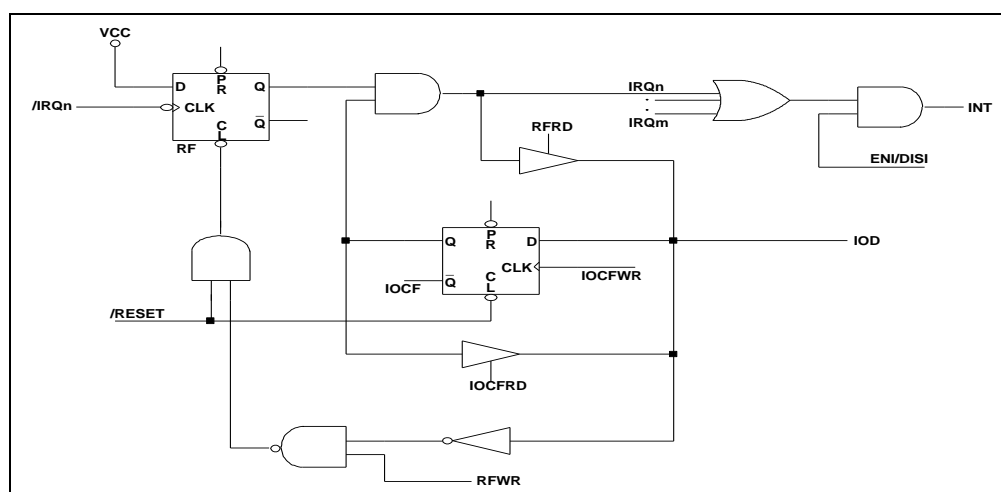


Figure 6-6 Interrupt Input Circuit

6.7 Oscillator

6.7.1 Oscillator Modes

The EM78P159N series can be operated in four different oscillator modes, such as External RC oscillator mode (ERC), Internal RC oscillator mode (IRC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). The desired mode can be selected by programming OSC2, OSC1, and OSC0 in the Code option register. The Table below describes how these four oscillator modes are defined with OSC2, OSC1, and OSC0.

■ Oscillator Modes Defined by OSC

Mode		OSC2	OSC1	OSC0
ERC (External RC oscillator mode); P55/OSCO act as P55		0	0	0
ERC (External RC oscillator mode); P55/OSCO act as OSCO		0	0	1
IRC (Internal RC oscillator mode) ; P55/OSCO act as P55		0	1	0
IRC (Internal RC oscillator mode); P55/OSCO act as OSCO		0	1	1
MCIRC (Manual calibration IRC mode); P55/OSCO act as P55	With ICE only	1	0	0
MCIRC (Manual calibration IRC mode); P55/OSCO act as OSCO		1	0	1
LXT (Low Crystal oscillator mode)		1	1	0
HXT (High Crystal oscillator mode) (default)		1	1	1

Note: The transient point of system frequency between HXT and LXY is 400kHz.

The maximum operational frequency of the crystal/resonator under different VDDs is as listed below.

■ Summary of Maximum Operating Speeds

Conditions	VDD	Max Freq. (MHz)
Two cycles with two clocks	2.1	4.0
	3.0	8.0
	5.0	20.0

6.7.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P159N series can be driven by an external clock signal through the OSCI pin as shown in the following figure.

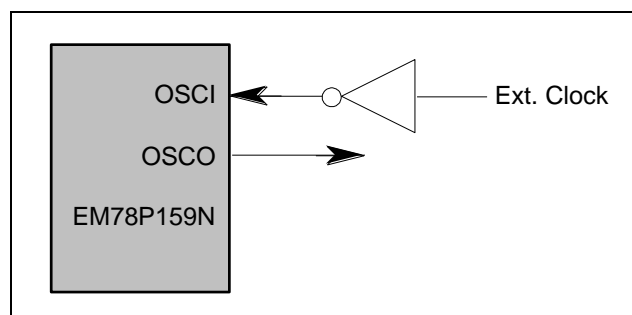


Figure 6-7a External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. The Figure below depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

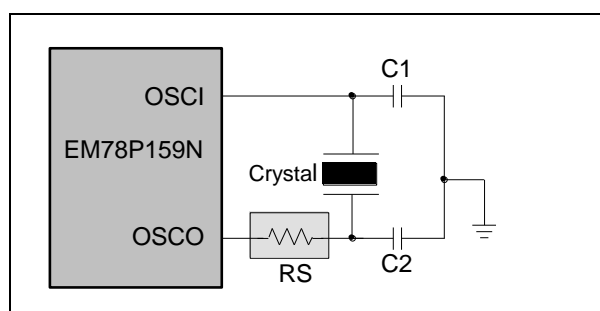


Figure 6-7b Crystal/Resonator Circuit

■ Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

Note: The values of capacitors C1 and C2 are for reference only.

6.7.3 External RC Oscillator Mode

For some applications that do not require a very precise timing calculation, the RC oscillator (Figure 6-8 below) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (R_{ext}), the capacitor (C_{ext}), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

In order to maintain a stable system frequency, the values of the C_{ext} should not be less than 20pF, and the value of R_{ext} should not be greater than 1 M Ω . If they cannot be kept in this range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the R_{ext} in the RC oscillator is, the faster its frequency will be. On the contrary, for very low R_{ext} values, for instance, 1 K Ω , the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the PCB layout, will affect the system frequency.

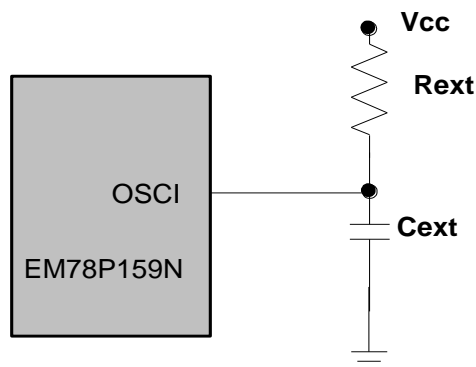


Figure 6-8 External RC Oscillator Mode Circuit

■ RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20pF	3.3k	3.92 MHz	3.65 MHz
	5.1k	2.67 MHz	2.60 MHz
	10k	1.39MHz	1.40 MHz
	100k	149 kHz	156 kHz
100pF	3.3k	1.39 MHz	1.33 MHz
	5.1k	940 kHz	920 kHz
	10k	480 kHz	475 kHz
	100k	52 kHz	50 kHz
300pF	3.3k	595 kHz	560 kHz
	5.1k	400 kHz	390 kHz
	10k	200 kHz	200 kHz
	100k	21 kHz	20 kHz

Note: ¹: Measured based on DIP packages.
²: The values are for design reference only.
³: The frequency drift is $\pm 30\%$.

6.7.4 Internal RC Oscillator Mode

The EM78P159N series offers a versatile internal RC mode with default frequency value of 4MHz. The Internal RC oscillator mode has other frequencies (1 MHz, 8 MHz and 455kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. All these four main frequencies can be calibrated by programming the Option Bits C3 ~ C0. The table below describes a typical instance of the calibration.

■ Internal RC Drift Rate (Ta = 25°C, VDD = 3.9V \pm 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C ~ +125°C)	Voltage (2.3V ~ 5.5V)	Process	Total
4 MHz	(+5) ~ -8.5%	$\pm 5\%$	$\pm 4\%$	(+14) ~ -17.5%
8 MHz	(+5) ~ -8.5%	$\pm 5\%$	$\pm 4\%$	(+14) ~ -17.5%
1 MHz	(+5) ~ -8.5%	$\pm 5\%$	$\pm 4\%$	(+14) ~ -17.5%
455kHz	(+5) ~ -8.5%	$\pm 5\%$	$\pm 4\%$	(+14) ~ -17.5%

Note: These are theoretical values which are provided for reference only. Actual values may vary depending on the actual process.

■ **Calibration Selection for Internal RC Mode**

C3	C2	C1	C0	Cycle Time (ns)	Frequency (MHz)
0	0	0	0	390.6	2.56
0	0	0	1	365.0	2.74
0	0	1	0	342.5	2.92
0	0	1	1	322.6	3.10
0	1	0	0	304.9	3.28
0	1	0	1	289.0	3.46
0	1	1	0	274.7	3.64
0	1	1	1	261.8	3.82
1	1	1	1	250.0	4.00
1	1	1	0	239.2	4.18
1	1	0	1	229.4	4.36
1	1	0	0	220.3	4.54
1	0	1	1	211.9	4.72
1	0	1	0	204.1	4.90
1	0	0	1	196.7	5.08
1	0	0	0	190.1	5.26

Note: These are theoretical values which are provided for reference only. Actual values may vary depending on the actual process.

6.8 Code Option Register

The EM78P159N series has Code option words that are not part of the normal program memory. The option bits cannot be accessed during normal program execution.

■ **Code Option Register and Customer ID Register Arrangement Distribution:**

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.8.1 Code Option Register (Word 0)

Word 0													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	—	—	—	—	CLKS	ENWDTB	OSC2	OSC1	OSC0	HLP	Protect		
1	—	—	—	—	4 clocks	Disable	High	High	High	High	Disable		
0	—	—	—	—	2 clocks	Enable	Low	Low	Low	Low	Enable		

Bit 0 ~ Bit 2 (Protect): Protect bits

Protect type can be chosen as enable or disable.

Bit 3 (HLP): Power selection

0: Low power

1: High power

Bit 4 ~ Bit 6 (OSC0 ~ OSC2): Oscillator Modes Selection bits

Mode		OSC2	OSC1	OSC0
ERC (External RC oscillator mode); P55/OSCO acts as P55		0	0	0
ERC (External RC oscillator mode); P55/OSCO acts as OSCO		0	0	1
IRC (Internal RC oscillator mode) ; P55/OSCO acts as P55		0	1	0
IRC (Internal RC oscillator mode); P55/OSCO acts as OSCO		0	1	1
MCIRC (Manual calibration IRC mode); P55/OSCO acts as P55	With ICE only	1	0	0
MCIRC (Manual calibration IRC mode); P55/OSCO acts as OSCO		1	0	1
LXT (Low Crystal oscillator mode)		1	1	0
HXT (High Crystal oscillator mode) (default)		1	1	1

Note: The transient point of system frequency between HXT and LXI is 400kHz.

Bit 7 (ENWDTB): Watchdog timer enable bit

0: Enable

1: Disable

Bit 8 (CLKS): Instruction period option bit

Word 0	CLK0
Four oscillator time periods (default)	1
Two oscillator time periods	0

For further details, refer to Section 5.12 *Instruction Set*.

Bit 9: Not used, but need to be set to “1” all the time to avoid possible error.

Bit 10: Not used, but need to be set to “0” all the time to avoid possible error.

Bit 11 ~ Bit 12: Not used, but need to be set to “1” all the time to avoid possible error.

6.8.2 Customer ID Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	RCOUT	–	–	–	–	CYES	C3	C2	C1	C0	RCM1	RCM0
1	–	System_clk	–	–	–	–	2 cycles	High	High	High	High	High	High
0	–	Open_drain	–	–	–	–	1 cycle	Low	Low	Low	Low	Low	Low

Bit 0 ~ Bit 1 (RCM0 ~ RCM1): IRC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	8
0	1	1
0	0	455kHz

Bits 5, 4, 3 and Bit 2 (C3, C2, C1, and C0): Calibration bits of internal RC mode.

These bits must always be set to “1” only (auto calibration).

Bit 6 (CYES): Instruction cycle selection bit

0: one instruction cycle

1: two instruction cycles (default)

Bit 7 ~ Bit 10: Not used

Bits 11 (RCOUT): System clock output enable bit in IRC or ERC mode

0: OSCO pin is open drain

1: OSCO output system clock

Bit 12: Not used

6.8.3 Customer ID Register (Word 2)

Word 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	–	–	–	–	–	–

Bit 0 ~ Bit 12: User's ID code

6.9 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply has stabilized.

The EM78P159N series POR voltage range is 1.7V~1.9V. For customer application, when power is OFF, Vdd must drop to below 1.2V and remains OFF for 10 μ s before power can be switched ON again. This way, the EM78P159N series will reset and operates normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

6.10 External Power-on Reset Circuit

The circuits shown in the figure implement an external RC provided to produce a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operation voltage. This circuit is used when the power supply has a slow rise time. Since the current leakage

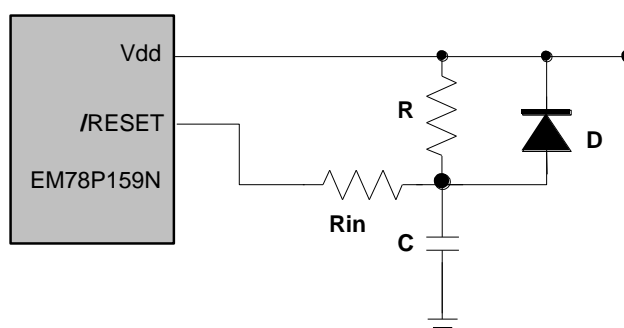


Figure 6-9 External Power-up Reset Circuit

from the /RESET pin is about $\pm 5 \mu$ A, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

6.11 Residue-Voltage Protection

When the battery is replaced, device power (Vdd) is cut off but residue-voltage remains. The residue-voltage may trip below minimum Vdd, but not to zero. This condition may cause a poor power-on reset. The following figures illustrate two recommended methods on how to build a residue-voltage protection circuit for EM78P159N series.

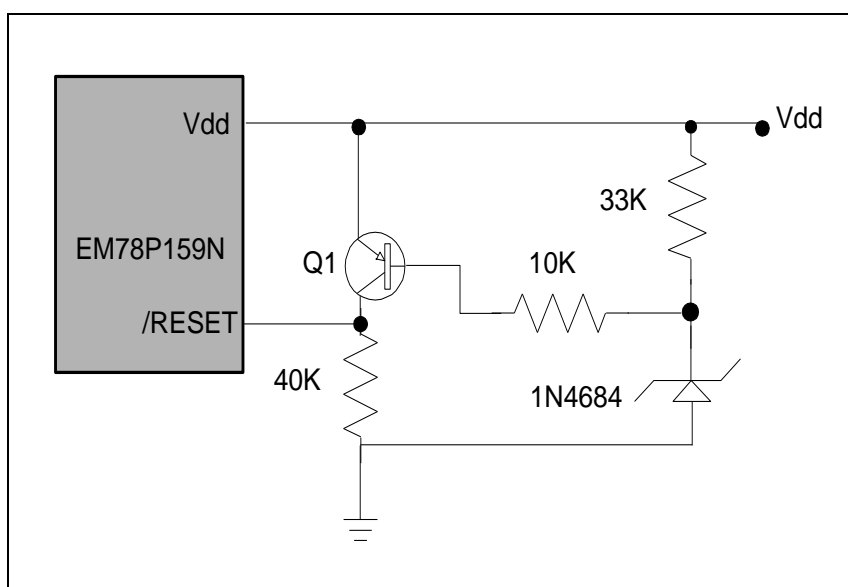


Figure 6-10a Residue Voltage Protection Circuit 1

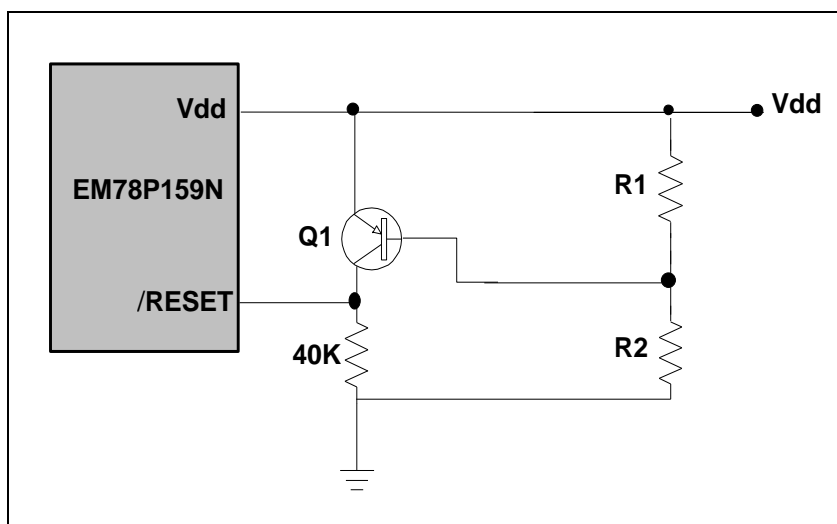


Figure 6-10b Residue Voltage Protection Circuit 2

6.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

- (A) Change one instruction cycle to consist of 4 oscillator periods.
- (B) "JMP," "CALL," "RET," "RETL," "RETI," or the conditional skip ("JBS," "JBC," "JZ," "JZA," "DJZ," "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be $CLK = Fosc/4$, instead of $Fosc/2$.

Moreover, the instruction set has the following features:

- 1) Every bit of any register can be set, cleared, or tested directly.
- 2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None ¹
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None ¹
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0100 10rr rrrr	04rr	COMA R	$/R \rightarrow A$	Z
0 0100 11rr rrrr	04rr	COM R	$/R \rightarrow R$	Z
0 0101 00rr rrrr	05rr	INCA R	$R+1 \rightarrow A$	Z
0 0101 01rr rrrr	05rr	INC R	$R+1 \rightarrow R$	Z
0 0101 10rr rrrr	05rr	DJZA R	$R-1 \rightarrow A$, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	$R-1 \rightarrow R$, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	$R(n) \rightarrow A(n-1)$, $R(0) \rightarrow C$, $C \rightarrow A(7)$	C
0 0110 01rr rrrr	06rr	RRC R	$R(n) \rightarrow R(n-1)$, $R(0) \rightarrow C$, $C \rightarrow R(7)$	C
0 0110 10rr rrrr	06rr	RLCA R	$R(n) \rightarrow A(n+1)$, $R(7) \rightarrow C$, $C \rightarrow A(0)$	C
0 0110 11rr rrrr	06rr	RLC R	$R(n) \rightarrow R(n+1)$, $R(7) \rightarrow C$, $C \rightarrow R(0)$	C
0 0111 00rr rrrr	07rr	SWAPA R	$R(0-3) \rightarrow A(4-7)$, $R(4-7) \rightarrow A(0-3)$	None
0 0111 01rr rrrr	07rr	SWAP R	$R(0-3) \leftrightarrow R(4-7)$	None
0 0111 10rr rrrr	07rr	JZA R	$R+1 \rightarrow A$, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	$R+1 \rightarrow R$, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	$0 \rightarrow R(b)$	None ²
0 101b bbrr rrrr	0xxx	BS R,b	$1 \rightarrow R(b)$	None ³
0 110b bbrr rrrr	0xxx	JBC R,b	if $R(b)=0$, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if $R(b)=1$, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	$PC+1 \rightarrow [SP]$, $(Page, k) \rightarrow PC$	None
1 01kk kkkk kkkk	1kkk	JMP k	$(Page, k) \rightarrow PC$	None
1 1000 kkkk kkkk	18kk	MOV A,k	$k \rightarrow A$	None
1 1001 kkkk kkkk	19kk	OR A,k	$A \vee k \rightarrow A$	Z
1 1010 kkkk kkkk	1Akk	AND A,k	$A \& k \rightarrow A$	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	$A \oplus k \rightarrow A$	Z
1 1100 kkkk kkkk	1Ckk	RETL k	$k \rightarrow A$, $[Top\ of\ Stack] \rightarrow PC$	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	$k-A \rightarrow A$	Z, C, DC
1 1110 0000 0001	1E01	INT	$PC+1 \rightarrow [SP]$, $001H \rightarrow PC$	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	$k+A \rightarrow A$	Z, C, DC

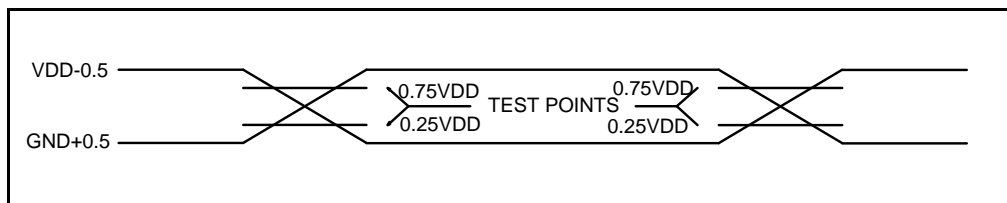
Note: ¹ This instruction is applicable to IOC5~IOC6, IOCB ~ IOCF only.

² This instruction is not recommended for RF operation.

³ This instruction cannot operate under RF.

6.13 Timing Diagrams

AC Test Input/Output Waveform



Note: AC Testing: Input are driven at VDD-0.5V for logic "1," and GND+0.5V for logic "0"
Timing measurements are made at 0.75VDD for logic "1," and 0.25VDD for logic "0"

Figure 6-13a AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK="0")

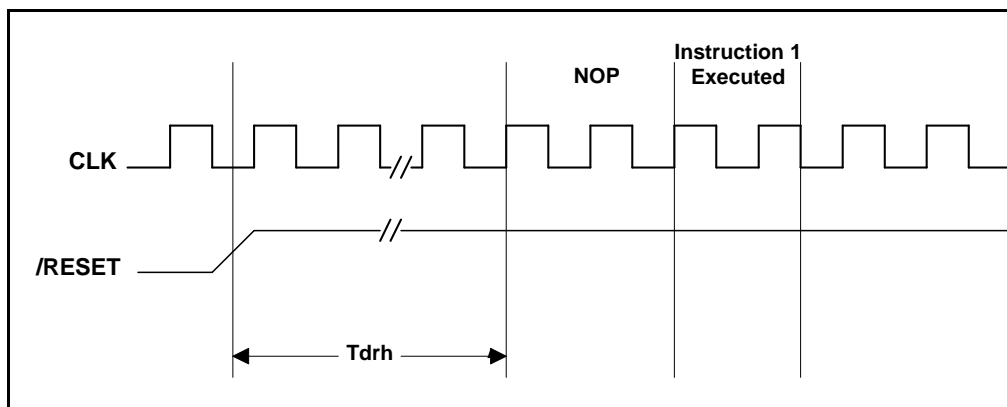


Figure 6-13b Reset Timing Diagram

TCC Input Timing (CLKS="0")

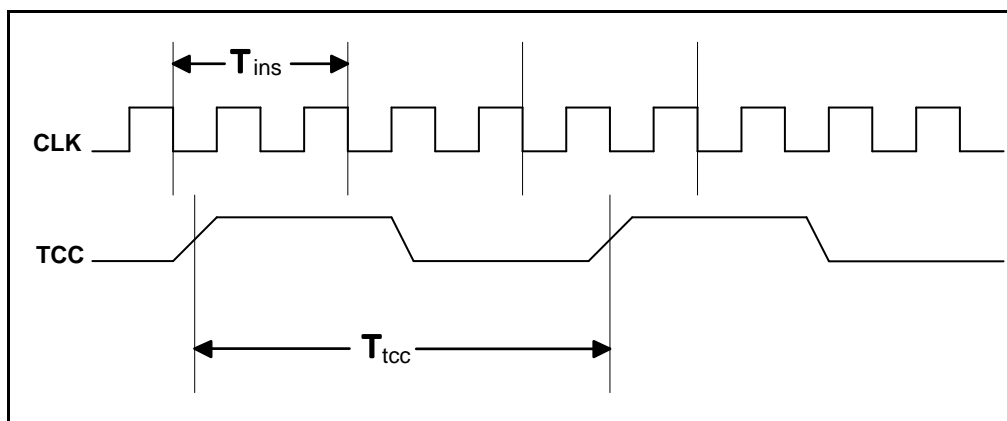


Figure 6-13c TCC Input Timing Diagram

7 Absolute Maximum Ratings

Items	Rating
Temperature under bias	-40°C to 125°C
Storage temperature	-65°C to 150°C
Working voltage	2.1 to 5.5V
Working frequency	DC to 20MHz*
Input voltage	Vss-0.3V to Vdd+0.5V
Output voltage	Vss-0.3V to Vdd+0.5V

Note: * These parameters are theoretical values and have not been tested.

8 Electrical Characteristics

8.1 DC Characteristics

Ta=25°C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8.0	MHz
	Crystal: VDD to 5V	Two cycles with two clocks	DC	–	20.0	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	940	F±30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6 (Schmitt Trigger)	–	0.75Vdd	–	V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6 (Schmitt Trigger)	–	0.3Vdd	–	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt Trigger)	–	2.0	–	V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)	–	1.2	–	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI (Schmitt Trigger)	–	0.75Vdd	–	V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI (Schmitt Trigger)	–	0.3Vdd	–	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6 (Schmitt Trigger)	–	0.75Vdd	–	V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6 (Schmitt Trigger)	–	0.3Vdd	–	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt Trigger)	–	1.5	–	V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt Trigger)	–	0.9	–	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI (Schmitt Trigger)	–	0.75Vdd	–	V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI (Schmitt Trigger)	–	0.3Vdd	–	V
VOH1	Output High Voltage (Port 5)	IOH = -6 mA	4.5	–	–	V
VOH1	Output High Voltage (Port 6) (Schmitt Trigger)	IOH = -6 mA	4.5	–	–	V
VOL1	Output Low Voltage (Port 5)	IOL = 16.5 mA	–	–	0.5	V
VOL1	Output Low Voltage (Port 6) (Schmitt Trigger)	IOL = 16.5 mA	–	–	0.5	V
IPH	Pull-high current	Pull-high active, Input pin at VSS	-50	-70	-100	μA
IPD	Pull-down current	Pull-down active, Input pin at VDD	25	50	120	μA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ISB1	Power down current (VDD=5.0V)	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1	2	μA
ISB2	Power down current (VDD=5.0V)	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	6	10	μA
ICC1	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	20	30	μA
ICC2	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	22	32	μA
ICC3	Operating supply current (VDD=5.0V) at two cycles/two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	1.7	2.5	mA
ICC4	Operating supply current (VDD=5.0V) at two cycles/four clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	2.7	3.5	mA

Note: These parameters are theoretical values and have not been tested.

Ta=125°C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 3V	Two cycles with two clocks	DC	4	–	MHz
	Crystal: VDD to 5V	Two cycles with two clocks	DC	12	–	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	940	F±30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6 (Schmitt Trigger)	–	0.75Vdd	–	V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6 (Schmitt Trigger)	–	0.3Vdd	–	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt Trigger)	–	2.0	–	V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)	–	1.2	–	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI (Schmitt Trigger)	–	0.75Vdd	–	V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI (Schmitt Trigger)	–	0.3Vdd	–	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6 (Schmitt Trigger)	–	0.75Vdd	–	V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6 (Schmitt Trigger)	–	0.3Vdd	–	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt Trigger)	–	1.5	–	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt Trigger)	–	0.9	–	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI (Schmitt Trigger)	–	0.75Vdd	–	V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI (Schmitt Trigger)	–	0.3Vdd	–	V
VOH1	Output High Voltage (Port 5)	IOH = -4.8 mA	4.5	–	–	V
VOH1	Output High Voltage (Port 6) (Schmitt Trigger)	IOH = -4.8 mA	4.5	–	–	V
VOL1	Output Low Voltage (Port 5)	IOL = 10.3 mA	–	–	0.5	V
VOL1	Output Low Voltage (Port 6) (Schmitt Trigger)	IOL = 10.3 mA	–	–	0.5	V
IPH	Pull-high current	Pull-high active, Input pin at VSS	–45	–63	–90	μA
IPD	Pull-down current	Pull-down active, Input pin at VDD	22.5	45	108	μA
ISB1	Power down current (VDD=5.0V)	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.75	–	μA
ISB2	Power down current (VDD=5.0V)	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	–	10	μA
ICC1	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	–	30	μA
ICC2	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	–	32	μA
ICC3	Operating supply current (VDD=5.0V) at two cycles/two clocks	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	–	2.5	mA
ICC4	Operating supply current (VDD=5.0V) at two cycles/four clocks	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	–	3.5	mA

Note: These parameters are theoretical values and have not been tested.

Internal RC Electrical Characteristics (Ta=25°C, VDD=5 V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.84 MHz	4 MHz	4.16 MHz
8 MHz	25°C	5V	7.68 MHz	8 MHz	8.32 MHz
1 MHz	25°C	5V	0.96 MHz	1 MHz	1.04 MHz
455kHz	25°C	5V	437kHz	455kHz	473kHz

Internal RC Electrical Characteristics (Ta=-40 ~125°C, VDD=2.2~5.5 V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	-40°C ~125°C	2.2V~5.5V	3.3 MHz	4 MHz	4.56 MHz
8 MHz	-40°C ~125°C	2.2V~5.5V	6.6 MHz	8 MHz	9.12 MHz
1 MHz	-40°C ~125°C	2.2V~5.5V	0.825 MHz	1 MHz	1.14 MHz
455kHz	-40°C ~125°C	2.2V~5.5V	375kHz	455kHz	519kHz

8.2 AC Characteristics

Ta=25°C, VDD=5V ± 5%, VSS=0V

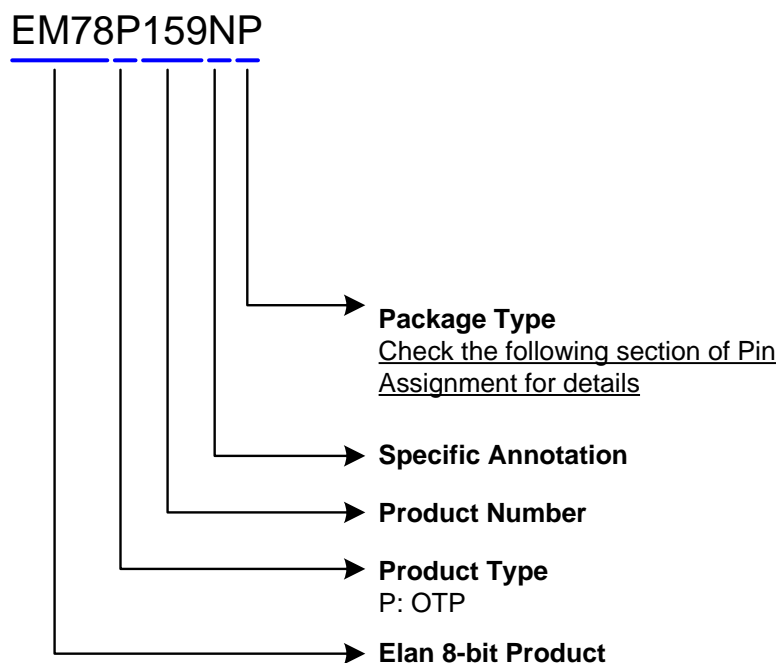
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

Note: These parameters are theoretical values and have not been tested.

* N = selected prescaler ratio

APPENDIX

A Ordering and Manufacturing Information

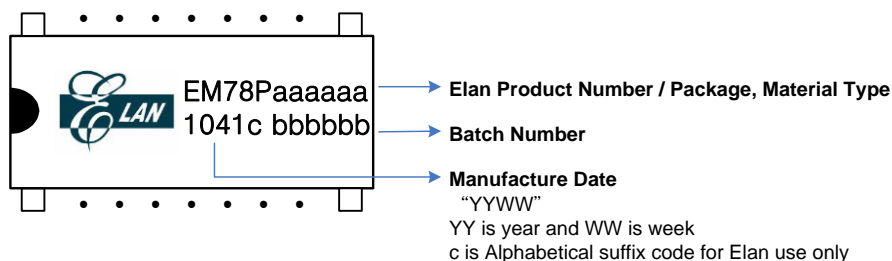


For example:

EM78P159NP

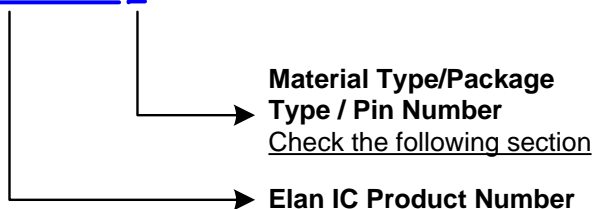
is EM78P159N with OTP program memory, product,
in 18-pin SOP 300mil package with Sony SS-00259 complied

IC Mark



Ordering Code

EM78P159NP



B Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P154NP	DIP	14	300 mil
EM78P154NM	SOP	14	150 mil
EM78P159NP	DIP	18	300 mil
EM78P159NM	SOP	18	300 mil

C Package Information

C.1 14-Lead Plastic Dual in-line (PDIP) — 300 mil

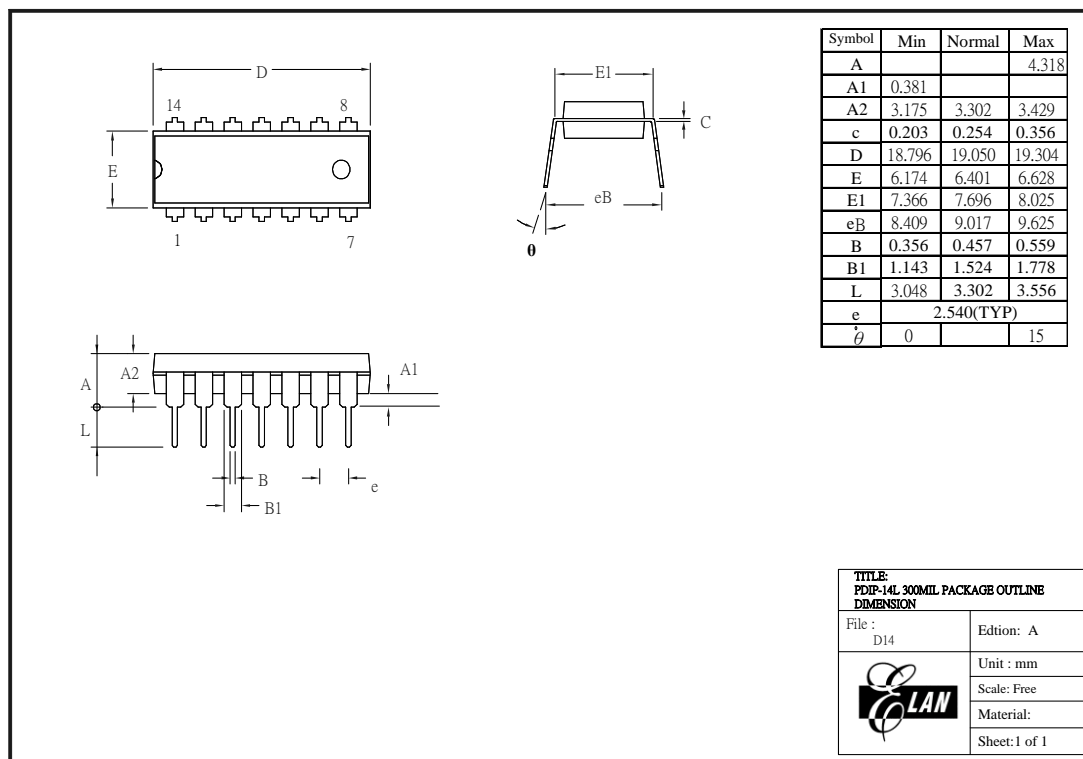


Figure B-1 EM78P154N 14-Lead PDIP Package Type

C.2 14-Lead Plastic Dual in line (SOP) — 150 mil

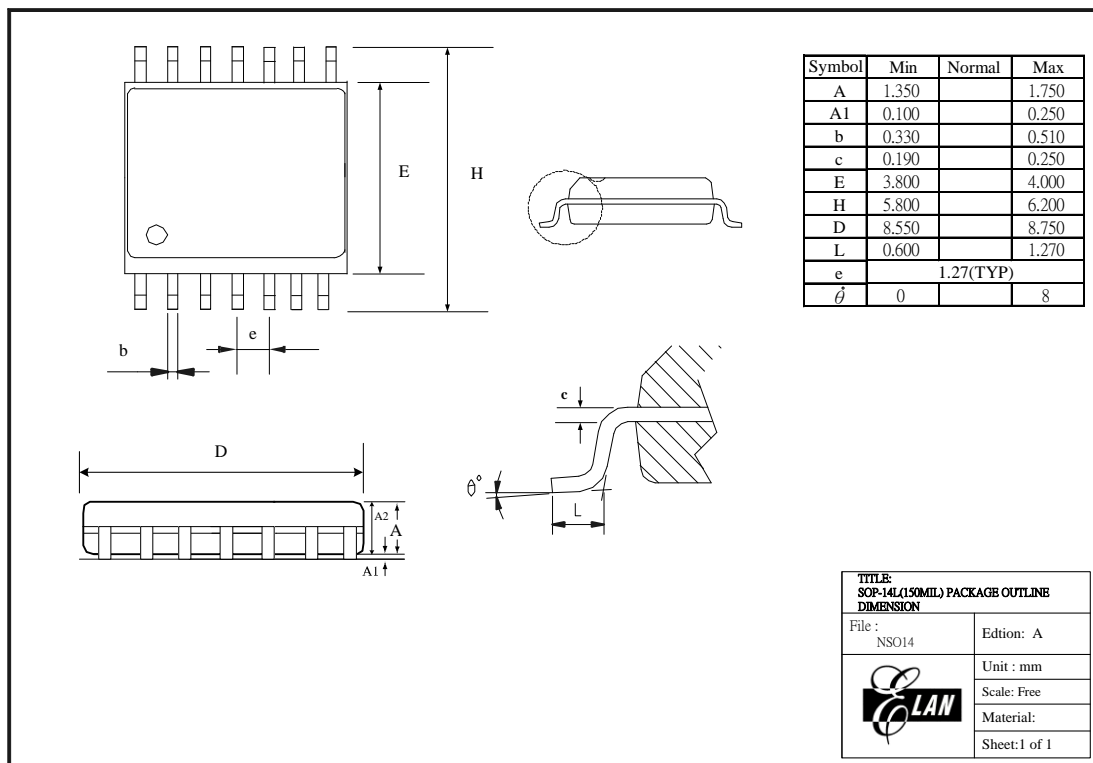


Figure B-2 EM78P154N 14-Lead SOP Package Type

C.3 18-Lead Plastic Dual in-line (PDIP) — 300 mil

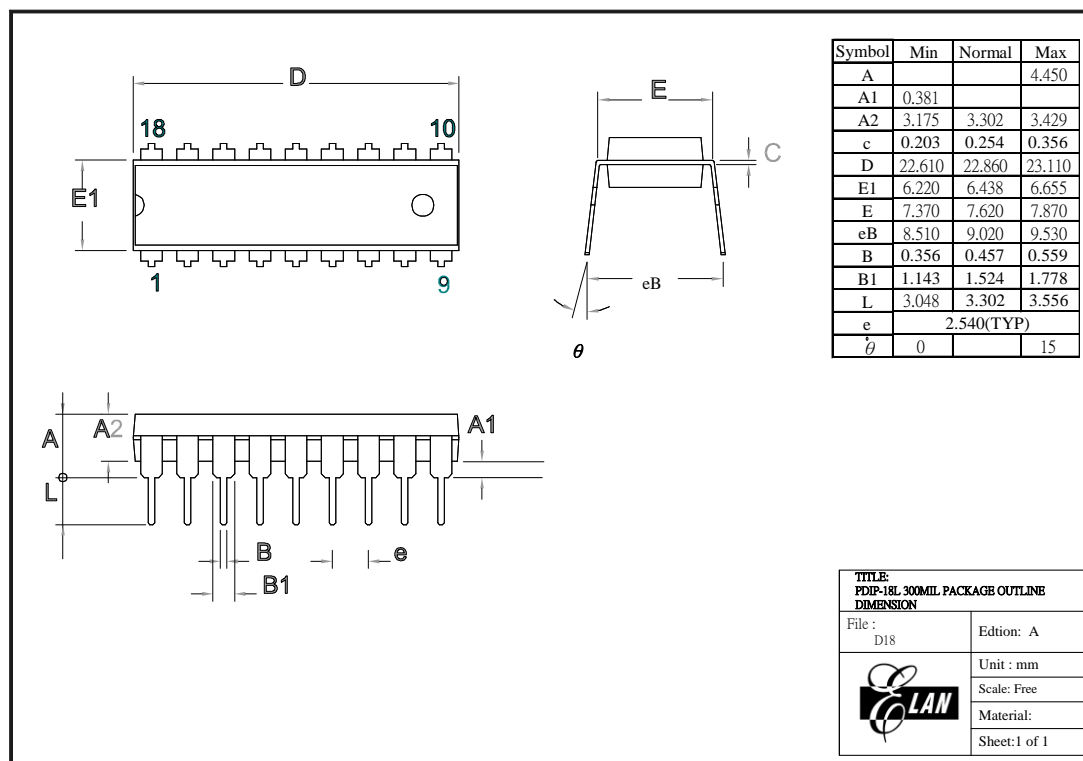


Figure B-3 EM78P159N 18-Lead PDIP Package Type

C.4 18-Lead Plastic Small Outline (SOP) — 300 mil

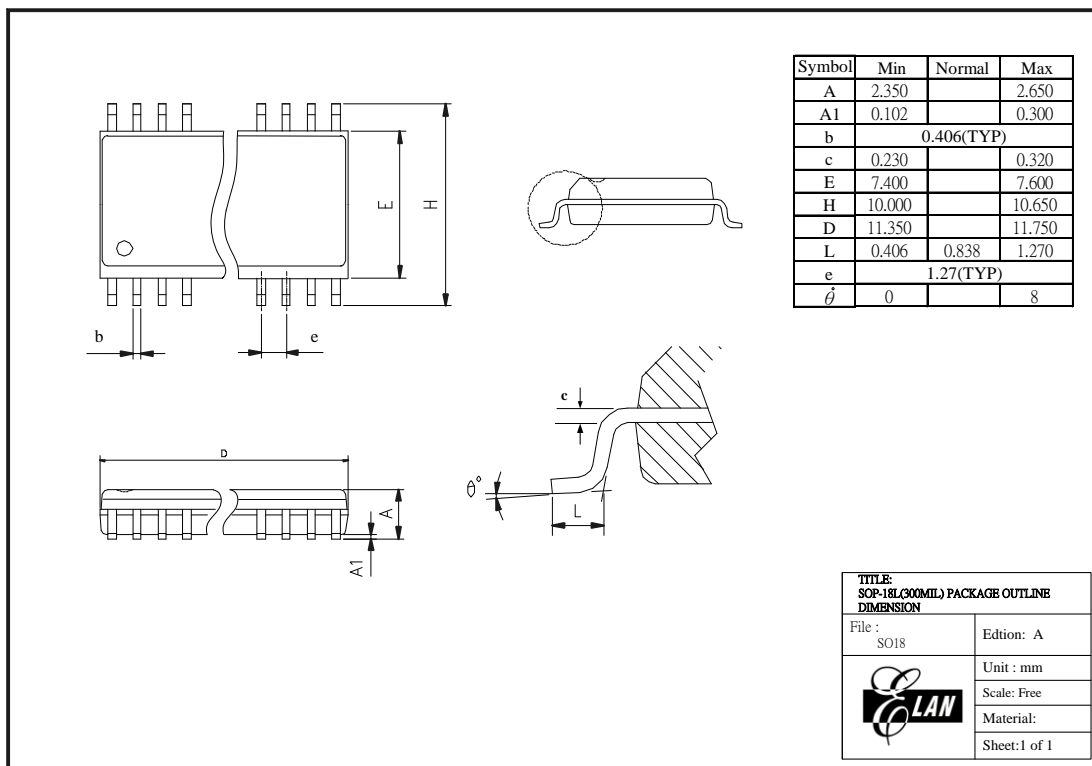


Figure B-4 EM78P159N 18-Lead SOP Package Type

D Quality Assurance and Reliability

D.1 Reliability Test

Test Category	Test Conditions	Remarks
Solderability	Solder temperature = $245 \pm 5^{\circ}\text{C}$ for 5 seconds up to the stopper using a rosin-type flux	—
Pre-condition	Step 1: TCT 65°C (15 mins) ~ 150°C (15 mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc.)
	Step 2: bake 125°C , TD (endurance) = 24 hrs	
	Step 3: soak $30^{\circ}\text{C}/60\%$, TD (endurance) = 192 hrs	
	Step 4: IR flow 3cycles (Pkg thickness $\geq 2.5\text{mm}$ or Pkg volume $\geq 350\text{ mm}^3$ -- $225 \pm 5^{\circ}\text{C}$) (Pkg thickness $\leq 2.5\text{mm}$ or Pkg volume $\leq 350\text{ mm}^3$ -- $240 \pm 5^{\circ}\text{C}$)	
Temperature cycle test	-65°C (15mins) ~ 150°C (15 mins), 200 cycles	—
Pressure cooker test	TA = 121°C , RH = 100%, pressure = 2 atm, TD (endurance) = 96 hrs	—
High temperature /high humidity test	TA = 85°C , RH = 85%, TD (endurance) = 168, 500 hrs	—
High-temperature storage life	TA = 150°C , TD (endurance) = 500, 1000 hrs	—
High-temperature operating life	TA = 125°C , VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	—
Latch-up	TA = 25°C , VCC = Max. operating voltage, 150mA/20V	—
ESD (HBM)	TA = 25°C , $\geq \pm 4\text{KV}$	IP_ND, OP_ND, IO_ND
ESD (MM)	TA = 25°C , $\geq \pm 400\text{V}$	IP_NS, OP_NS, IO_NS
		IP_PD, OP_PD, IO_PD, IP_PS, OP_PS, IO_PS, VDD_VSS (+) mode, VDD_VSS (-) mode

D.2 Power-on Reset and Vdd Voltage Drop/Rise Timing Test

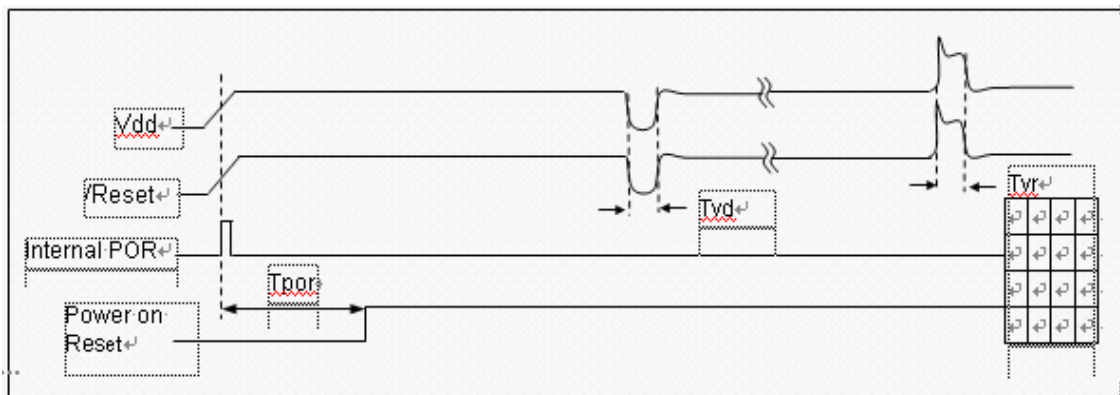


Figure C-1 EM78P159N series Power-on Reset and Vdd Voltage Drop/Rise Timing Test Timing Diagram

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tpor	Power-on reset time	Vdd = 5V, -40°C to 85°C	10.5	16.8	22	ms
Tvd*	Vdd Voltage drop time	Vdd = 5V, -40°C to 85°C	—	—	1	μs
Tvr**	Vdd Voltage rise time	Vdd = 5V, -40°C to 85°C	—	—	1	us

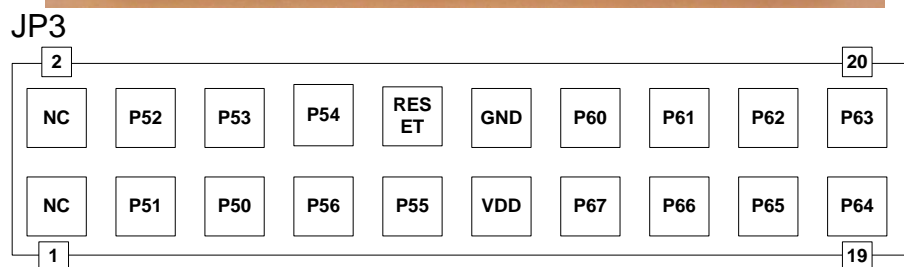
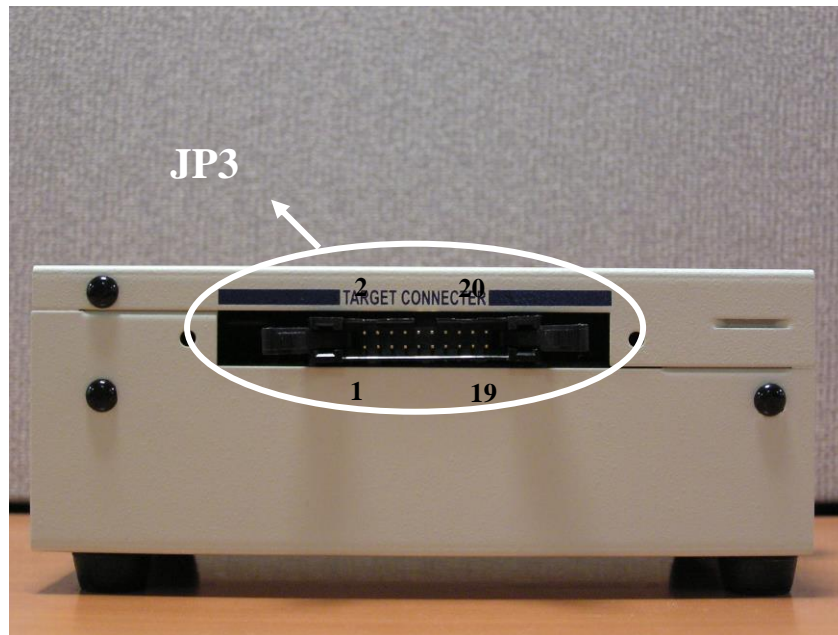
Note: * Tvd is the period of Vdd voltage lower than POR voltage.

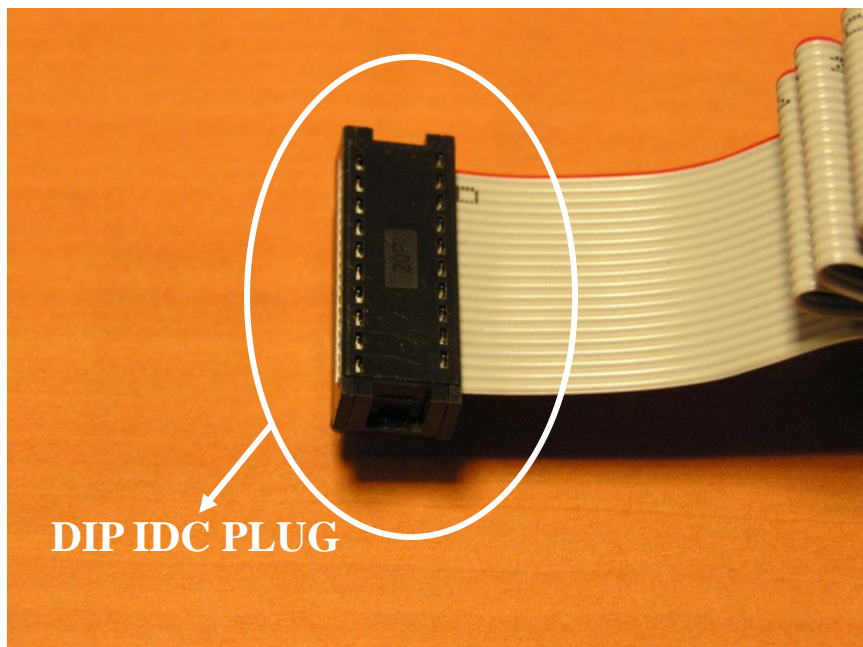
** Tvr is the period of Vdd voltage higher than 5.5V.

D.3 Address Trap Detect

An address trap detect is one of the fail-safe function that detects CPU malfunction caused by noise or the like. If the CPU attempts to fetch an instruction from a part of RAM, an internal recovery circuit will be auto started. Until CPU got the correct function, it will execute the next program.

E Interface of ICE159N





DIP IDC PLUG

