
EM78P418N

**8-Bit Microprocessor
with OTP ROM**

**Product
Specification**

DOC. VERSION 2.1

ELAN MICROELECTRONICS CORP.


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Contents

1	General Description	1
2	Feature	1
3	Pin Assignment	2
4	Pin Description	3
4.1	EM78P418ND18/SO18	3
4.2	EM78P418ND20/SO20	4
4.3	EM78P418NK24/SO24	5
5	Block Diagram	6
6	Function Description.....	7
6.1	Operational Registers	7
6.1.1	R0 (Indirect Address Register)	7
6.1.2	R1 (Time Clock/Counter).....	7
6.1.3	R2 (Program Counter) and Stack	7
6.1.3.1	Data Memory Configuration	9
6.1.4	R3 (Status Register)	10
6.1.5	R4 (RAM Select Register)	10
6.1.6	R5 ~ R7 (Port 5 ~ Port 7)	11
6.1.7	R8 (AISR: ADC Input Select Register)	11
6.1.8	R9 (ADCON: ADC Control Register).....	12
6.1.9	RA (ADOC: ADC Offset Calibration Register)	13
6.1.10	RB (ADDATA: Converted Value of ADC).....	14
6.1.11	RC (ADDATA1H: Converted Value of ADC)	14
6.1.12	RD (ADDATA1L: Converted Value of ADC).....	14
6.1.13	RE (WUCR: Wake-up Control Register)	14
6.1.14	RF (Interrupt Status Register)	16
6.1.15	R10 ~ R3F	16
6.2	Special Function Registers	17
6.2.1	A (Accumulator).....	17
6.2.2	CONT (Control Register).....	17
6.2.3	IOC50 ~ IOC70 (I/O Port Control Register)	18
6.2.4	IOC80 (PWMCON: PWM Control Register).....	18
6.2.5	IOC90 (TMRCON: Timer Control Register).....	19
6.2.6	IOCA0 (CMPCON: Comparator Control Register)	20
6.2.7	IOCB0 (Pull-down Control Register)	20
6.2.8	IOCC0 (Open-drain Control Register).....	21
6.2.9	IOCD0 (Pull-high Control Register).....	21
6.2.10	IOCE0 (WDT Control Register).....	22
6.2.11	IOCF0 (Interrupt Mask Register).....	23
6.2.12	IOC51 (PRD1: PWM1 Time Period).....	24

6.2.13	IOC61 (PRD2: PWM2 Time Period)	24
6.2.14	IOC71 (PRD3: PWM3 Time Period)	24
6.2.15	IOC81 (DT1L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM1 Duty Cycle)	24
6.2.16	IOC91 (DT2L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM2 Duty Cycle)	24
6.2.17	IOCA1 (DT3L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM3 Duty Cycle)	24
6.2.18	IOCB1 (DTH: Most Significant Bits of PWM Duty Cycle)	24
6.2.19	IOCC1 (TMR1L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM1 Timer)	24
6.2.20	IOCD1 (TMR2L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM2 Timer)	25
6.2.21	IOCE1 (TMR3L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM3 Timer)	25
6.2.22	IOCF1 (TMRH: Most Significant Bits of the PWM Timer)	25
6.3	TCC/WDT and Prescaler	25
6.4	I/O Ports	26
6.4.1	Usage of Port 6 Input Change Wake-up/Interrupt Function	29
6.5	Reset and Wake-up	29
6.5.1	Reset and Wake-up Operation	29
6.5.1.1	Wake-up and Interrupt Modes Operation Summary	32
6.5.1.2	Register Initial Values after Reset	33
6.5.1.3	Controller Reset Block Diagram	38
6.5.2	T and P Status in the Status Register	39
6.6	Interrupt	39
6.7	Analog-to-Digital Converter (ADC)	41
6.7.1	ADC Control Register (AISR/R8, ADCON/R9, ADOC/RA)	41
6.7.1.1	R8 (AISR: ADC Input Select Register)	41
6.7.1.2	R9 (ADCON: ADC Control Register)	43
6.7.1.3	RA (ADOC: ADC Offset Calibration Register)	44
6.7.2	ADC Data Register (ADDATA/RB, ADDATA1H/RC, ADDATA1L/RD)	44
6.7.3	ADC Sampling Time	45
6.7.4	AD Conversion Time	45
6.7.5	ADC Operation during Sleep Mode	45
6.7.6	Programming Process/Considerations	46
6.7.6.1	Programming Process	46
6.7.6.2	Sample Demo Programs	46
6.8	PWM (Pulse Width Modulation)	48
6.8.1	Overview	48
6.8.2	Increment Timer Counter	49
6.8.3	PWM Time Period	49
6.8.4	PWM Duty Cycle	50
6.8.5	Comparator X	50
6.8.6	PWM Programming Process/Steps	50

6.9	Timer	50
6.9.1	Overview	50
6.9.2	Function Description.....	51
6.9.3	Programming the Related Registers	52
6.9.3.1	Related Control Registers of TMR1, TMR2, and TMR3	52
6.9.4	Timer Programming Process/Steps.....	52
6.10	Comparator.....	52
6.10.1	External Reference Signal	53
6.10.2	Comparator Output.....	53
6.10.3	Using a Comparator as an Operation Amplifier	54
6.10.4	Comparator Interrupt.....	54
6.10.5	Wake-up from Sleep Mode.....	54
6.11	Oscillator.....	54
6.11.1	Oscillator Modes.....	54
6.11.2	Crystal Oscillator/Ceramic Resonators (Crystal).....	55
6.11.3	External RC Oscillator Mode.....	56
6.11.4	Internal RC Oscillator Mode	57
6.12	Power-on Considerations.....	57
6.12.1	External Power-on Reset Circuit	58
6.12.2	Residual Voltage Protection	58
6.13	Code Option	59
6.13.1	Code Option Register (Word 0).....	59
6.13.2	Code Option Register (Word 1).....	60
6.13.3	Customer ID Register (Word 2).....	61
6.14	Instruction Set.....	62
7	Absolute Maximum Ratings.....	64
8	DC Electrical Characteristics.....	64
8.1	AD Converter Characteristics.....	66
8.2	Comparator (OP) Characteristics	67
8.3	Device Characteristics	67
9	AC Electrical Characteristics	68
10	Timing Diagrams	69

APPENDIX

A	Ordering and Manufacturing Information	70
B	Package Type	72
C	Package Information	73
	C.1 EM78P418ND18.....	73
	C.2 EM78P418NSO18	74
	C.3 EM78P418ND20.....	75
	C.4 EM78P418NSO20	76
	C.5 EM78P418NK24	77
	C.6 EM78P418NSO24	78
	C.7 EM78P418NSS24.....	79
D	EM78P418N Program Pin	80
E	Quality Assurance and Reliability	81
	E.1 Address Trap Detect	81

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial official version	2005/06/23
1.1	Added the IRC drift rate in the Features section	2006/01/06
1.2	Added the EM78P418NAM SSOP 20-pin package	2006/02/22
1.3	Revised RE, RF, and IOCF0 registers contents	2006/06/01
1.4	1. Modified the General Description, Pin Assignment and Features sections 2. Added Green Product Information 3. Modified the Functional Block Diagram	2006/10/02
1.5	Deleted the EM78P418NAM SSOP 20-pin package.	2007/11/13
1.6	Modified the package type name	2007/12/11
1.7	1. Added the EM78P418NSS24 SSOP 24-pin package 2. Added EM78P418N Program Pin	2008/08/20
1.8	Modified Appendix C <i>EM78P418N Program Pin diagram</i>	2010/02/03
1.9	Fixed HLP to "0" at Bit 3 of Code Option Word 0.	2011/01/18
2.0	Added back "HLP" for more function selection.	2011/09/29
2.1	Added Appendix A for Ordering and Manufacturing Information	2016/04/06

1 General Description

The EM78P418N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. This device has an on-chip 4K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides Protection bits to prevent intrusion of user's code in the OTP memory as well as from unwanted external accesses. Three Code Option bits are also available to meet user's application requirements.

With its enhanced OTP-ROM features, the EM78P418N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Feature

- CPU configuration
 - 4K×13 bits on-chip ROM
 - 144×8 bits on-chip registers (SRAM)
 - 8 level stacks for subroutine nesting
 - Less than 2.2 mA at 5V/4 MHz
 - Typically 15 μ A, at 3V/32kHz
 - Typically 1 μ A, during sleep mode
- I/O port configuration
 - 3 bi-directional I/O ports
 - Wake-up port : P6
 - 8 Programmable pull-down I/O pins
 - 8 programmable pull-high I/O pins
 - 8 programmable open-drain I/O pins
 - External interrupt : P50
- Operating voltage range:
 - 2.3V~5.5V at 0°C~70°C (commercial)
 - 2.5V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (base on 2 clocks):
 - Crystal mode: DC ~ 20 MHz, 5V; DC ~ 8 MHz, 3V
 - ERC mode: DC ~ 16 MHz, 5V; DC ~ 4 MHz, 3V
 - IRC mode: 4 MHz at 2.3V~5.5V
- Fast set-up time requires only 2ms in high Crystal and 32 CLKS in IRC mode from wake up to operating mode
- Peripheral configuration
 - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
 - 8-bit multi-channel Analog-to-Digital Converter with 12-bit resolution in Vref mode
 - Three Pulse Width Modulation (PWM) with 10-bit resolution
 - One pair of comparator (can be set as an OP)
 - Power-down (Sleep) mode
- Six available interrupts
 - TCC overflow interrupt
 - Input-port status changed interrupt (wake-up from sleep mode)
 - External interrupt
 - ADC completion interrupt
 - PWM period match completion
 - Comparator high/low interrupt
- Programmable free running watchdog timer
- Power-on voltage detector provided (2.0V+0.1V)
- Package types:
 - 18-pin DIP 300mil : EM78P418ND18
 - 18-pin SOP 300mil : EM78P418NSO18
 - 20-pin DIP 300mil : EM78P418ND20
 - 20-pin SOP 300mil : EM78P418NSO20
 - 24-pin skinny DIP 300mil:EM78P418NK24
 - 24-pin SOP 300mil : EM78P418NSO24
 - 24-pin SSOP 150mil :EM78P418NSS24

Internal RC Frequency	Drift Rate			
	Temperature (-40°C+85°C)	Voltage (2.3V~5.5V)	Process	Total
4MHz	±10%	±5%	±4%	±19%
8MHz	±10%	±6%	±4%	±20%
1MHz	±10%	±5%	±4%	±19%
455kHz	±10%	±5%	±4%	±19%

- All these four main frequencies can be trimmed by programming with four calibrated bits in the ICE418N Simulator. OTP is auto trimmed by ELAN Writer.

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Assignment

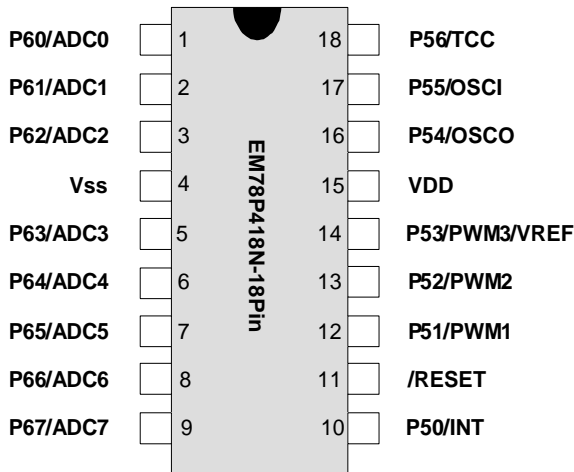


Figure 3-1 EM78P418ND18/SO18

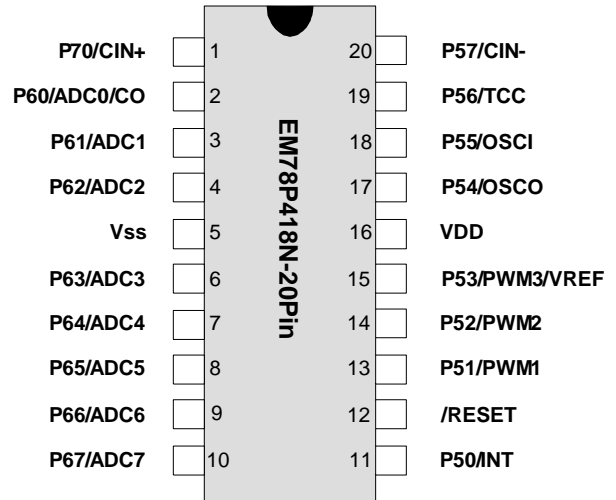


Figure 3-2 EM78P418ND20/SO20

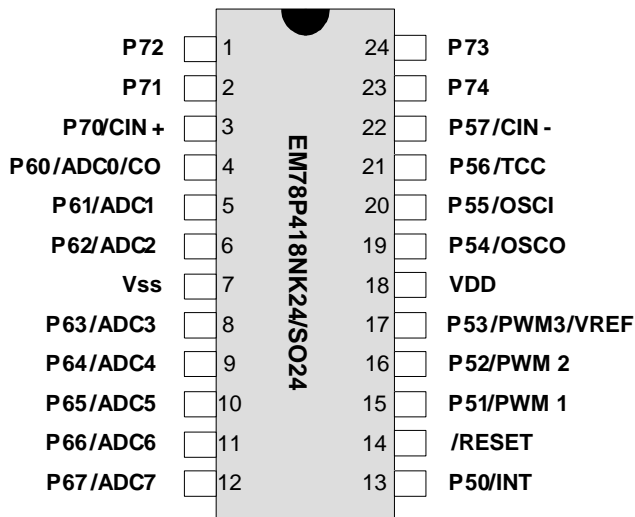


Figure 3-3 EM78P418NK24/SO24

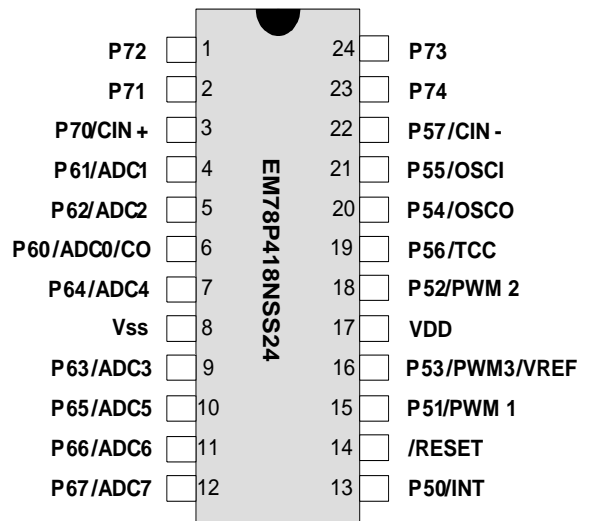


Figure 3-4 EM78P418NSS24

4 Pin Description

4.1 EM78P418ND18/SO18

Symbol	Pin No.	Type	Function
VDD	15	–	Power supply
OSCI	17	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	16	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin RC type: Clock output with a duration one instruction cycle. The prescaler is determined by the CONT register. External clock signal input
P60 ~ P67	1 ~ 3 5 ~ 9	I/O	General-purpose I/O pin Default value at power-on reset
P50 ~ P56	10, 12~14, 16 ~ 18	I/O	General-purpose I/O pin Default value at power-on reset
INT	10	I	External interrupt pin triggered by a falling or rising edge
ADC0 ~ ADC7	1 ~ 3 5 ~ 9	I	Analog-to-Digital Converter Defined by ADCON (R9) <0:2>
PWM1 PWM2 PWM3	12, 13, 14	O	Pulse width modulation outputs Defined by PWMCON (IOC80) <5:7>
VREF	14	I	External reference voltage for ADC Defined by ADCON (R9) <7>
/RESET	11	I	General purpose input only. If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET must not exceed V _{dd} during normal mode.
TCC	18	I	Real time clock/counter with Schmitt trigger input pin. It must be tied to VDD or VSS if not in use.
VSS	5	–	Ground

4.2 EM78P418ND20/SO20

Symbol	Pin No.	Type	Function
VDD	16	–	Power supply
OSCI	18	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	17	O	Crystal type: Output terminal for crystal oscillator or external clock input pin RC type: Clock output with a duration of one instruction cycle time. The prescaler is determined by the CONT register. External clock signal input
P50 ~ P57	11,13~15 17 ~ 20,	I/O	General-purpose I/O pin Default value at power-on reset
P60 ~ P67	2 ~ 4, 6 ~ 10	I/O	General-purpose I/O pin Default value at power-on reset
P70	1	I/O	General-purpose I/O pin Default value at power-on reset
INT	11	I	External interrupt pin triggered by falling edge or rising edge.
ADC0~ADC7	2 ~ 4, 6 ~ 10	I	Analog to Digital Converter Defined by ADCON (R9) <0:2>
PWM1 PWM2 PWM3	13, 14, 15	O	Pulse width modulation outputs Defined by PWMCON (IOC80) <5:7>
VREF	15	I	External reference voltage for ADC Defined by ADCON (R9) <7>
CIN- CIN+ CO	20 1 2	I I O	“–” → the input pin of Vin– of the comparator “+” → the input pin of Vin+ of the comparator Pin CO is the output of the comparator Defined by CMPCON (IOCA0) <0:1>
/RESET	12	I	General-purpose Input only If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET must not exceed Vdd during normal mode.
TCC	19	I	Real time clock/counter with Schmitt trigger input pin. It must be tied to VDD or VSS if not in use.
VSS	5	–	Ground

4.3 EM78P418NK24/SO24

Symbol	Pin No.	Type	Function
VDD	18	-	Power supply
OSCI	20	I	Crystal type:Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	19	O	Crystal type:Output terminal for crystal oscillator or external clock input pin RC type:Clock output with a duration of one instruction cycle time. The prescaler is determined by the CONT register. External clock signal input
P50 ~ P57	13, 15 ~ 17 19 ~ 22,	I/O	General-purpose I/O pin Default value at power-on reset
P60 ~ P67	4 ~ 6, 8 ~ 12	I/O	General-purpose I/O pin Default value at power-on reset
P70 ~ P74	3, 2, 1, 24, 23	I/O	General-purpose I/O pin Default value at power-on reset
INT	13	I	External interrupt pin triggered by a falling edge or rising edge.
ADC0 ~ADC7	4 ~ 6, 8 ~ 12	I	Analog-to-Digital Converter Defined by ADCON (R9) <0:2>
PWM1 PWM2 PWM3	15, 16, 17	O	Pulse width modulation outputs Defined by PWMCON (IOC80) <5:7>
VREF	17	I	External reference voltage for ADC Defined by ADCON (R9)<7>
CIN- CIN+ CO	22, 3, 4	I I O	"-" → input pin of Vin- of a comparator "+" → input pin of Vin+ of a comparator Pin CO is the comparator output Defined by CMPCON (IOCA0) <0:1>
/RESET	14	I	General-purpose Input only If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET must not exceed Vdd during normal mode.
TCC	21	I	Real time clock/counter with Schmitt trigger input pin. It must be tied to VDD or VSS if not in use.
VSS	7	-	Ground

5 Block Diagram

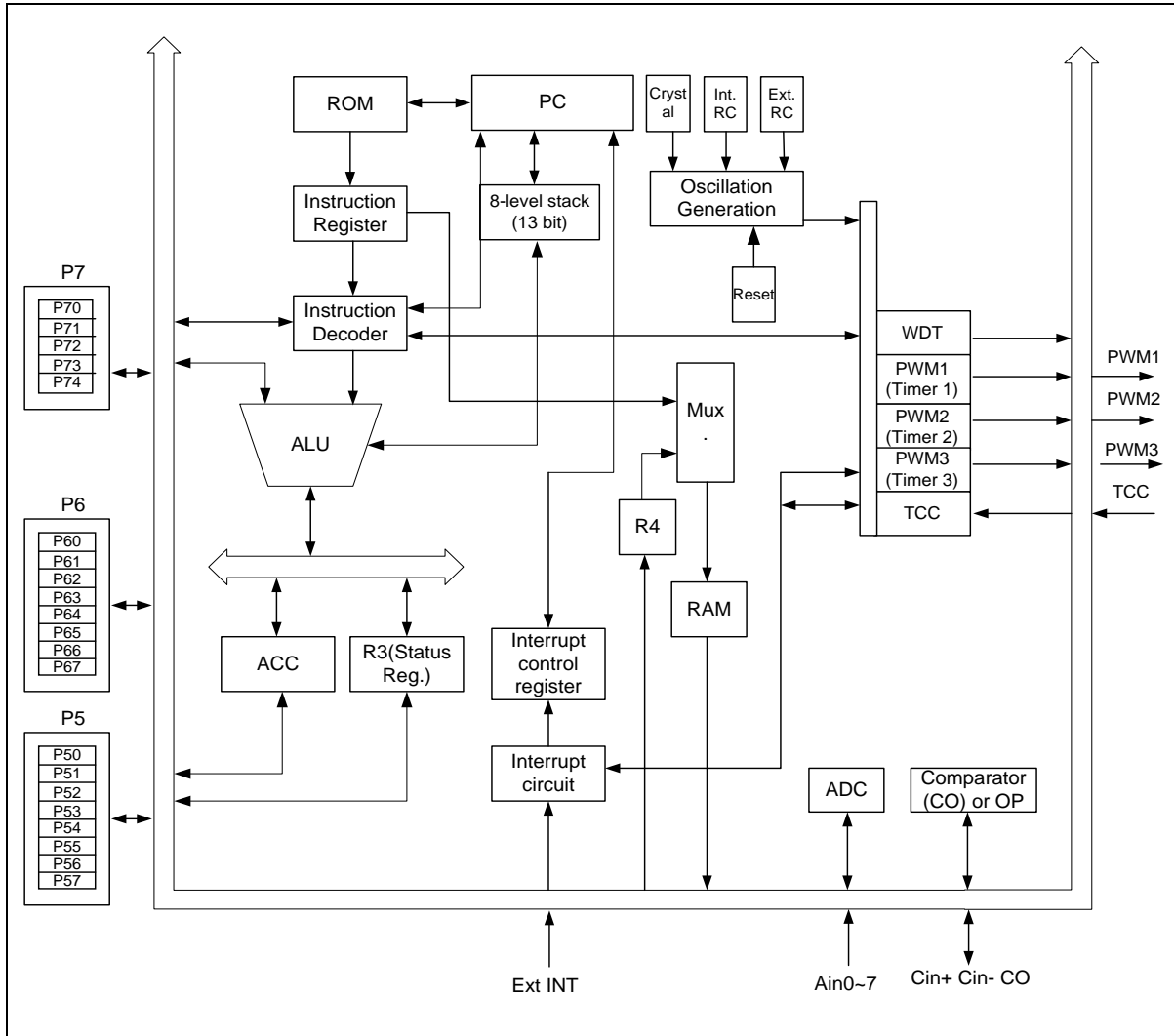


Figure 5-1 EM78P418N Block Diagram

6 Function Description

6.1 Operational Registers

6.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1 (Time Clock/Counter)

R1 is incremented by an external signal edge through the TCC pin, or by the instruction cycle clock.

- External signal of TCC trigger pulse width must be greater than one instruction.
- The signals to increase the counter are determined by Bit 4 and Bit 5 of the CONT register.
- Writable and readable as any other registers.

6.1.3 R2 (Program Counter) and Stack

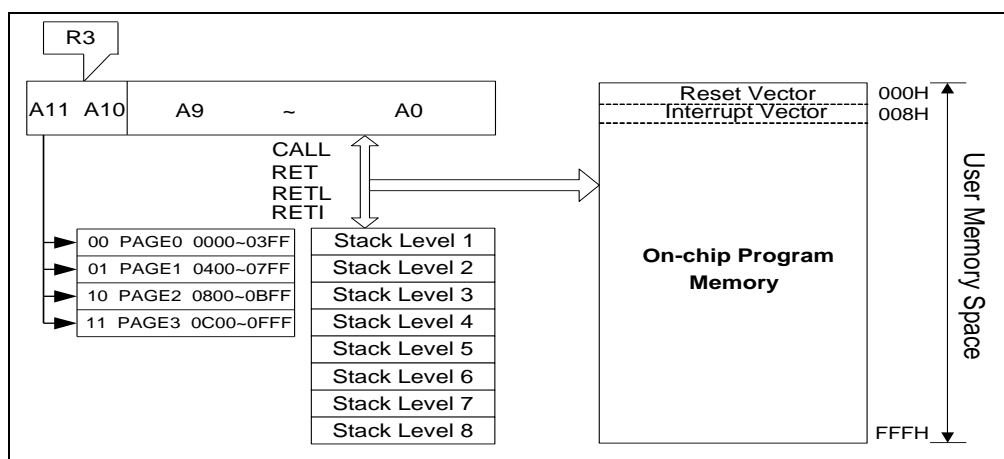


Figure 6-1 Program Counter Organization

- R2 and hardware stacks are 12-bit wide. The structure is depicted in the table under Section 6.1.3.1 *Data Memory Configuration*.
- The configuration structure generates 4K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are all set to "0"s when a reset condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.



- "CALL" instruction loads the lower 10 bits of the PC and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction (except "ADD R2,A") that is written to R2 (e.g., "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- In the case of EM78P418N, the most two significant bits (A11 and A10) will be loaded with the content of PS1 and PS0 in the status register (R3) upon execution of a "JMP", "CALL", or any other instructions set which write to R2.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instructions that are written to R2. Note that these instructions need one or two instructions cycle as determined by Code Option Register CYES bit.

6.1.3.1 Data Memory Configuration

Address	Page Registers				IOC Page Registers				IOC Page Registers			
00	R0 (Indirect Addressing Register)				Reserve				Reserve			
01	R1 (Time Clock Counter)				Reserve				Reserve			
02	R2 (Program Counter)				Reserve				Reserve			
03	R3 (Status Register)				Reserve				Reserve			
04	R4 (RAM Select Register)				Reserve				Reserve			
05	R5 (Port 5)				IOC50 (I/O Port Control Register)				IOC51 (PRD1: PWM1 time period)			
06	R6 (Port 6)				IOC60 (I/O Port Control Register)				IOC61 (PRD2: PWM2 time period)			
07	R7 (Port 7)				IOC70 (I/O Port Control Register)				IOC71 (PRD3: PWM3 time period)			
08	R8 (ADC Input Select Register)				IOC80 (PWM Control Register)				IOC81 (DT1L: PWM1 D uty cycle)			
09	R9 (ADC Control Register)				IOC90 (Timer Control Register)				IOC91 (DT2L: PWM2 Duty cycle)			
0A	RA (ADC Offset Calibration Register)				IOCA0 (Comparator Control Register)				IOCA1 (DT3L: PWM3 Duty cycle)			
0B	RB (ADDA1H: ADC data Bit 11 ~ Bit 4)				IOCB0 (Pull-down Control Register)				IOCB1 (DTH: PWM Duty cycle)			
0C	RC (ADDA1H: ADC data Bit 11 ~ Bit 8)				IOCC0 (Open-drain Control Register)				IOCC1 (TIMER1L: PWM1 timer)			
0D	RD (ADDA1L: ADC data Bit 7 ~ Bit 0)				IOCD0 (Pull-high Control Register)				IOCD1 (TIMER2L: PWM2 timer)			
0E	RE (Wake-up Control Register)				IOCE0 (WDT Control Register)				IOCE1 (TIMER3L: PWM3 timer)			
0F	RF (Interrupt Status Register)				IOCF0 (Interrupt Mask Register)				IOCF1 (TMRH: PWM timer)			
10 : 1F	General Registers											
20 : 3F	Bank 0	Bank 1	Bank 2	Bank 3								



6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCS	PS1	PS0	T	P	Z	DC	C

Bit 7 (IOCS): Select the Segment of IO control register.

0: Segment 0 (IOC50 ~ IOCF0) selected

1: Segment 1 (IOC51 ~ IOCF1) selected

Bit 6 ~ Bit 5 (PS1 ~ PS0): Page select bits. PS0 ~ PS1 are used to select a program memory page. When executing a "JMP," "CALL," or other instructions which cause the program counter to change (e.g., MOV R2, A), PS0 ~ PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will always be back to the page from where the subroutine was called regardless of the current PS0 ~ PS1 bits setting.

PS1	PS0	Program Memory Page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

Bit 4 (T): Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands, or during power on, and Reset to 0 by WDT time-out.

Bit 3 (P): Power-down bit. Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

NOTE

Bit 4 and Bit 3 (T and P) are read only.

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7 and Bit 6: used to select Banks 0 ~ 3.

Bit 5 ~ Bit 0: used to select registers (Address: 00 ~ 3F) in indirect addressing mode.

See the table under Section 6.1.3.1 *Data Memory Configuration*.

6.1.6 R5 ~ R7 (Port 5 ~ Port 7)

R5 and R6 are I/O registers.

R7 is an I/O register. The upper three bits of R7 are fixed at 0.

6.1.7 R8 (AISR: ADC Input Select Register)

The AISR register defines the Port 6 pins individually as analog input or as digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P67 pin

- 0: Disable ADC7, P67 is configured as I/O pin
- 1: Enable ADC7 which is configured as analog input pin

Bit 6 (ADE6): AD converter enable bit of P66 pin

- 0: Disable ADC6, P66 is configured as I/O pin
- 1: Enable ADC6 which is configured as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin

- 0: Disable ADC5, P65 is configured as I/O pin
- 1: Enable ADC5 which is configured as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin

- 0: Disable ADC4, P64 is configured as I/O pin
- 1: Enable ADC4 which is configured as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin

- 0: Disable ADC3, P63 is configured as I/O pin
- 1: Enable ADC3 which is configured as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin

- 0: Disable ADC2, P62 is configured as I/O pin
- 1: Enable ADC2 which is configured as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

- 0: Disable ADC1, P61 is configured as I/O pin
- 1: Enable ADC1 which is configured as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin

- 0: Disable ADC0, P60 is configured as I/O pin
- 1: Enable ADC0 which is configured as analog input pin

NOTE

Take Note of the pin priority of the COS1 and COS0 bits of IOCA0 Control register when P60/ADC0 is configured as analog input or as digital I/O. The Comparator/OP select bits are as shown in a table under Section 6.2.6, IOCA0 (CMPCON: Comparator Control Register).

The P60/ADC0/CO pin priority is as follows:

P60/ADE0/CO Priority		
High	Medium	Low
CO	ADC0	P60

6.1.8 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of the Vref of the ADC

0: The Vref of the ADC is connected to Vdd (default value), and the P53/VREF pin carries out the function of P53

1: The Vref of the ADC is connected to P53/VREF

NOTE

The P53/PWM3/VREF pin cannot be applied to PWM3 and VREF at the same time. If P53/PWM3/VREF is configured as VREF analog input pin, then PWM3E must be "0".

The P53/PWM3/VREF pin priority is as follows:

P53/PWM3/VREF Pin Priority		
High	Medium	Low
VREF	PWM3	P53

Bit 6 and Bit 5 (CKR1 and CKR0): Prescaler of the oscillator clock rate of ADC

00 = 1: 16 (default value)

01 = 1: 4

10 = 1: 64

11 = 1: WDT ring oscillator frequency

CKR1 : CKR0	Operation Mode	Max. Operating Frequency
00	Fosc/16	4 MHz
01	Fosc/4	1 MHz
10	Fosc/64	16 MHz
11	Internal RC (WDT time base)	–

Bit 4 (ADRUN): ADC starts to RUN

0: Reset upon completion of the conversion. This bit **cannot** be reset by software.

1: an AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to save power even while the CPU is operating

1: ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

000 = ADIN0/P60

001 = ADIN1/P61

010 = ADIN2/P62

011 = ADIN3/P63

100 = ADIN4/P64

101 = ADIN5/P65

110 = ADIN6/P66

111 = ADIN7/P67

These bits can only be changed when the ADIF bit (see Section 6.1.14) and the ADRUN bit are both low.

6.1.9 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	"0"	"0"	"0"

Bit 7 (CALI): Calibration enable bit for ADC offset

0: Calibration disabled

1: Calibration enabled

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P418N	ICE418N
0	0	0	0LSB	0LSB
0	0	1	2LSB	1LSB
0	1	0	4LSB	2LSB
0	1	1	6LSB	3LSB
1	0	0	8LSB	4LSB
1	0	1	10LSB	5LSB
1	1	0	12LSB	6LSB
1	1	1	14LSB	7LSB

Bit 2 ~ Bit 0: Unimplemented, read as '0'

6.1.10 RB (ADDATA: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

When the AD conversion is completed, the result is loaded into the ADDATA. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14) is set.

RB is read only.

6.1.11 RC (ADDATA1H: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	AD11	AD10	AD9	AD8

When the AD conversion is completed, the result is loaded into the ADDATA1H. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14) is set.

RC is read only.

6.1.12 RD (ADDATA1L: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

When the AD conversion is completed, the result is loaded into the ADDATA1L. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14) is set.

RD is read only.

6.1.13 RE (WUCR: Wake-up Control Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EM78P418N	"0"	"0"	"0"	"0"	ADWE	CMPWE	ICWE	"0"
ICE418N Simulator	C3	C2	C1	C0	ADWE	CMPWE	ICWE	"0"

Bit 7 ~ Bit 4: [For EM78P418N]: Unimplemented, read as '0'

[With Simulator (C3~C0)]: IRC calibration bits in IRC oscillator mode. For ICE418N simulator, these are the IRC calibration bits in IRC oscillator mode.

C3	C2	C1	C0	Frequency (MHz)
0	0	0	0	(1-36%) x F
0	0	0	1	(1-31.5%) x F
0	0	1	0	(1-27%) x F
0	0	1	1	(1-22.5%) x F
0	1	0	0	(1-18%) x F
0	1	0	1	(1-13.5%) x F
0	1	1	0	(1-9%) x F
0	1	1	1	(1-4.5%) x F
1	1	1	1	F (default)
1	1	1	0	(1+4.5%) x F
1	1	0	1	(1+9%) x F
1	1	0	0	(1+13.5%) x F
1	0	1	1	(1+18%) x F
1	0	1	0	(1+22.5%) x F
1	0	0	1	(1+27%) x F
1	0	0	0	(1+31.5%) x F

NOTE

1. Frequency values shown are theoretical and taken from an instance of a high frequency mode. Hence these are shown for reference only. Definite values will depend on the actual process.
2. Similar way of calculation is also applicable to low frequency mode.

Bit 3 (ADWE): ADC wake-up enable bit

- 0:** Disable ADC wake-up
- 1:** Enable ADC wake-up

When the ADC Complete status is used to wake-up the EM78P418N from sleep with AD conversion running, the ADWE bit must be set to "Enable".

Bit 2 (CMPWE): Comparator wake-up enable bit

- 0:** Disable Comparator wake-up
- 1:** Enable Comparator wake-up

When the Comparator output status change is used to wake-up the EM78P418N from sleep, the CMPWE bit must be set to "Enable".

Bit 1 (ICWE): Port 6 input change to wake-up status enable bit

- 0:** Disable Port 6 input change to wake-up status
- 1:** Enable Port 6 input change wake-up status

When the Port 6 Input Status Change is used to wake-up the EM78P418N from sleep, the ICWE bit must be set to "Enable".

Bit 0: Not implemented, read as '0'

6.1.14 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIF	PWM3IF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF

NOTE

- "1" means with interrupt request; "0" means no interrupt occurs.
- RF can be cleared by instruction but cannot be set.
- IOCF0 is the interrupt mask register.
- Reading RF will result to "logic AND" of RF and IOCF0.

Bit 7 (CMPIF): Comparator interrupt flag. Set when a change occurs in the Comparator output. Reset by software.

Bit 6 (PWM3IF): PWM3 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached. Reset by software.

Bit 5 (PWM2IF): PWM2 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached. Reset by software.

Bit 4 (PWM1IF): PWM1 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached. Reset by software.

Bit 3 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed. Reset by software.

Bit 2 (EXIF): External interrupt flag. Set by falling edge on /INT pin. Reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes. Reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

6.1.15 R10 ~ R3F

All of these are 8-bit general-purpose registers.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

- 0: interrupt occurs at a rising edge on the INT pin
- 1: interrupt occurs at a falling edge on the INT pin

Bit 6 (INT): Interrupt enable flag

- 0: masked by DISI or hardware interrupt
- 1: enabled by the ENI/RETI instructions

This bit is readable only.

Bit 5 (TS): TCC signal source

- 0: internal instruction cycle clock. If P56 is used as I/O pin, TS must be 0.
- 1: transition on the TCC pin

Bit 4 (TE): TCC signal edge

- 0: increment if the transition from low to high takes place on the TCC pin
- 1: increment if the transition from high to low takes place on the TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

- 0: prescaler disable bit. TCC rate is 1:1.
- 1: prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

NOTE

Tcc time-out period [1/Fosc x prescaler x 256 (Tcc cnt) x 1 (CLK=2)]
Tcc time-out period [1/Fosc x prescaler x 256 (Tcc cnt) x 2 (CLK=4)]



6.2.3 IOC50 ~ IOC70 (I/O Port Control Register)

- 0: defines the relative I/O pin as output
- 1: sets the relative I/O pin into high impedance

IOC50, IOC60, and IOC70 registers are all readable and writable.

NOTE

Using EM78P418N-18Pin and EM78P418N-20Pin type, Bit 9 of the Code Option Register (Word 0) must be set to "1". Using EM78P418N-18Pin type, user must set the extra Bit 7 of IOC50 and Bit 0 of IOC70 to "0". Then set the pin status to "0". This will have no additional power consumption.

6.2.4 IOC80 (PWMCON: PWM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3E	PWM2E	PWM1E	"0"	T1EN	T1P2	T1P1	T1P0

Bit 7 (PWM3E): PWM3 enable bit

- 0: PWM3 is off (default value), and its related pin carries out the P53 function.
- 1: PWM3 is on, and its related pin is automatically set to output.

NOTE

The P53/PWM3/VREF pin cannot be applied to PWM3 and VREF at the same time. IF P53/PWM3/VREF is configured as VREF analog input pin, then PWM3E must be "0".
The P53/PWM3/VREF pin priority is as follows:

P53/PWM3/VREF Pin Priority		
High	Medium	Low
VREF	PWM3	P53

Bit 6 (PWM2E): PWM2 enable bit

- 0: PWM2 is off (default value), and its related pin carries out the P52 function
- 1: PWM2 is on, and its related pin is automatically set to output

Bit 5 (PWM1E): PWM1 enable bit

- 0: PWM1 is off (default value), and its related pin carries out the P51 function
- 1: PWM1 is on, and its related pin is automatically set as output

Bit 4: Unimplemented, read as '0'

Bit 3 (T1EN): TMR1 enable bit

- 0: TMR1 is off (default value)
- 1: TMR1 is on

Bit 2 ~ Bit 0 (T1P2 ~ T1P0): TMR1 clock prescaler option bits

T1P2	T1P1	T1P0	Prescaler
0	0	0	1:2 (default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.5 IOC90 (TMRCON: Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3EN	T2EN	T3P2	T3P1	T3P0	T2P2	T2P1	T2P0

Bit 7 (T3EN): TMR3 enable bit

0: TMR3 is off (default value)

1: TMR3 is on

Bit 6 (T2EN): TMR2 enable bit

0: TMR2 is off (default value)

1: TMR2 is on

Bit 5 ~ Bit 3 (T3P2 ~ T3P0): TMR3 clock prescaler option bits

T3P2	T3P1	T3P0	Prescaler
0	0	0	1:2 (default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 2 ~ Bit 0 (T2P2 ~ T2P0): TMR2 clock prescaler option bits

T2P2	T2P1	T2P0	Prescale
0	0	0	1:2 (default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.6 IOCA0 (CMPCON: Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	"0"	CPOUT	COS1	COS0

Bit 7 ~ Bit 3: Unimplemented, read as '0'

Bit 2 (CPOUT): Result of the comparator output

Bit 1 ~ Bit 0 (COS1 ~ COS0): Comparator/OP Select bits

COS1	COS0	Function Description
0	0	Comparator and OP are not used. P60 is configured as normal I/O pin.
0	1	Configured as Comparator and P60 is configured as normal I/O pin.
1	0	Configured as Comparator and P60 is configured as Comparator output pin (CO).
1	1	Configured as OP and P60 is configured as OP output pin (CO).

NOTE

- The CO and ADC0 of the P60/ADC0/CO pins cannot be used at the same time.
- The P60/ADE0/CO pin priority is as follows:

P60/ADE0/CO Priority		
High	Medium	Low
CO	ADC0	P60

6.2.7 IOCB0 (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

The IOCB0 register is both readable and writable

Bit 7 (/PD7): Control bit used to enable the P67 pull-down pin

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD6): Control bit used to enable the P66 pull-down pin

Bit 5 (/PD5): Control bit used to enable the P65 pull-down pin

Bit 4 (/PD4): Control bit used to enable the P64 pull-down pin

Bit 3 (/PD3): Control bit used to enable the P63 pull-down pin

Bit 2 (/PD2): Control bit used to enable the P62 pull-down pin

Bit 1 (/PD1): Control bit used to enable the P61 pull-down pin

Bit 0 (/PD0): Control bit used to enable the P60 pull-down pin

6.2.8 IOCC0 (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0

The **IOCC0** register is both readable and writable.

Bit 7 (OD7): Control bit used to enable open-drain of the P57 pin.

- 0: Enable open-drain output
- 1: Disable open-drain output

Bit 6 (OD6): Control bit used to enable open-drain of the P56 pin.

Bit 5 (OD5): Control bit used to enable open-drain of the P55 pin.

Bit 4 (OD4): Control bit used to enable open-drain of the P54 pin.

Bit 3 (OD3): Control bit used to enable open-drain of the P53 pin.

Bit 2 (OD2): Control bit used to enable open-drain of the P52 pin.

Bit 1 (OD1): Control bit used to enable open-drain of the P51 pin.

Bit 0 (OD0): Control bit used to enable open-drain of the P50 pin.

6.2.9 IOCD0 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

The **IOCD0** register is both readable and writable.

Bit 7 (PH7): Control bit used to enable the P67 pull-high pin.

- 0: Enable internal pull-high
- 1: Disable internal pull-high

Bit 6 (PH6): Control bit used to enable pull-high of the P66 pin.

Bit 5 (PH5): Control bit used to enable pull-high of the P65 pin.

Bit 4 (PH4): Control bit used to enable pull-high of the P64 pin.

Bit 3 (PH3): Control bit used to enable pull-high of the P53 pin.

Bit 2 (PH2): Control bit used to enable pull-high of the P52 pin.

Bit 1 (PH1): Control bit used to enable pull-high of the P51 pin.

Bit 0 (PH0): Control bit used to enable pull-high of the P50 pin.



6.2.10 IOCE0 (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	PSWE	PSW2	PSW1	PSW0	"0"	"0"

Bit 7 (WDTE): Control bit used to enable the Watchdog Timer

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of the P50 (/INT) pin

0: P50, normal I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P50 (Bit 0 of IOC50) must be set to "1".

NOTE

- When EIS is "0," the path of the /INT is masked. When EIS is "1," the status of the /INT pin can also be read by way of reading Port 5 (R5). Refer to Figure 6-4 (I/O Port and I/O Control Register Circuit for P50 (/INT)) under Section 6.4 (I/O Ports).
- EIS is both readable and writable.

Bit 5 (PSWE): Prescaler enable bit for WDT

0: prescaler disable bit. WDT rate is 1:1

1: prescaler enable bit. WDT rate is set at Bit 4~Bit 2.

Bit 4 ~ Bit 2 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 1 ~ Bit 0: Unimplemented, read as '0'.

6.2.11 IOCF0 (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIE	PWM3IE	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE

NOTE

- IOCF0 register is both readable and writable.
- Individual interrupt is enabled by setting its associated control bit in the IOCF0 to "1."
- Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).

Bit 7 (CMPIE): CMPIF interrupt enable bit

- 0: Disable CMPIF interrupt
- 1: Enable CMPIF interrupt

When the Comparator output status change is used to enter an interrupt vector, the CMPIE bit must be set to "Enable".

Bit 6 (PWM3IE): PWM3IF interrupt enable bit

- 0: Disable PWM3 interrupt
- 1: Enable PWM3 interrupt

Bit 5 (PWM2IE): PWM2IF interrupt enable bit

- 0: Disable PWM2 interrupt
- 1: Enable PWM2 interrupt

Bit 4 (PWM1IE): PWM1IF interrupt enable bit

- 0: Disable PWM1 interrupt
- 1: Enable PWM1 interrupt

Bit 3 (ADIE): ADIF interrupt enable bit

- 0: Disable ADIF interrupt
- 1: Enable ADIF interrupt

When the ADC Complete is used to enter an interrupt vector, the ADIE bit must be set to "Enable".

Bit 2 (EXIE): EXIF interrupt enable bit

- 0: Disable EXIF interrupt
- 1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

- 0: Disable ICIF interrupt
- 1: Enable ICIF interrupt

If Port 6 Input Status Change Interrupt is used to enter an interrupt vector, the ICIE bit must be set to "Enable".

Bit 0 (TCIE): TCIF interrupt enable bit.

- 0: Disable TCIF interrupt
- 1: Enable TCIF interrupt



6.2.12 IOC51 (PRD1: PWM1 Time Period)

The content of IOC51 is the time period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

6.2.13 IOC61 (PRD2: PWM2 Time Period)

The content of IOC61 is the time period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

6.2.14 IOC71 (PRD3: PWM3 Time Period)

The content of IOC71 is the time period (time base) of PWM3. The frequency of PWM3 is the reverse of the period.

6.2.15 IOC81 (DT1L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM1 Duty Cycle)

A specified value keeps the output of PWM1 to remain high until the value matches with TMR1.

6.2.16 IOC91 (DT2L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM2 Duty Cycle)

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2.

6.2.17 IOCA1 (DT3L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM3 Duty Cycle)

A specified value keeps the output of PWM3 to remain high until the value matches with TMR3.

6.2.18 IOCB1 (DTH: Most Significant Bits of PWM Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	PWM3[9]	PWM3[8]	PWM2[9]	PWM2[8]	PWM1[9]	PWM1[8]

Bit 7 and Bit 6: Unimplemented, read as '0'.

Bit 5 and Bit 4 (PWM3[9], PWM3[8]): Most Significant Bits of PWM3 Duty Cycle.

Bit 3 and Bit 2 (PWM2[9], PWM2[8]): Most Significant Bits of PWM2 Duty Cycle.

Bit 1 and Bit 0 (PWM1[9], PWM1[8]): Most Significant Bits of PWM1 Duty Cycle.

6.2.19 IOCC1 (TMR1L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM1 Timer)

The contents of IOCC1 are read-only.

6.2.20 IOCD1 (TMR2L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM2 Timer)

The contents of IOCD1 are read-only.

6.2.21 IOCE1 (TMR3L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM3 Timer)

The contents of IOCE1 are read-only.

6.2.22 IOCF1 (TMRH: Most Significant Bits of the PWM Timer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	TMR3[9]	TMR3[8]	TMR2[9]	TMR2[8]	TMR1[9]	TMR1[8]

The contents of IOCF1 are read-only.

Bit 7 and Bit 6: Unimplemented, read as '0'

Bit 5 and Bit 4 (TMR3 [9], TMR3 [8]): Most Significant Bits of PWM1 Timer

Bit 3 and Bit 2 (TMR2 [9], TMR2 [8]): Most Significant Bits of PWM2 Timer

Bit 1 and Bit 0 (TMR1 [9], TMR1 [8]): Most Significant Bits of PWM3 Timer

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0 ~ PST2 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PWR0 ~ PWR2 bits of the IOCE0 register are used to determine the WDT prescaler. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-2 (next page) depicts the block diagram of TCC/WDT.

TCC (R1) is an 8-bit timer/counter. The TCC clock source can be internal clock or external signal input (edge selectable from the TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). Referring to Figure 6-2, CLK=Fosc/2 or CLK=Fosc/4 is dependent to the Code Option bit <CLKS>. CLK=Fosc/2 if the CLKS bit is "0," and CLK=Fosc/4 if the CLKS bit is "1." If TCC signal source is from an external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept in High or Low level) must be greater than 1 CLK.

NOTE

The internal TCC will stop running when sleep mode occurs. However, during AD conversion, when TCC is set to "SLEP" instruction, if the ADWE bit of the RE register is enabled, TCC will keep on running.

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode through software programming. Refer to WDTE bit of IOCE0 register (Section 6.2.10 *IOCE0 (WDT Control Register)*). With no prescaler, the WDT time-out duration is approximately 18ms.¹

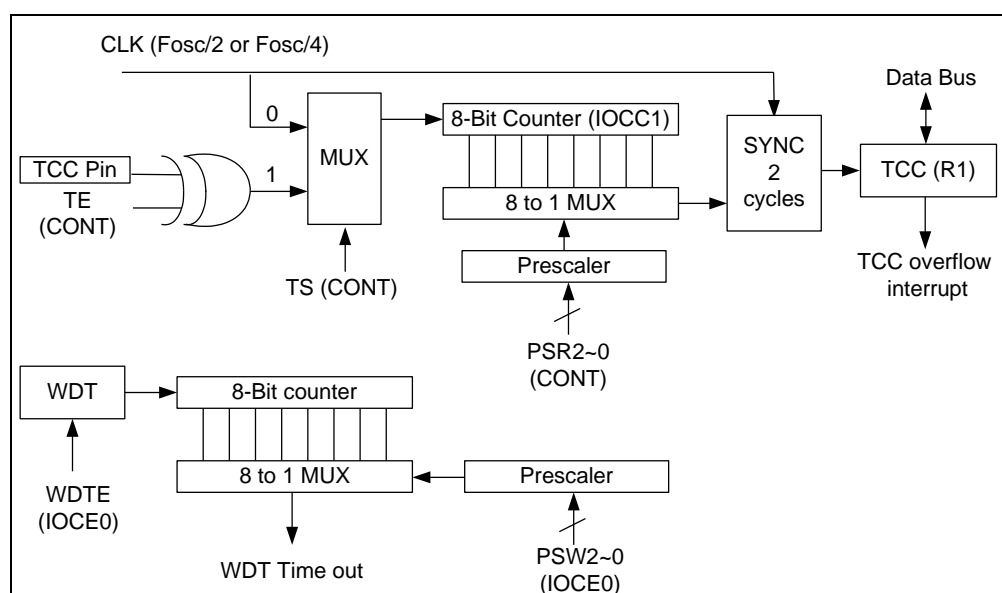
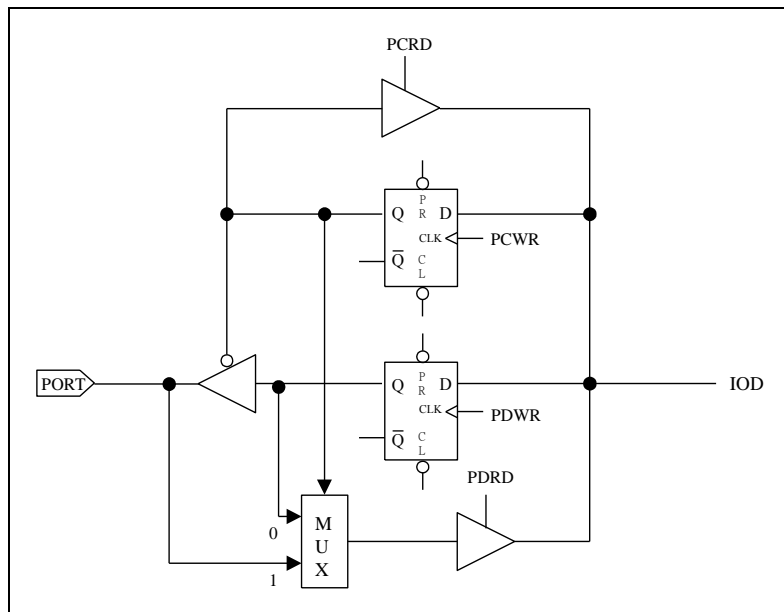


Figure 6-2 TCC and WDT Block Diagram

6.4 I/O Ports

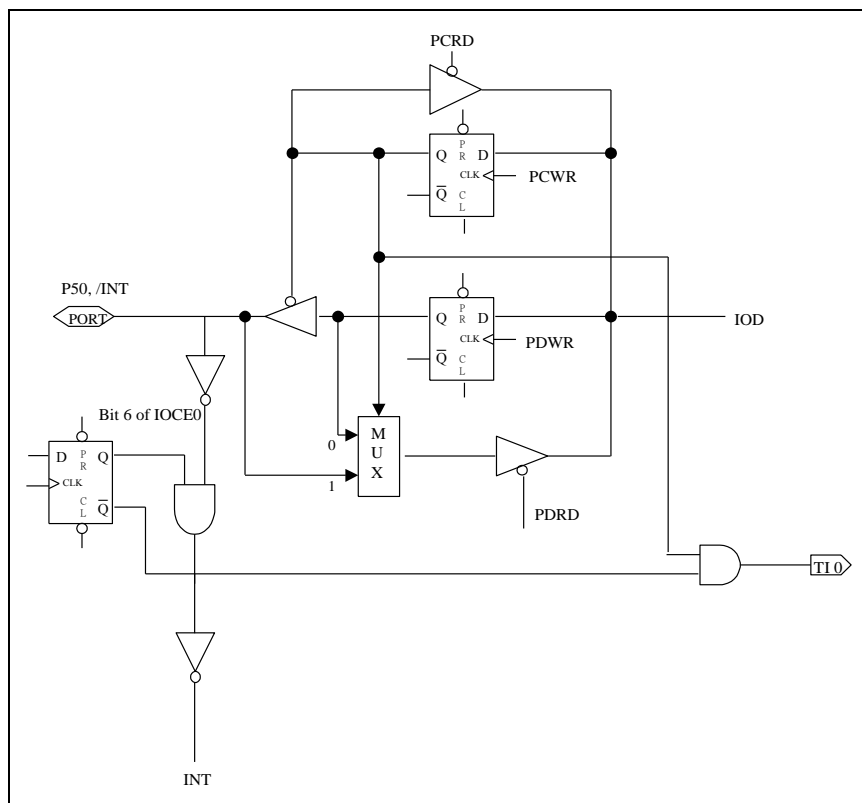
The I/O registers (Port 5, Port 6, and Port 7) are bidirectional tri-state I/O ports. The Pull-high, Pull-down, and Open-drain functions can be set internally by IOCB0, IOCC0, and IOCD0 respectively. Port 6 has an input status change interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control registers (IOC50 ~ IOC70). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6, and Port 7 are illustrated in Figures 6-3, 6-4, and 6-5 respectively. Port 6 with Input Change Interrupt/Wake-up is shown in Figure 6-6.

¹ VDD=5V, Setup time period = 16.5ms ± 30%.
VDD=3V, Setup time period = 18ms ± 30%.



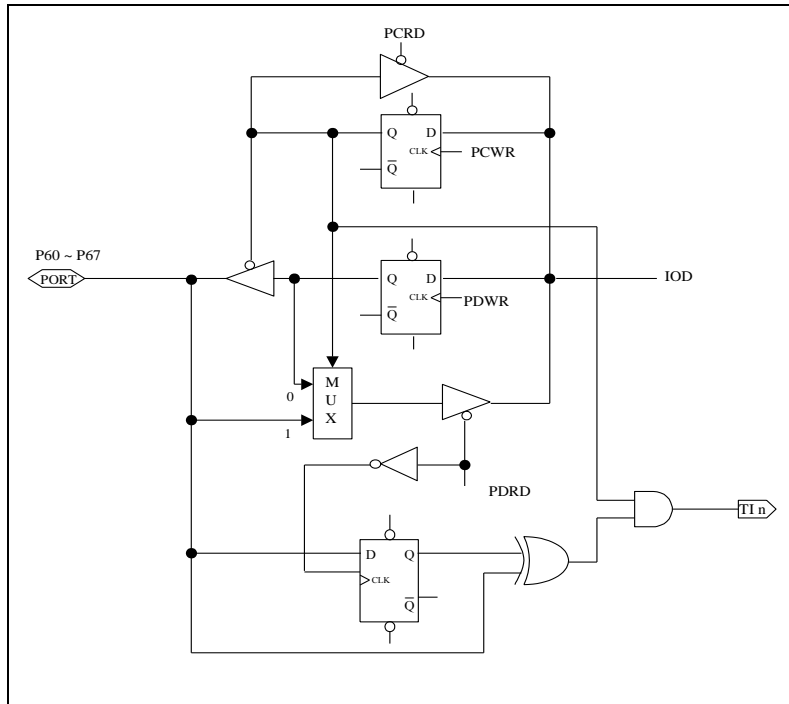
Note: Pull-high and Open-drain are not shown in the figure.

Figure 6-3 I/O Port and I/O Control Register Circuit for Port 5 and Port 7



Note: Pull-high and Open-drain are not shown in the figure.

Figure 6-4 I/O Port and I/O Control Register Circuit for P50 (/INT)



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-5 I/O Port and I/O Control Register Circuit for Port 6

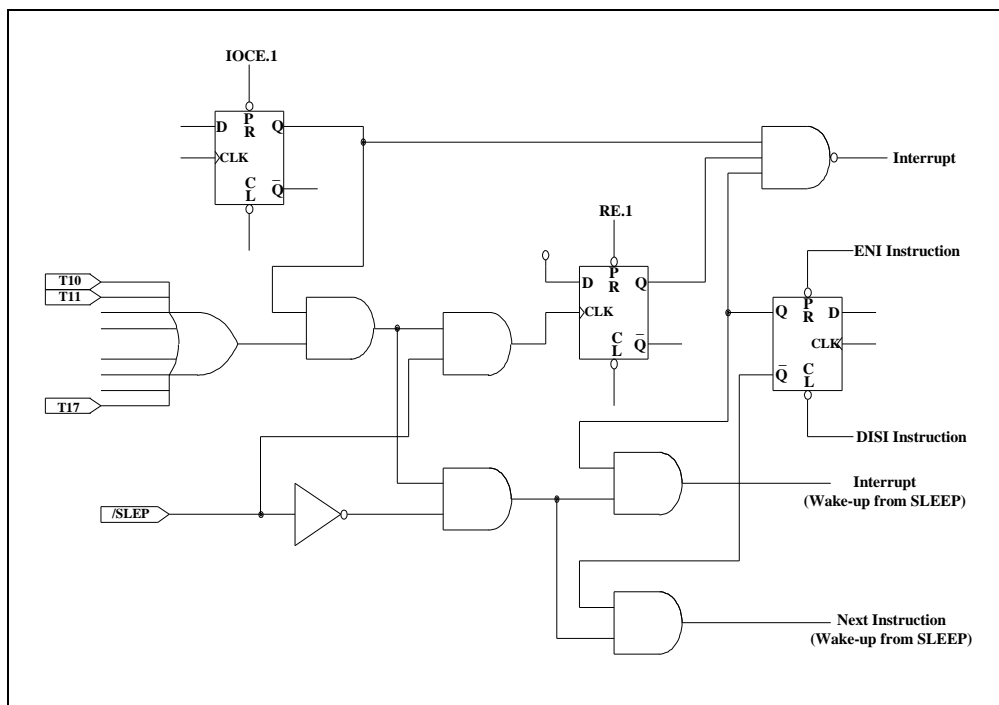


Figure 6-6 Port 6 Block Diagram with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

(1) Wake-up	(2) Wake-up and Interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port 6 (MOV R6,R6)	2. Read I/O Port 6 (MOV R6,R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set RE ICWE =1)	4. Enable wake-up bit (Set RE ICWE =1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set IOCF0 ICIE =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt Vector (008H)
	2. IF "DISI" → Next instruction
(3) Interrupt	
(a) Before Port 6 pin change	
1. Read I/O Port 6 (MOV R6,R6)	
2. Execute "ENI" or "DISI"	
3. Enable interrupt (Set IOCF0 ICIE =1)	
(b) After Port 6 pin changed (interrupt)	
1. IF "ENI" → Interrupt vector (008H)	
2. IF "DISI" → Next instruction	

6.5 Reset and Wake-up

6.5.1 Reset and Wake-up Operation

A reset is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

A device is kept in a reset condition for a period of approximately 18 ms.² when a reset is detected. When in LXT mode, the reset time is 500 ms. Once a reset occurs, the following functions are performed (the initial Address is 000h):

- The oscillator continues running, or will be started (if in sleep mode)
- The Program Counter (R2) is set to all "0"
- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog Timer and prescaler are cleared
- When power is switched on, the upper 3 bits of R3 and upper 2 bits of R4 are cleared
- The IOCB0 register bits are set to all "1"
- The IOCC0 register bits are set to all "1"
- The IOCD0 register bits are set to all "1"
- Bit 7 of the IOCE0 register is set to "1", and Bits 6~0 are cleared
- Bits 0~6 of the RF register and bits 0~6 of IOCF0 register are cleared

² VDD=5V, WDT Time-out period = 16.5ms ± 30%.
VDD=3V, WDT Time-out period = 18ms ± 30%.

Executing the “SLEP” instruction will assert the sleep (power down) mode. While entering sleep mode, the Oscillator, TCC, Timer 1, Timer 2, and Timer 3 are stopped. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by:

- Case 1 External reset input on the /RESET pin
- Case 2 WDT time-out (if enabled)
- Case 3 Port 6 input status changes (if ICWE is enabled)
- Case 4 Comparator output status changes (if CMPWE is enabled)
- Case 5 AD conversion completed (if ADWE enable).

The first two Cases (1 and 2) will cause the EM78P418N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, and 5 are considered the continuation of program execution and the global interrupt (“ENI” or “DISI” being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x8 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction next to SLEP after wake-up.

Only one of Cases 1 to 5 can be enabled before entering into sleep mode. That is:

- Case [a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78P418N can be awakened only with Case 1 or Case 2. Refer to the section on Interrupt (Section 6.6) for further details.
- Case [b] If Port 6 Input Status Change is used to wake -up EM78P418N and ICWE bit of RE register is enabled before SLEP, WDT must be disabled. Hence, the EM78P418N can be awakened only in Case 3. Wake-up time is dependent on the oscillator mode. In RC mode, wake-up time is 32 clocks (for stable oscillators). In High Crystal mode, wake-up time is 2ms and 32 clocks (for stable oscillators); and in low Crystal mode, Wake-up time is 500ms.
- Case [c] If Comparator output status change is used to wake-up EM78P418N and CMPWE bit of RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P418N can be awakened only in Case 4.

Wake-up time is dependent on the oscillator mode. In RC mode, wake-up time is 32 clocks (for stable oscillator). In High Crystal mode, wake-up time is 2ms and 32 clocks (for oscillator stables); and in low Crystal mode, wake-up time is 500ms.
- Case [d] If AD conversion completed is used to wake-up EM78P418N and ADWE bit of RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P418N can be awakened only in Case 5. The wake-up time is 15 TAD (ADC clock period).



If Port 6 Input Status Change Interrupt is used to wake up the EM78P418N (as in the Case b above), the following instructions must be executed before SLEP:

```
BC          R3, 7           ; Select Segment 0
MOV         A, @001110xxb   ; Select WDT prescaler and Disable WDT
IOW        IOCE0
WDTC                          ; Clear WDT and prescaler
MOV         R6, R6         ; Read Port 6
ENI (or DISI)                ; Enable (or disable) global interrupt
MOV         A, @00000x1xb   ; Enable Port 6 input change wake-up bit
MOV         RE
MOV         A, @00000x1xb   ; Enable Port 6 input change interrupt
IOW        IOCF0
SLEP                          ; Sleep
```

Similarly, if the Comparator Interrupt is used to wake up the EM78P418N (as in Case [c] above), the following instructions must be executed before SLEP:

```
BC          R3, 7           ; Select Segment 0
MOV         A, @xxxxxxx10b  ; Select a comparator and P60 is
                               ; configured as CO pin
IOW        IOCA0
MOV         A, @001110xxb   ; Select WDT prescaler and Disable WDT
IOW        IOCE0
WDTC                          ; Clear WDT and prescaler
ENI (or DISI)                ; Enable (or disable) global interrupt
MOV         A, @000001xxb   ; Enable comparator output status change
                               ; wake-up bit
MOV         RE
MOV         A, @000001xxb   ; Enable comparator output status change
                               ; interrupt
IOW        IOCF0
SLEP                          ; Sleep
```

6.5.1.1 Wake-up and Interrupt Modes Operation Summary

All categories under Wake-up and Interrupt modes are summarized below.

Signal	Sleep Mode	Normal Mode
TCC Overflow	N/A	DISI + IOCF0 (TCIE) Bit 0 = 1 Next Instruction+ Set RF (TCIF) = 1 ENI + IOCF0 (TCIE) Bit 0 = 1 Interrupt Vector (0x08)+ Set RF (TCIF) = 1
Port 6 Input Status Change	RE (ICWE) Bit 1 = 0, IOCF0 (ICIE) Bit 1 = 0 Oscillator, TCC and TIMERX are stopped. Port 6 input status changed wake-up is invalid.	IOCF0 (ICIE) Bit1 = 0 Port 6 input status change interrupt is invalid
	RE (ICWE) Bit 1 = 0, IOCF0 (ICIE) Bit 1 = 1 Set RF (ICIF) = 1, Oscillator, TCC and TIMERX are stopped. Port 6 input status changed wake-up is invalid.	
	RE (ICWE) Bit 1 = 1, IOCF0 (ICIE) Bit 1 = 0 Wake-up+ Next Instruction Oscillator, TCC and TIMERX are stopped.	
	RE (ICWE) Bit 1 = 1, DISI + IOCF0 (ICIE) Bit 1 = 1 Wake-up+ Next Instruction+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	DISI + IOCF0 (ICIE) Bit 1 = 1 Next Instruction+ Set RF (ICIF) = 1
	RE (ICWE) Bit 1 = 1, ENI + IOCF0 (ICIE) Bit 1 = 1 Wake-up+ Interrupt Vector (0x08)+ Set RF (ICIF)= Oscillator, TCC and TIMERX are stopped.	ENI + IOCF0 (ICIE) Bit 1 = 1 Interrupt Vector (0x08)+ Set RF (ICIF) = 1
INT Pin	N/A	DISI + IOCF0 (EXIE) Bit 2 = 1 Next Instruction+ Set RF (EXIF) = 1 ENI + IOCF0 (EXIE) Bit 2 = 1 Interrupt Vector (0x08)+ Set RF (EXIF) = 1
AD Conversion	RE (ADWE) Bit 3 = 0, IOCF0 (ADIE) Bit 3 = 0 Clear R9 (ADRUN)=0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	IOCF0 (ADIE) Bit 1 = 0 AD conversion interrupt is invalid
	RE (ADWE) Bit 3=0, IOCF0 (ADIE) Bit 3 = 1 Set RF (ADIF)=1, R9 (ADRUN) = 0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	
	RE (ADWE) Bit 3 = 1, IOCF0 (ADIE) Bit 3 = 0 Wake-up+ Next Instruction, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	
	RE (ADWE) Bit 3 = 1, DISI + IOCF0 (ADIE) Bit 3 = 1 Wake-up+ Next Instruction+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	DISI + IOCF0 (ADIE) Bit 3 = 1 Next Instruction+ RF (ADIF) = 1
	RE (ADWE) Bit 3 = 1, ENI + IOCF0 (ADIE) Bit 3 = 1 Wake-up+ Interrupt Vector (0x08)+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	ENI + IOCF0 (ADIE) Bit 3 = 1 Interrupt Vector (0x08)+ Set RF (ADIF) = 1
PWMX (PWM1,PWM2,PWM3) (When TimerX matches PRDX)	N/A	DISI + IOCF0 (PWMXIE) = 1 Next Instruction+ Set RF (PWMXIF) = 1 ENI + IOCF0 (PWMXIE) = 1 Interrupt Vector (0x08)+ Set RF (PWMXIF) = 1

(Continuation)

Signal	Sleep Mode	Normal Mode
Comparator (Comparator Output Status Change)	RE (CMPWE) Bit 2 = 0, IOCF0 (CMPIE) Bit 7 = 0 Comparator output status changed wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	IOCF0 (CMPIE) Bit 7 = 0 Comparator output status change interrupt is invalid.
	RE (CMPWE) Bit 2 = 0, IOCF0 (CMPIE) Bit 7 = 1 Set RF (CMPIF) = 1, Comparator output status changed wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	
	RE (CMPWE) Bit 2 = 1, IOCF0 (CMPIE) Bit 7 = 0 Wake-up+ Next Instruction, Oscillator, TCC and TIMERX are stopped.	
	RE (CMPWE) Bit 2 = 1, DISI + IOCF0 (CMPIE) Bit 7 = 1 Wake-up+ Next Instruction+ Set RF (CMPIF)=1, Oscillator, TCC and TIMERX are stopped.	DISI + IOCF0 (CMPIE) Bit 7 = 1 Next Instruction+ Set RF (CMPIF) = 1
	RE (CMPWE) Bit 2 = 1, ENI + IOCF0 (CMPIE) Bit 7 = 1 Wake-up+ Interrupt Vector (0x08)+ Set RF (CMPIF) = 1, Oscillator, TCC and TIMERX are stopped.	ENI + IOCF0 (CMPIE) Bit 7 = 1 Interrupt Vector (0x08)+ Set RF (CMPIF) = 1
WDT Time Out IOCE (WDTE) Bit 7 = 1	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)

6.5.1.2 Register Initial Values after Reset

The following table summarizes the registers initialized values:

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC70	Bit Name	-	-	-	C74	C73	C72	C71	C70
		Power-on	0	0	0	1	1	1	1	1
		/RESET & WDT	0	0	0	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC80 (PWMCON)	Bit Name	PWM3E	PWM2E	PWM1E	-	T1EN	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC90 (TMRCON)	Bit Name	T3EN	T2EN	T3P2	T3P1	T3P0	T2P2	T2P1	T2P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA0 (CMPCON)	Bit Name	-	-	-	-	-	CPOUT	COS1	COS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB0	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC0	Bit Name	/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD0	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE0	Bit Name	WDTE	EIS	PSWE	PSW2	PSW1	PSW0	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCF0	Bit Name	CMPIE	PMW3IE	PMW2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC51 (PRD1)	Bit Name	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC61 (PRD2)	Bit Name	PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC71 (PRD3)	Bit Name	PRD3[7]	PRD3[6]	PRD3[5]	PRD3[4]	PRD3[3]	PRD3[2]	PRD3[1]	PRD3[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC81 (DT1L)	Bit Name	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC91 (DT2L)	Bit Name	DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]	DT2[1]	DT2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA1 (DT3L)	Bit Name	DT3[7]	DT3[6]	DT3[5]	DT3[4]	DT3[3]	DT3[2]	DT3[1]	DT3[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	P	P
N/A	IOCB1 (DT1H, 2H, 3H)	Bit Name	-	-	DT3[9]	DT3[8]	DT2[9]	DT2[8]	DT1[9]	DT1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC1 (TMR1L)	Bit Name	TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD1 (TMR2L)	Bit Name	TMR2[7]	TMR2[6]	TMR2[5]	TMR2[4]	TMR2[3]	TMR2[2]	TMR2[1]	TMR2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCE1 (TMR3L)	Bit Name	TMR3[7]	TMR3[6]	TMR3[5]	TMR3[4]	TMR3[3]	TMR3[2]	TMR3[1]	TMR3[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCF1 (TMR1H, 2H, 3H)	Bit Name	-	-	TMR3[9]	TMR3[8]	TMR2[9]	TMR2[8]	TMR1[9]	TMR1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x08 or continue to execute next instruction							
0x03	R3(SR)	Bit Name	IOCS	PS1	PS0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET & WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	BS7	BS6	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET & WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	R7	Bit Name	-	-	-	P74	P73	P72	P71	P70
		Power-on	0	0	0	1	1	1	1	1
		/RESET & WDT	0	0	0	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	R8 (AISR)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09	R9 (ADCON)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	RA (ADOC)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0B	RB (ADDDATA)	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	RC (ADDDATA1H)	Bit Name	-	-	-	-	AD11	AD10	AD9	AD8
		Power-on	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	RD (ADDATA1L)	Bit Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	RE (WUCR)	Bit Name	-	-	-	-	ADWE	CMPWE	ICWE	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0F	RF (ISR)	Bit Name	CMPIF	PWM3IF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x10 ~ 0x3F	R10 ~ R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: - : not used
 U: unknown or don't care
 t: check "Reset Type" table in Section 6.5.2
 P: previous value before reset

6.5.1.3 Controller Reset Block Diagram

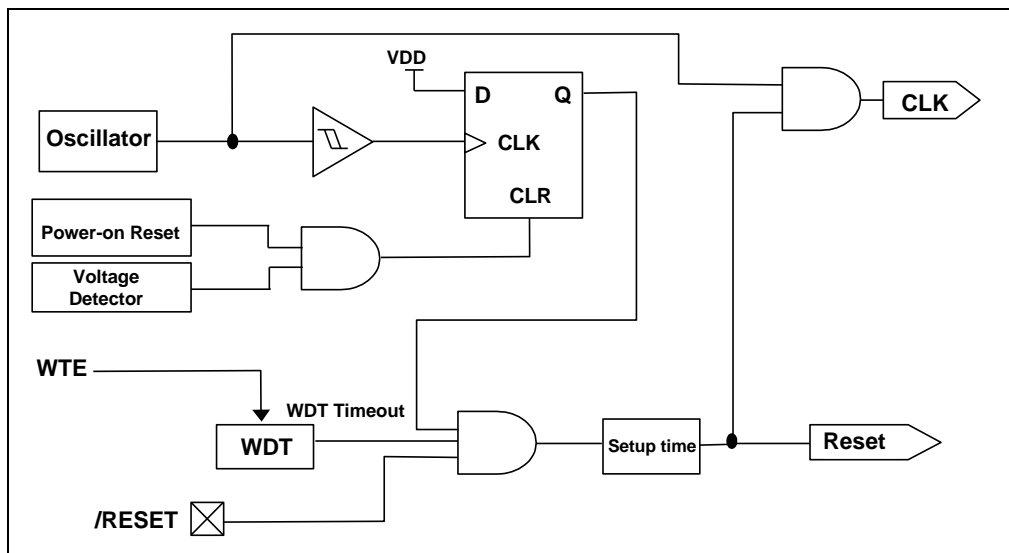


Figure 6-7 Controller Reset Block Diagram

6.5.2 T and P Status in the Status Register

A reset condition is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The values of T and P as listed in the table below, are used to check how the processor wakes up.

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

*P: Previous status before reset

The following shows the events that may affect the status of T and P.

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during Sleep mode	1	0

*P: Previous value before reset

6.6 Interrupt

The EM78P418N has six interrupts as listed below:

1. TCC overflow interrupt
2. Port 6 Input Status Change Interrupt
3. External interrupt [(P50, /INT) pin]
4. Analog to Digital conversion completed
5. When TMR1/TMR2/TMR3 matches with PRD1/PRD2/PRD3 respectively in PWM
6. When the comparators output changes (for EM78P418N – 20 Pin and EM78P418N – 24 Pin only)

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6, R6") is necessary. Each Port 6 pin will have this feature if its status changes. Any pin configured as output, including the P50 pin which is configured as /INT, is excluded from this function. Port 6 Input Status Change Interrupt will wake up the EM78P418N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP instruction.

When wake-up occurs, the controller will continue to execute the succeeding program if the global interrupt is disabled. If enabled, it will branch out to the Interrupt Vector 008H.

External interrupt equipped with digital noise rejection circuit (input pulse less than 8 system clock time) is eliminated as noise. Edge selection is possible with /INT. Refer to the Word 1 Bits 8–7 (Section 6.14.2, Code Option Register (Word 1)) for digital noise rejection definition.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from Address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or of the ENI execution. Note that the result of RF will be the logic AND of RF and IOCF0 (refer to figure below). The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

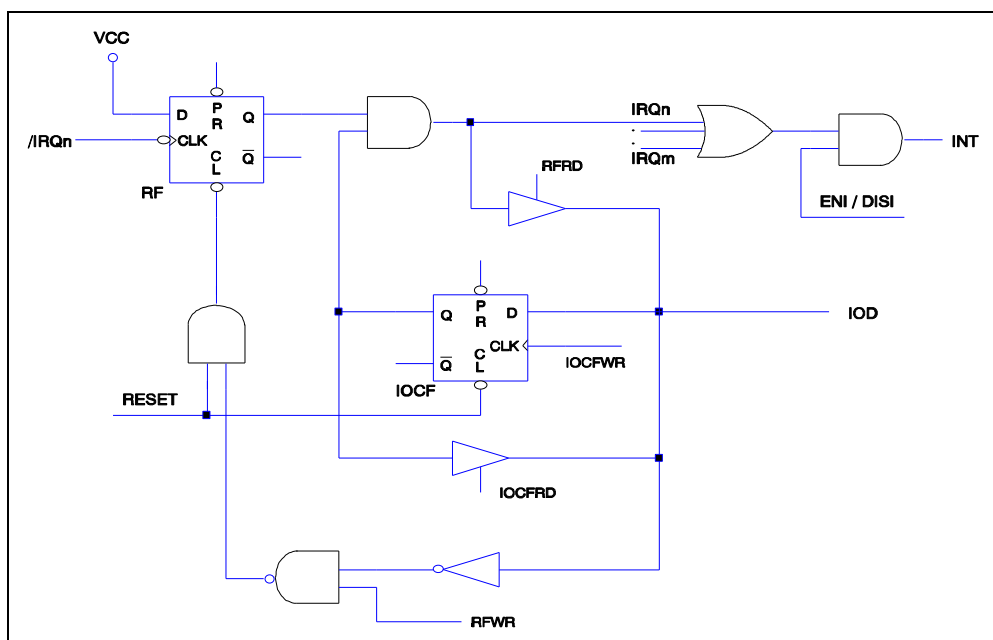


Figure 6-8 Interrupt Input Circuit

6.7 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 8-bit analog multiplexer; three control registers (AISR/R8, ADCON/R9, and ADOC/RA), three data registers (ADDATA1/RB, ADDATA1H/RC, and ADDATA1L/RD) and an ADC with 12-bit resolution as shown in the functional block diagram below. The analog reference voltage (Vref) and the analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATA, ADDATA1H and ADDATA1L. Input channels are selected by the analog input multiplexer via the ADCON register bits. Connecting to external VREF is more accuracy than internal VDD.

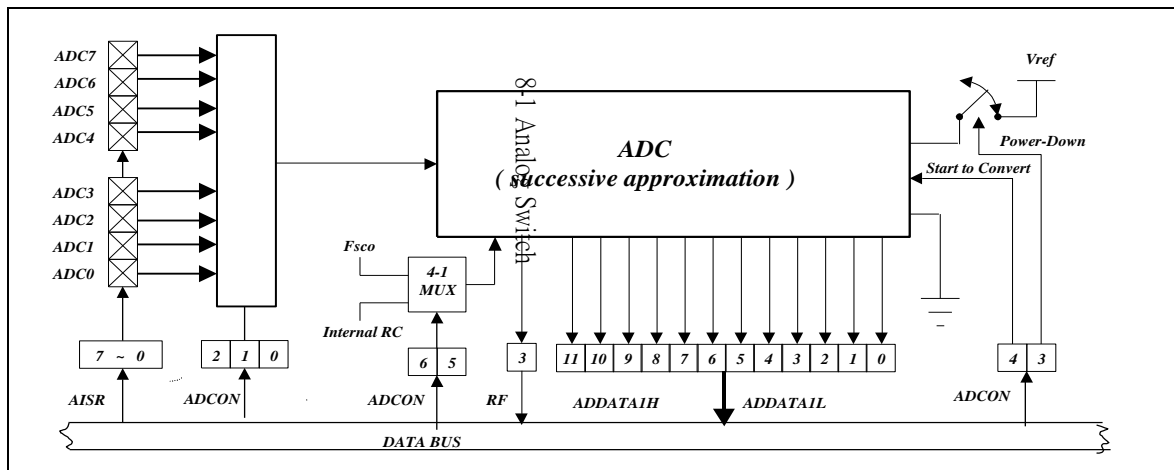


Figure 6-9 Analog-to-Digital Conversion Functional Block Diagram

6.7.1 ADC Control Register (AISR/R8, ADCON/R9, ADOC/RA)

6.7.1.1 R8 (AISR: ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1
*Init_Value	0	0	0	0	0	0	0

The AISR register individually defines the Port 6 pins as analog input or as digital I/O.

Bit 7 (ADE7): AD converter enable bit of P67 pin

- 0: Disable ADC7, P67 is configured as I/O pin
- 1: Enable ADC7 which is configured as analog input pin

Bit 6 (ADE6): AD converter enable bit of P66 pin

- 0: Disable ADC6, P66 is configured as I/O pin
- 1: Enable ADC6 which is configured as analog input pin



- Bit 5 (ADE5):** AD converter enable bit of P65 pin
 0: Disable ADC5, P65 is configured as I/O pin
 1: Enable ADC5 which is configured as analog input pin
- Bit 4 (ADE4):** AD converter enable bit of P64 pin
 0: Disable ADC4, P64 is configured as I/O pin
 1: Enable ADC4 which is configured as analog input pin
- Bit 3 (ADE3):** AD converter enable bit of P63 pin
 0: Disable ADC3, P63 is configured as I/O pin
 1: Enable ADC3 which is configure as analog input pin
- Bit 2 (ADE2):** AD converter enable bit of P62 pin
 0: Disable ADC2, P63 is configured as I/O pin
 1: Enable ADC2 which is configured as analog input pin
- Bit 1 (ADE1):** AD converter enable bit of P61 pin
 0: Disable ADC1, P61 is configured as I/O pin
 1: Enable ADC1 which is configured as analog input pin
- Bit 0 (ADE0):** AD converter enable bit of P60 pin
 0: Disable ADC0, P60 is configured as I/O pin
 1: Enable ADC0 which is configured as analog input pin

NOTE

Note the pin priority of the COS1 and COS0 bits of IOCA0 Control register when P60/ADC0 is configured as analog input or as digital I/O. The Comparator/OP select bits are as shown in the table under Section 6.2.6.

The P60/ADE0/CO pin priority is as follows:

P60/ADE0/CO Priority		
High	Medium	Low
CO	ADC0	P60

6.7.1.2 R9 (ADCON: ADC Control Register)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
*Init_Value	0	0	0	0	0	0	0	0

Note: *Init_Value: Initial value at power-on reset

The ADCON register controls the operation of the AD conversion and determines which pin should be currently active.

Bit 7 (VREFS): The input source of the Vref of the ADC

0: The Vref of the ADC is connected to Vdd (default value), and the P53/VREF pin carries out the function of P53

1: The Vref of the ADC is connected to P53/VREF

NOTE

The P53/PWM3/VREF pin cannot be applied to PWM3 and VREF at the same time. If P53/PWM3/VREF is configured as VREF analog input pin, then PWM3E must be "0".

The P53/PWM3/VREF pin priority is as follows:

P53/PWM3/VREF Pin Priority		
High	Medium	Low
VREF	PWM3	P53

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler oscillator clock rate of ADC

00 = 1:16 (default value)

01 = 1: 4

10 = 1: 64

11 = 1: WDT ring oscillator frequency

CKR1:CKR0	Operation Mode	Max. Operation Frequency
00	Fosc/16	4 MHz
01	Fosc/4	1 MHz
10	Fosc/64	16 MHz
11	Internal RC	-

Bit 4 (ADRUN): ADC starts to RUN

0: reset on completion of the conversion. This bit cannot be reset by software.

1: an AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: switch off the resistor reference to save power even while the CPU is operating.

1: ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

- 000 = AN0/P60
- 001 = AN1/P61
- 010 = AN2/P62
- 011 = AN3/P63
- 100 = AN4/P64
- 101 = AN5/P65
- 110 = AN6/P66
- 111 = AN7/P67

These bits can only be changed when the ADIF bit and the ADRUN bit are both low.

6.7.1.3 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	"0"	"0"	"0"

Bit 7 (CALI): Calibration enable bit for ADC offset

- 0: Calibration disabled
- 1: Calibration enabled

Bit 6 (SIGN): Polarity bit of offset voltage

- 0: Negative voltage
- 1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P418N	ICE418N
0	0	0	0LSB	0LSB
0	0	1	2LSB	1LSB
0	1	0	4LSB	2LSB
0	1	1	6LSB	3LSB
1	0	0	8LSB	4LSB
1	0	1	10LSB	5LSB
1	1	0	12LSB	6LSB
1	1	1	14LSB	7LSB

Bit 2 ~ Bit 0: Unimplemented, read as '0'

6.7.2 ADC Data Register (ADDATA/RB, ADDATA1H/RC, ADDATA1L/RD)

When the AD conversion is completed, the result is loaded to the ADDATA, ADDATA1H and ADDATA1L registers. The ADRUN bit is cleared, and the ADIF is set.

6.7.3 ADC Sampling Time

The accuracy, linearity, and speed of the successive approximation of the AD converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μ s for each K Ω of the analog source impedance and at least 2 μ s for the low-impedance source. The maximum recommended impedance for analog source is 10 K Ω at V_{dd}=5V. After the analog input channel is selected, this acquisition time must be done before the conversion is started.

6.7.4 AD Conversion Time

CKR1 and CKR0 select the conversion time (T_{ct}), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the AD conversion accuracy. For the EM78P418N, the conversion time per bit is about 4 μ s. The table below shows the relationship between T_{ct} and the maximum operating frequencies.

CKR1:CKR0	Operation Mode	Max. Operation Frequency	Max. Conversion Rate/Bit	Max. Conversion Rate
00	Fosc/16	4 MHz	250kHz (4 μ s)	15*4 μ s=60 μ s (16.7kHz)
01	Fosc/4	1 MHz	250kHz (4 μ s)	15*4 μ s=60 μ s (16.7kHz)
10	Fosc/64	16 MHz	250kHz (4 μ s)	15*4 μ s=60 μ s (16.7kHz)
11	Internal RC	-	14kHz (71 μ s)	15*71 μ s=1065 μ s (0.938kHz)

NOTE

- Pin not used as an analog input pin can be used as regular input or output pin.
- During conversion, do not perform output instruction to maintain precision for all of the pins.

6.7.5 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, Timer 1, Timer 2, Timer 3, and AD conversion.

The AD Conversion is considered completed as determined by:

1. ADRUN bit of R9 register is cleared ("0" value)
2. Wake-up from AD conversion (where it remains in operation during sleep mode)

The results are fed into the ADDATA, ADDATA1H, and ADDATA1L registers when the conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of ADPD bit is.

6.7.6 Programming Process/Considerations

6.7.6.1 Programming Process

Follow these steps to obtain data from the ADC:

1. Write to the eight bits (ADE7:ADE0) on the R8 (AISR) register to define the characteristics of R6 (digital I/O, analog channels, or voltage reference pin)
2. Write to the R9/ADCON register to configure the AD module:
 - a) Select ADC input channel (ADIS2:ADIS0)
 - b) Define AD conversion clock rate (CKR1:CKR0)
 - c) Select the VREFS input source of the ADC
 - d) Set the ADPD bit to 1 to begin sampling
3. Set the ADWE bit, if the wake-up function is employed
4. Set the ADIE bit, if the interrupt function is employed
5. Write "ENI" instruction, if the interrupt function is employed
6. Set the ADRUN bit to 1
7. Write "SLEP" instruction or Polling.
8. Wait for wake-up or for ADRUN bit to be cleared ("0" value)
9. Read the ADDATA or ADDATA1H and ADDATA1L conversion data registers. If ADC input channel changes at this time, the ADDATA, ADDATA1H, and ADDATA1L values can be cleared to '0'.
10. Clear the interrupt flag bit (ADIF).
11. For the next conversion, go to Step 1 or Step 2 as required. At least 2 Tct is required before the next acquisition starts.

NOTE

In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion

6.7.6.2 Sample Demo Programs

A. Define a General Registers

```
R_0 == 0           ; Indirect addressing register
PSW == 3           ; Status register
PORT5 == 5
PORT6 == 6
RE == 0XE          ; Wake-up control register
RF == 0XF          ; Interrupt status register
```

B. Define a Control Register

```
IOC50 == 0X5       ; Control Register of Port 5
IOC60 == 0X6       ; Control Register of Port 6
C_INT == 0XF       ; Interrupt Control Register
```

C. ADC Control Register

```

ADDATA == 0xB      ; The contents are the results of ADC
AISR == 0x08      ; ADC Input select register
ADCON == 0x9      ; 7   6   5   4   3   2   1   0
                   ; VREFS CKR1 CKR0 ADRUN ADPD ADIS2 ADIS1 ADIS0

```

D. Define Bits in ADCON

```

ADRUN == 0x4      ; ADC is executed as the bit is set
ADPD == 0x3      ; Power Mode of ADC

```

E. Program Starts

```

ORG 0              ; Initial address
JMP INITIAL       ;

ORG 0x08          ; Interrupt vector
;
;
; (User program section)
;
;
CLR RF            ; To clear the ADIF bit
BS ADCON, ADRUN  ; To start to execute the next AD conversion
                  ; if necessary

RETI
INITIAL:
MOV A, @0B00000001 ; To define P60 as an analog input
MOV AISR, A
MOV A, @0B00001000 ; To select P60 as an analog input channel, and
                  ; AD power on
MOV ADCON, A      ; To define P60 as an input pin and set clock
                  ; rate at fosc/16

En_ADC:
MOV A, @0BXXXXXXX1 ; To define P50 as an input pin, and the others

IOW PORT6        ; are dependent on applications
MOV A, @0BXXXX1XXX ; Enable the ADWE wake-up function of ADC, "X"
                  ; by application

MOV RE, A
MOV A, @0BXXXX1XXX ; Enable the ADIE interrupt function of ADC,
                  ; "X" by application

IOW C_INT
ENI              ; Enable the interrupt function

BS ADCON, ADRUN ; Start to run the ADC

; If the interrupt function is employed, the following three lines
; may be ignored

POLLING:
JBC ADCON, ADRUN ; To check the ADRUN bit continuously;
JMP POLLING      ; ADRUN bit will be reset as the AD conversion
                  ; is completed

;
;
; (User program section)
;
;

```

6.8 PWM (Pulse Width Modulation)

6.8.1 Overview

In PWM mode, PWM1, PWM2, and PWM3 pins produce up to a 10-bit resolution PWM output (see the functional block diagram below). A PWM output consisted of a time period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the time period. Figure 6-11 (PWM Output Timing) depicts the relationships between a time period and a duty cycle.

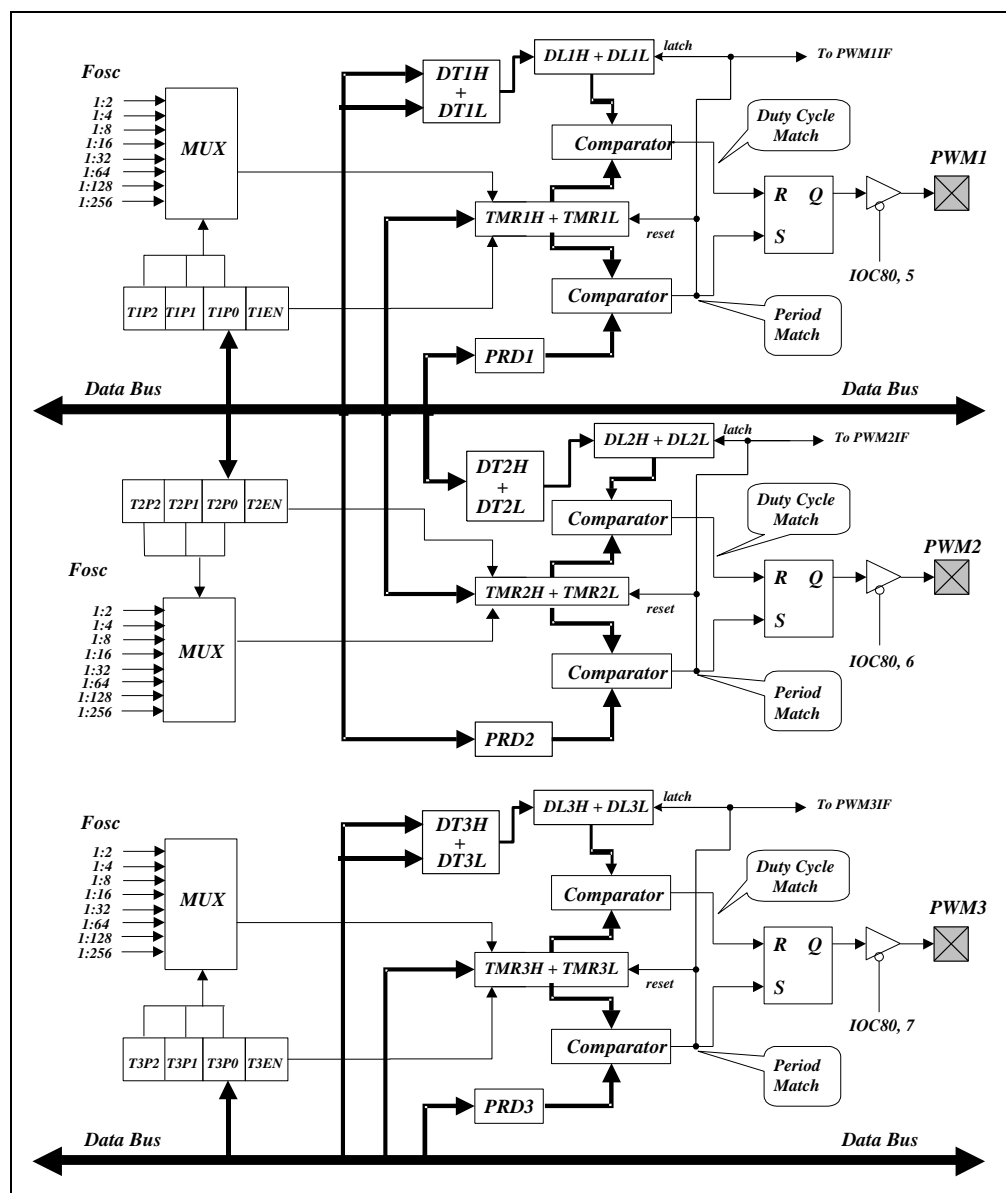


Figure 6-10 Three PWMs Functional Block Diagram

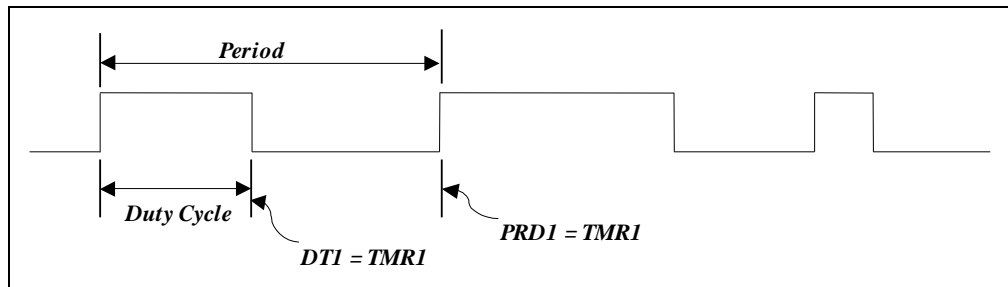


Figure 6-11 PWM Output Timing

6.8.2 Increment Timer Counter (TMRX: TMR1H/TWR1L, TMR2H/TWR2L, or TMR3H/TWR3L)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. If employed, such can be turned off to conserve power by setting the T1EN bit [IOC80<3>], T2EN bit [IOC90<6>] or T3EN bit [IOC90<7>] to 0.

6.8.3 PWM Time Period (PRDX: PRD1 or PRD2)

The PWM time period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared
- The PWMX pin is set to 1
- The PWM duty cycle is latched from DT1/DT2/DT3 to DL1/DL2/DL3

NOTE

The PWM output will not be set if the duty cycle is 0.

- The PWMXIF pin is set to 1

The following formula shows how to calculate the PWM time period:

$$\text{PERIOD} = (\text{PRDX} + 1) * 4 * (1/\text{Fosc}) * \text{CLKS}/2 * (\text{TMRX prescale value})$$

Example:

PRDX=49; Fosc=4MHz; CLKS bit of Code Option Register =0 (2 oscillator periods); TMRX (0,0,0)=1:2, then PERIOD=(49 + 1) * 4 * (1/4M) * 2/2 * 2 =100us



6.8.4 PWM Duty Cycle (DTX: DT1H/DT1L, DT2H/DT2L and DT3H/DT3L; DLX: DL1H/DL1L, DL2H/DL2L and DL3H/DL3L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula shows how to calculate the PWM duty cycle:

$$\text{Duty Cycle} = (\text{DTX}) * (1/\text{Fosc}) * \text{CLKS}/2 * (\text{TMRX prescale value})$$

Example:

DTX=10; Fosc=4MHz; CLKS bit of Code Option Register =0 (2 oscillator periods); TMRX (0,0,0)=1:2, then Duty Cycle=10 * (1/4M) * 2/2 * 2 =5us

6.8.5 Comparator X

Changing the output status while a match occurs will simultaneously set the TMRXIF flag.

6.8.6 PWM Programming Process/Steps

Load PRDX with the PWM time period.

1. Load DTX with the PWM Duty Cycle.
2. Enable interrupt function by writing IOCF0, if required.
3. Set PWMX pin to be output by writing a desired value to IOC80.
4. Load a desired value to IOC51 with TMRX prescaler value and enable both PWMX and TMRX.

6.9 Timer

6.9.1 Overview

Timer 1 (TMR1), Timer 2 (TMR2), and Timer 3 (TMR3) (TMRX) are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. The Timer 1, Timer 2, and Timer 3 will stop running when sleep mode occurs with AD conversion not running. However, if AD conversion is running when sleep mode occurs, the Timer 1, Timer 2 and Timer 3 will keep on running.

6.9.2 Function Description

The following figure shows the TMRX block diagram with descriptions of its signals and blocks:

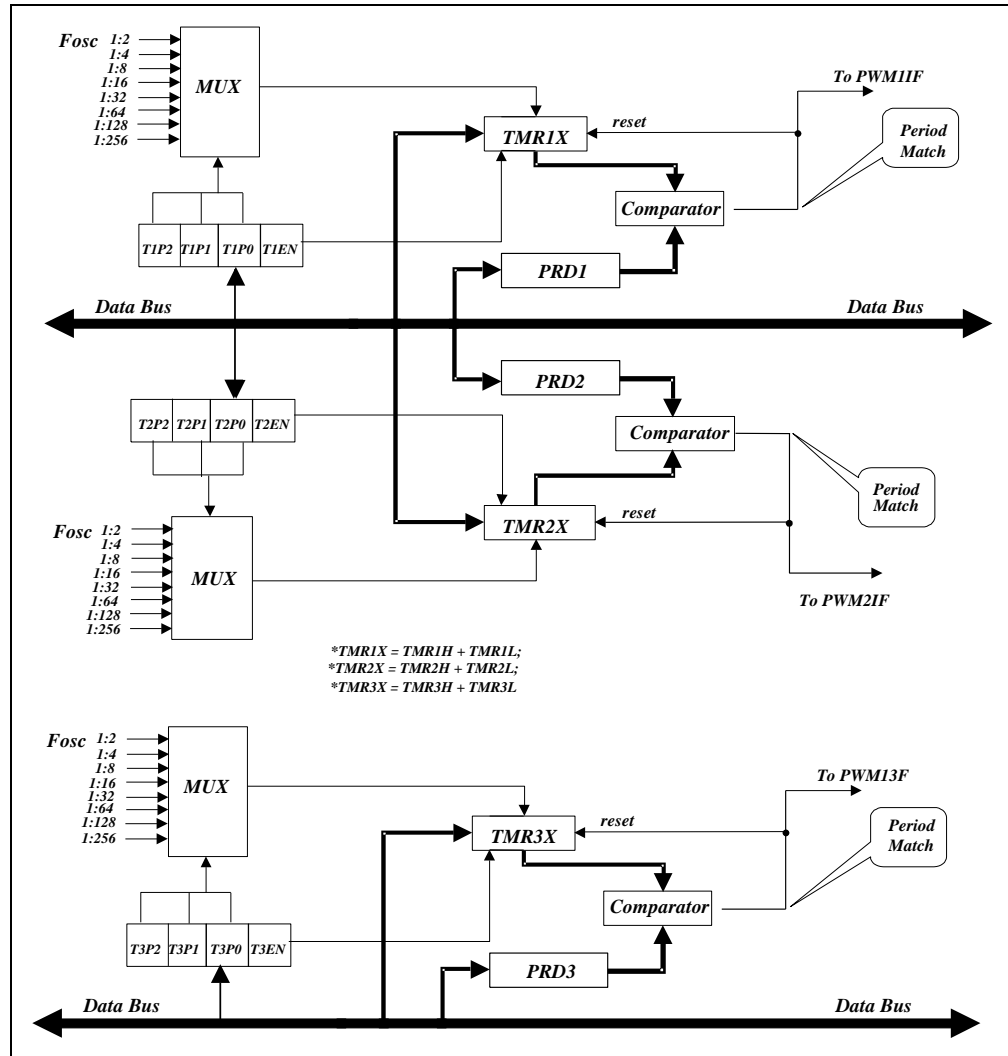


Figure 6-12 TMRX Block Diagram

Fosc: Input clock

Prescaler (T1P2, T1P1 and T1P0 / T2P2, T2P1 and T2P0 / T3P2, T3P1 and T3P0):

The options 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256 are defined by TMRX. It is cleared when any type of reset occurs.

TMR1X, TMR2X and TMR3X (TMR1H/TMR1L, TMR2H/TMR2L, and TMR3H/TMR3L): Timer X register; TMRX is increased until it matches with PRDX, and then is reset to 1 (default value).

PRDX (PRD1, PRD2 and PRD3): PWM time period register.

Comparator X (Comparator 1 and Comparator 2):

Reset TMRX while a match occurs. The TMRXIF flag is set at the same time.

6.9.3 Programming the Related Registers

When defining TMRX, refer to the related registers of its operation as shown in the table below. It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, Bit 7 ~ Bit 5 of the PWMCON register must be set to '0'.

6.9.3.1 Related Control Registers of TMR1, TMR2, and TMR3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC80	PWMCON/IOC80	PWM3E	PWM2E	PWM1E	"0"	T1EN	T1P2	T1P1	T1P0
IOC90	TMRCON/IOC90	T3EN	T2EN	T3P2	T3P1	T3P0	T2P2	T2P1	T2P0

6.9.4 Timer Programming Process/Steps

1. Load PRDX with the Timer duration.
2. Enable interrupt function by writing IOCF0, if required.
3. Load a desired TMRX prescaler value to PWMCON and TMRCON, enable TMRX and disable PWMX.

6.10 Comparator

The EM78P418N has one comparator comprising of two analog inputs and one output. The comparator can be utilized to wake up the EM78P418N from sleep mode. The comparator circuit diagram is depicted in the figure below.

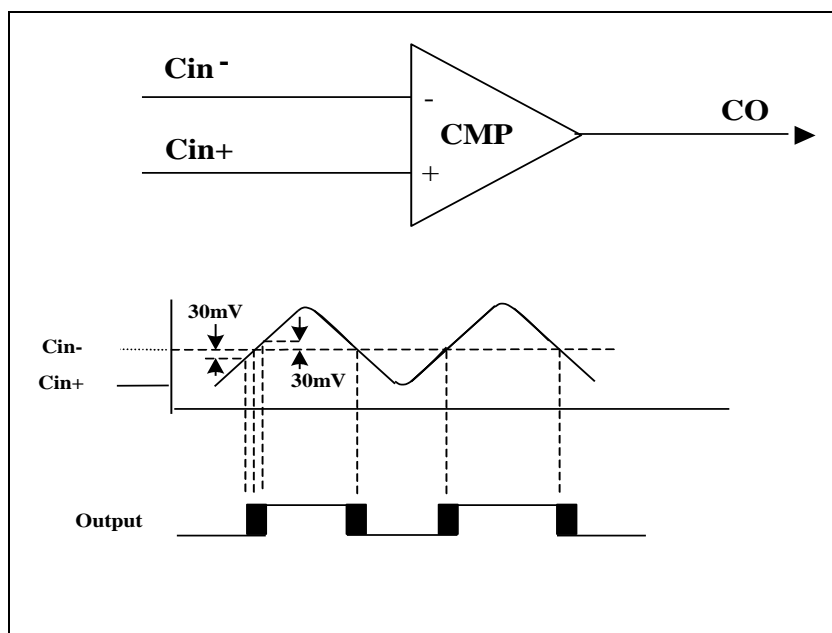


Figure 6-13 Comparator Circuit Diagram and Operation Mode

6.10.1 External Reference Signal

The analog signal that is presented at Cin- is compared to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations:

NOTE

- The reference signal must be between Vss and Vdd.
- The reference voltage can be applied to either pin of the comparator.
- Threshold detector applications may be of the same reference.
- The comparator can operate from the same or different reference sources.

6.10.2 Comparator Output

- The compared result is stored in the CMPOUT of IOCA0.
- The comparator outputs are sent to CO (P60) by programming Bit 1, Bit 0 <COS1, COS0> of the IOCA0 register to <1, 0>. See Section 6.2.6, IOCA0 (CMPCON: Comparator Control Register) for Comparator/OP select bits function description.

NOTE

- The CO and ADE0 of the P60/ADE0/CO pins cannot be used at the same time.
- The P60/ADE0/CO pin priority is as follows:

P60/ADE0/CO Priority		
High	Medium	Low
CO	ADE0	P60

The following figure shows the Comparator Output block diagram.

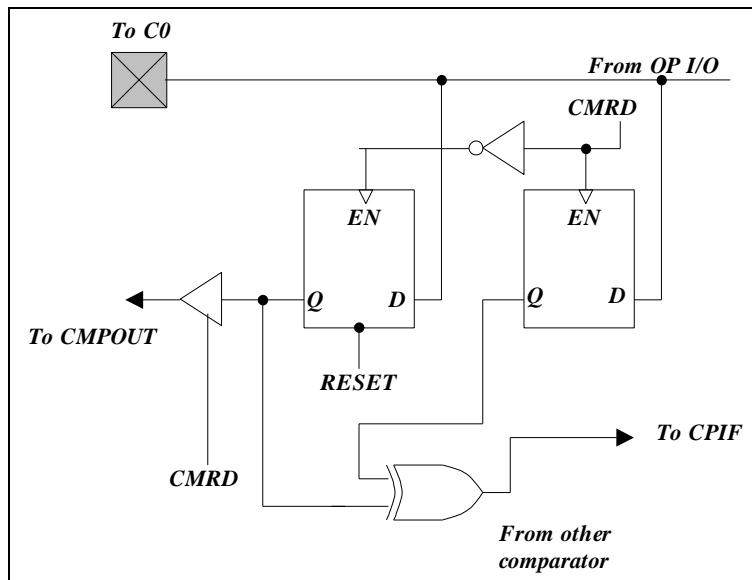


Figure 6-14 Comparator Output Configuration



6.10.3 Using a Comparator as an Operation Amplifier

The comparator can be used as an operation amplifier if a feedback resistor is connected from the input to the output externally. In this case, the Schmitt Trigger can be disabled for power saving by setting Bit 1, Bit 0<COS1, COS0> of the IOCA0 register to <1, 1>. See Section 6.2.6, IOCA0 (CMPCON: Comparator Control Register) for Comparator/OP select bits function description.

6.10.4 Comparator Interrupt

- CMPIE (IOCF0.7) must be enabled for the “ENI” instruction to take effect.
- Interrupt is triggered whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading the Bit CMPOUT, IOCA0<2>.
- CMPIF (RF.7), the comparator interrupt flag, can only be cleared by software.

6.10.5 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

6.11 Oscillator

6.11.1 Oscillator Modes

The EM78P418N can be operated in four different oscillator modes, such as High Crystal oscillator mode (HXT), Low Crystal oscillator mode (LXT), External RC oscillator mode (ERC), and RC oscillator mode with Internal RC oscillator mode (IRC). Select one of them by programming the OSC2, OCS1, and OSC0 in the Code Option register.

The Oscillator modes defined by OSC2, OCS1, and OSC0 are described below.

Oscillator Modes	OSC2	OSC1	OSC0
ERC ¹ (External RC oscillator mode); P54/OSCO is configured as P54	0	0	0
ERC ¹ (External RC oscillator mode); P54/OSCO is configured as OSCO	0	0	1
IRC ² (Internal RC oscillator mode); P54/OSCO is configured as P54	0	1	0
IRC ² (Internal RC oscillator mode); P54/OSCO is configured as OSCO	0	1	1
LXT ³ (Low Crystal oscillator mode)	1	1	0
HXT ³ High Crystal oscillator mode) (default)	1	1	1

NOTE

After waking up from Sleep 2 mode, WDT is automatically enabled. The WDT enable/disable operation after waking up from Sleep 2 mode should be properly defined in the software. The transient point of the system frequency between HXT and LXY is 400kHz

- 1** In ERC mode, OSCI is used as oscillator pin. OSCO/P54 is defined by Code Option Word 0 Bit 6 ~ Bit 4.
- 2** In IRC mode, P55 is a normal I/O pin. OSCO/P54 is defined by Code Option Word 0 Bit 6 ~ Bit 4
- 3** In LXT and HXT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins

The maximum operating frequency limits of the crystal/resonator at different VDDs are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.3	4
	3.0	8
	5.0	20

6.11.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P418N can be driven by an external clock signal through the OSCI pin as illustrated below.

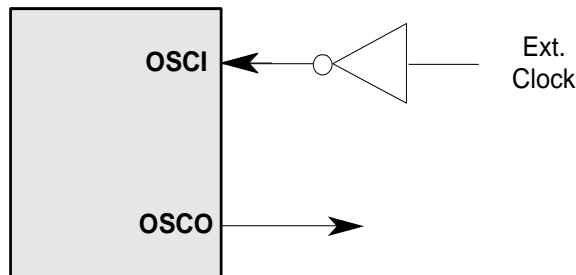


Figure 6-15 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-16 below depicts such a circuit. The same applies to the HXT mode and the LXT mode.

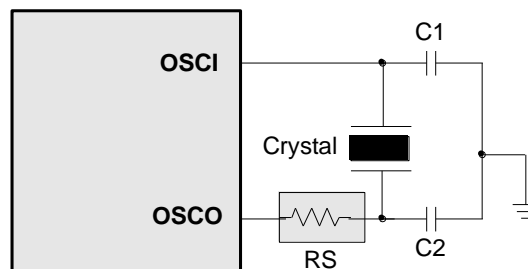


Figure 6-16 Crystal/Resonator Circuit



The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, refer to the resonator specifications for appropriate values of C1 and C2. RS, a serial resistor, may be required for AT strip cut crystal or low frequency mode.

Capacitor selection guide for crystal oscillator or ceramic resonators:

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

6.11.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Figure 6-17) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

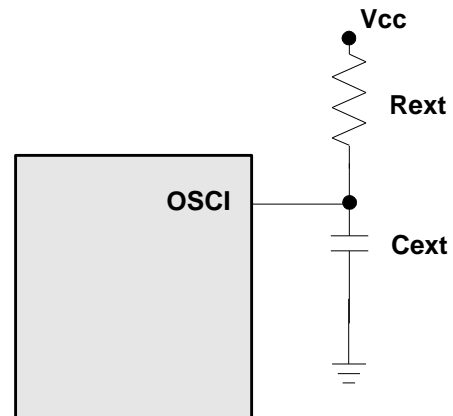


Figure 6-17 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should be not less than 20pF, and the value of Rext should be not greater than 1 MΩ. If the frequency cannot be kept within this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot discharge the capacitance current correctly.

Based on the stated facts, it must be kept in mind that all supply voltage, operation temperature, components of the RC oscillator, package types, and the PCB layout has certain effects on the system frequency.

The RC Oscillator frequencies:

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140 kHz	140kHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850kHz	820kHz
	10k	450kHz	450kHz
	100k	48kHz	50kHz
300 pF	3.3k	560kHz	540kHz
	5.1k	370kHz	360kHz
	10k	196kHz	192kHz
	100k	20kHz	20kHz

Note: ¹: Measured based on DIP packages.
²: The values are for design reference only.
³: The frequency drift is $\pm 30\%$.

6.11.4 Internal RC Oscillator Mode

The EM78P418N offers a versatile internal RC mode with default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (1 MHz, 8 MHz, and 455kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. Table below describes the EM78P418N internal RC drift with the variation of voltage, temperature, and process.

Internal RC Drift Rate ($T_a=25^\circ\text{C}$, $V_{DD}=5\text{V}\pm 5\%$, $V_{SS}=0\text{V}$)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.3V~5.5V)	Process	Total
4 MHz	$\pm 10\%$	$\pm 5\%$	$\pm 4\%$	$\pm 19\%$
8 MHz	$\pm 10\%$	$\pm 6\%$	$\pm 4\%$	$\pm 20\%$
1 MHz	$\pm 10\%$	$\pm 5\%$	$\pm 4\%$	$\pm 19\%$
455kHz	$\pm 10\%$	$\pm 5\%$	$\pm 4\%$	$\pm 19\%$

Note: These are theoretical values which are provided for reference only. Actual values may vary depending on the actual process.

6.12 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply has stabilized.

The EM78P418N has an on-chip Power-on Voltage Detector (POVD) with detection level range of 1.9V to 2.1V. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises quickly enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.12.1 External Power-on Reset Circuit

The circuits shown in the following figure implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to reach the minimum operating voltage. This circuit is used when the power supply has a slow power rise time. Since

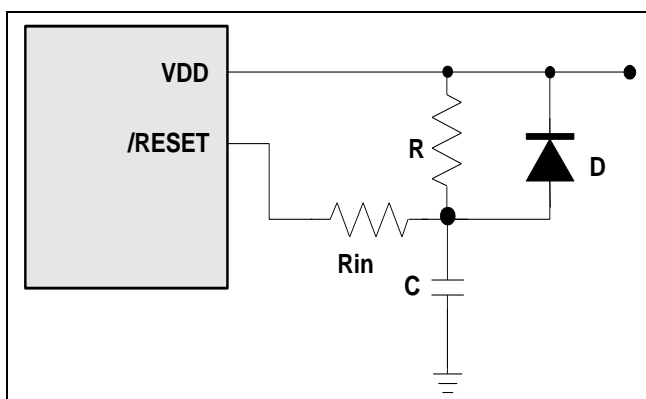


Figure 6-18 External Power-on Reset Circuit

the current leakage from the /RESET pin is $\pm 5\mu\text{A}$, it is recommended that R should not be greater than 40 K. This way, the voltage at Pin /RESET is held below 0.2V. The diode (D) functions as a short circuit at power-down. The “C” capacitor is discharged quickly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

6.12.2 Residual Voltage Protection

When the battery is replaced, device power (Vdd) is removed but residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-16 and Figure 6-20 show how to create a protection circuit against residual voltage.

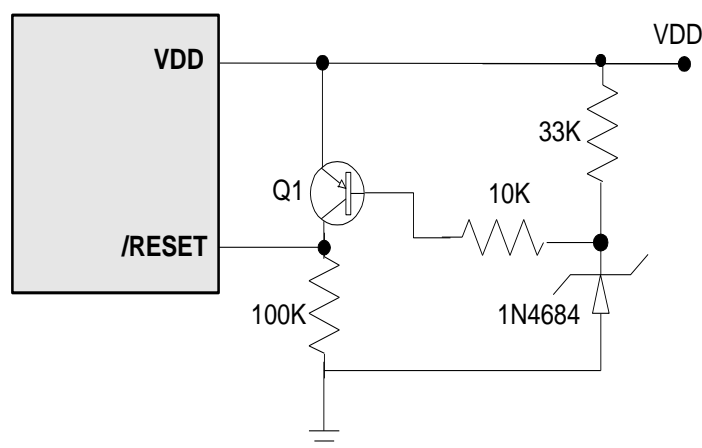


Figure 6-19 Residual Voltage Protection Circuit 1

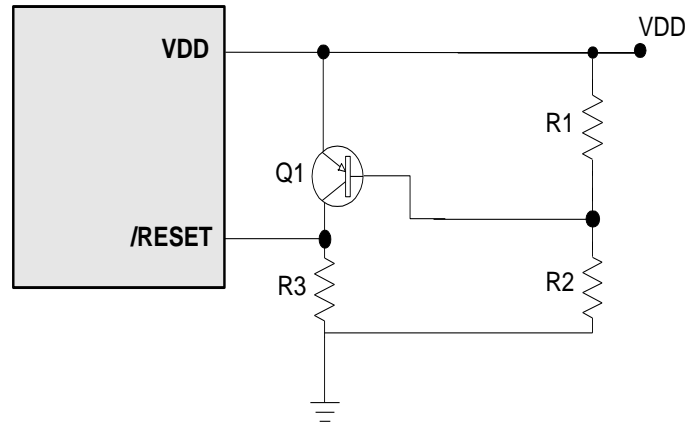


Figure 6-20 Residual Voltage Protection Circuit 2

6.13 Code Option

The EM78P418N has two Code Option Words and one Customer ID word that are not part of the normal program memory.

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.13.1 Code Option Register (Word 0)

Word 0									
Bit	Bit 12 ~ Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 ~ Bit 0
Mnemonic	–	TYPE	CLKS	ENWDTB	OSC2	OSC1	OSC0	HLP	Protect
1	–	High	4 clocks	Disable	High	High	High	High	Disable
0	–	Low	2 clocks	Enable	Low	Low	Low	Low	Enable

Bits 12 ~ 10: Not used (reserved). These bits are set to “1” all the time.

Bit 9 (TYPE): Type selection Pin.

0: EM78P418N-24Pin

1: EM78P418N-18Pin/EM78P418N-20Pin (default)

Bit 8 (CLKS): Instruction time period option bit

0: two oscillator time periods

1: four oscillator time periods (default)

Refer to the Section 6.15 for Instruction Set

Bit 7 (ENWDTB): Watchdog timer enable bit

0: Enable

1: Disable (default)



Bits 6, 5 and 4 (OSC2, OSC1 and OSC0): Oscillator Modes Select bits

Oscillator Modes	OSC2	OSC1	OSC0
ERC ¹ (External RC oscillator mode); P54/OSCO is configured as P54	0	0	0
ERC ¹ (External RC oscillator mode); P54/OSCO is configured as OSCO	0	0	1
IRC ² (Internal RC oscillator mode); P54/OSCO is configured as P54	0	1	0
IRC ² (Internal RC oscillator mode); P54/OSCO is configured as OSCO	0	1	1
LXT ³ (Low Crystal oscillator mode)	1	1	0
HXT ³ High Crystal oscillator mode) (default)	1	1	1

Note: The transient point of the system frequency between HXT and LXT is 400kHz.

¹ In ERC mode, OSC1 is used as oscillator pin. OSCO/P54 is defined by code option Word 0 Bit 6 ~ Bit 4.

² In IRC mode, P55 is normal I/O pin. OSCO/P54 is defined by code option Word 0 Bit 6 ~ Bit 4.

³ In LXT and HXT modes; OSC1 and OSC0 are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

Bit 3 (HLP): Power consumption selection

0: Low power consumption, applies to working frequency at 4 MHz or below 4MHz

1: High power consumption, applies to working frequency above 4MHz

Bits 2 ~ 0 (Protect): Protect Bits

0: Enable

1: Disable

6.13.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	NRHL	NRE	CYES	C3	C2	C1	C0	RCM1	RCM0
1	-	-	-	-	32/fc	Enable	2cycles	High	High	High	High	High	High
0	-	-	-	-	8/fc	Disable	1cycle	Low	Low	Low	Low	Low	Low

Bits 12 ~ 9: Not used (reserved). These bits are set to “1” all the time.

Bit 8 (NRHL): Noise rejection high/low pulses define bit. The INT pin are falling or rising edge triggered.

0: Pulses equal to 8/fc [s] are regarded as signal

1: Pulses equal to 32/fc [s] are regarded as signal (default)

NOTE

The noise rejection function is turned off under the LXT and sleep mode.

Bit 7 (NRE): Noise rejection enabled

0: Disable noise rejection

1: Enable noise rejection (default). However in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bit 6 (CYES): Instruction cycle selection bit

0: One instruction cycle

1: Two instruction cycles (default)

Bits 5, 4, 3 and Bit 2 (C3, C2, C1, and C0): Calibration bits of internal RC mode. These bits must always be set to “1” only (auto calibration)

Bit 1 and Bit 0 (RCM1 and RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	8
0	1	1
0	0	455kHz

6.13.3 Customer ID Register (Word 2)

Word 2												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x

Bits 12 ~ 0: Customer's ID code



6.14 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator time periods), unless the program counter is changed by instructions "MOV R2,A," "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.). In this case, these instructions need one or two instruction cycles as determined by Code Option Register CYES bit.

In addition, the instruction set has the following features:

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

The following symbols are used in the Instruction Set table:

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None ¹
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None ¹
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z



Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0010 00rr rrrr	02rr	OR A,R	$A \vee VR \rightarrow A$	Z
0 0010 01rr rrrr	02rr	OR R,A	$A \vee VR \rightarrow R$	Z
0 0010 10rr rrrr	02rr	AND A,R	$A \& R \rightarrow A$	Z
0 0010 11rr rrrr	02rr	AND R,A	$A \& R \rightarrow R$	Z
0 0011 00rr rrrr	03rr	XOR A,R	$A \oplus R \rightarrow A$	Z
0 0011 01rr rrrr	03rr	XOR R,A	$A \oplus R \rightarrow R$	Z
0 0011 10rr rrrr	03rr	ADD A,R	$A + R \rightarrow A$	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	$A + R \rightarrow R$	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	$R \rightarrow A$	Z
0 0100 01rr rrrr	04rr	MOV R,R	$R \rightarrow R$	Z
0 0100 10rr rrrr	04rr	COMA R	$/R \rightarrow A$	Z
0 0100 11rr rrrr	04rr	COM R	$/R \rightarrow R$	Z
0 0101 00rr rrrr	05rr	INCA R	$R+1 \rightarrow A$	Z
0 0101 01rr rrrr	05rr	INC R	$R+1 \rightarrow R$	Z
0 0101 10rr rrrr	05rr	DJZA R	$R-1 \rightarrow A$, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	$R-1 \rightarrow R$, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	$R(n) \rightarrow A(n-1), R(0) \rightarrow C, C \rightarrow A(7)$	C
0 0110 01rr rrrr	06rr	RRC R	$R(n) \rightarrow R(n-1), R(0) \rightarrow C, C \rightarrow R(7)$	C
0 0110 10rr rrrr	06rr	RLCA R	$R(n) \rightarrow A(n+1), R(7) \rightarrow C, C \rightarrow A(0)$	C
0 0110 11rr rrrr	06rr	RLC R	$R(n) \rightarrow R(n+1), R(7) \rightarrow C, C \rightarrow R(0)$	C
0 0111 00rr rrrr	07rr	SWAPA R	$R(0-3) \rightarrow A(4-7), R(4-7) \rightarrow A(0-3)$	None
0 0111 01rr rrrr	07rr	SWAP R	$R(0-3) \leftrightarrow R(4-7)$	None
0 0111 10rr rrrr	07rr	JZA R	$R+1 \rightarrow A$, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	$R+1 \rightarrow R$, skip if zero	None
0 100b brrr rrrr	0xxx	BC R,b	$0 \rightarrow R(b)$	None ²
0 101b brrr rrrr	0xxx	BS R,b	$1 \rightarrow R(b)$	None ³
0 110b brrr rrrr	0xxx	JBC R,b	if $R(b)=0$, skip	None
0 111b brrr rrrr	0xxx	JBS R,b	if $R(b)=1$, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	$PC+1 \rightarrow [SP], (Page, k) \rightarrow PC$	None
1 01kk kkkk kkkk	1kkk	JMP k	$(Page, k) \rightarrow PC$	None
1 1000 kkkk kkkk	18kk	MOV A,k	$k \rightarrow A$	None
1 1001 kkkk kkkk	19kk	OR A,k	$A \vee k \rightarrow A$	Z
1 1010 kkkk kkkk	1Akk	AND A,k	$A \& k \rightarrow A$	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	$A \oplus k \rightarrow A$	Z
1 1100 kkkk kkkk	1Ckk	RETL k	$k \rightarrow A, [Top\ of\ Stack] \rightarrow PC$	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	$k-A \rightarrow A$	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	$k+A \rightarrow A$	Z, C, DC

Note: ¹ This instruction is applicable to IOC50–IOC51, IOC51 ~ IOC51 only.

² This instruction is not recommended for RF operation.

³ This instruction cannot operate under RF.

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	V _{ss} -0.3V	to	V _{dd} +0.5V
Output voltage	V _{ss} -0.3V	to	V _{dd} +0.5V
Working Voltage	2.5V	to	5.5V
Working Frequency	DC	to	20 MHz

8 DC Electrical Characteristics

T_a = 25°C, V_{DD} = 5.0V, V_{SS} = 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	DC	–	20	MHz
	Crystal: VDD to 3V		DC	–	8	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	850	F±30%	kHz
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	3.5	–	V
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	1.5	–	V
IIL	Input Leakage Current for input pins	V _{IN} = V _{DD} , V _{SS}	–1.0	0	1.0	μA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7	–	3.75	–	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7	–	1.25	–	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	–	2.0	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	1.0	–	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	–	3.75	–	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	–	1.25	–	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.5	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.5	–	V
IOH1	Output High Voltage (Ports 5, 6, 7)	V _{OH} = V _{DD} -0.5V (I _{OH} = –6mA)	–	–6.0	–	mA
IOL1	Output Low Voltage (Ports 5, 6, 7)	V _{OL} = GND+0.5V (I _{OL} = 12mA)	–	12.0	–	mA
IPH	Pull-high current	Pull-high active, input pin at V _{SS}	–50	–75	–240	μA
IPL	Pull-low current	Pull-low active, input pin at V _{DD}	25	40	120	μA
ISB1	Power down current	All input and I/O pins at V _{DD} , Output pin floating, WDT disabled	–	1.0	2.0	μA
ISB2	Power down current	All input and I/O pins at V _{DD} , Output pin floating, WDT enabled	–	–	15	μA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type,CLKS="0"), Output pin floating, WDT disabled	15	20	35	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type,CLKS="0"), Output pin floating, WDT enabled	–	25	35	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	1.7	2.2	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	3.0	3.5	mA

Internal RC Electrical Characteristics (Ta=25°C, VDD=5V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.84 MHz	4 MHz	4.16 MHz
8 MHz	25°C	5V	7.68 MHz	8 MHz	8.32 MHz
1 MHz	25°C	5V	0.96 MHz	1 MHz	1.04 MHz
455kHz	25°C	5V	436.8kHz	455kHz	473.2kHz

Internal RC Electrical Characteristics (Ta=-40 ~85°C, VDD=2.2~5.5V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	-40 ~85°C	2.2~5.5V	3.24 MHz	4 MHz	4.76 MHz
8 MHz	-40 ~85°C	2.2~5.5V	6.4 MHz	8 MHz	9.6 MHz
1 MHz	-40 ~85°C	2.2~5.5V	0.81 MHz	1 MHz	1.19 MHz
455kHz	-40 ~85°C	2.2~5.5V	368kHz	455kHz	542kHz

8.1 AD Converter Characteristics

V_{dd}=2.5V to 5.5V, V_{ss}=0V, T_a=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VREF	Analog reference voltage	VREF – VSS ≥ 2.5V	2.5	–	VDD	V
VSS			VSS	–	VSS	V
VAI	Analog input voltage	–	VSS	–	VREF	V
IAI1	Analog supply current	VDD=VREF=5.0V, VSS = 0.0V (V reference from VDD)	750	850	1000	μA
			-10	0	+10	μA
IAI2	Analog supply current	VDD=VREF=5.0V, VSS = 0.0V (V reference from VREF)	500	600	820	μA
			200	250	300	μA
RN1	Resolution	ADREF=0, Internal VDD VDD=5.0V, VSS = 0.0V	–	9	10	Bits
RN2	Resolution	ADREF=1, External VREF VDD=VREF=5.0V, VSS = 0.0V	–	11	12	Bits
LN1	Linearity error	VDD= 2.5 to 5.5V T _a =25°C	0	± 4	± 8	LSB
LN2	Linearity error	VDD= 2.5 to 5.5V T _a =25°C	0	± 2	± 4	LSB
DNL	Differential non-linear error	VDD= 2.5 to 5.5V T _a =25°C	0	± 0.5	± 0.9	LSB
FSE1	Full scale error	VDD=5.0V, V _{SS} = 0.0V	± 0	± 4	± 8	LSB
FSE2	Full scale error	VDD=VREF=5.0V, VSS = 0.0V	± 0	± 2	± 4	LSB
OE	Offset error	VDD=VREF=5.0V, VSS = 0.0V	± 0	± 2	± 4	LSB
ZAI	Recommended impedance of analog voltage source	–	0	8	10	KΩ
ADIV	A/D input voltage range	VDD =VREF=5.0V, VSS = 0.0V	0	–	VREF	V
ADOV	A/D output voltage swing	VDD =VREF=5.0V, VSS = 0.0V, RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
TAD	A/D clock period	VDD=VREF=5.0V, VSS = 0.0V	4	–	–	μs
TCN	A/D conversion time	VDD=VREF=5.0V, VSS = 0.0V	15	–	15	TAD
PSR	Power Supply Rejection	VDD=5.0V ± 0.5V	± 0	–	± 2	LSB

- Note:**
1. These parameters are hypothetical (not tested) and are provided for design reference only.
 2. There is no current consumption when ADC is off other than minor leakage current.
 3. AD conversion result will not decrease when the input voltage is increased, and no missing code will result.
 4. These parameters are subject to change without further notice.

8.2 Comparator (OP) Characteristics

V_{dd} = 5.0V, V_{ss}=0V, T_a=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SR	Slew rate	–	0.1	0.2	–	V/μs
IVR	Input voltage range	V _{dd} =5.0V, V _{SS} =0.0V	0	–	5	V
OVS	Output voltage swing	V _d =5.0V, V _{SS} =0.0V, R _L =10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
I _{op}	Supply current of OP	–	250	350	500	μA
I _{co}	Supply current of Comparator	–	–	300	–	μA
PSRR	Power-supply Rejection Ration for OP	V _{dd} = 5.0V, V _{SS} =0.0V	50	60	70	dB
V _s	Operating range	–	2.5	–	5.5	V

Note: 1. These parameters are hypothetical (not tested) and are provided for design reference only.
2. These parameters are subject to change without further notice.

8.3 Device Characteristics

The graphs below were derived based on a limited number of samples and they are provided for reference only. Hence, the device characteristic shown herein cannot be guaranteed as fully accurate. In these graphs, the data maybe out of the specified operating warranted range.

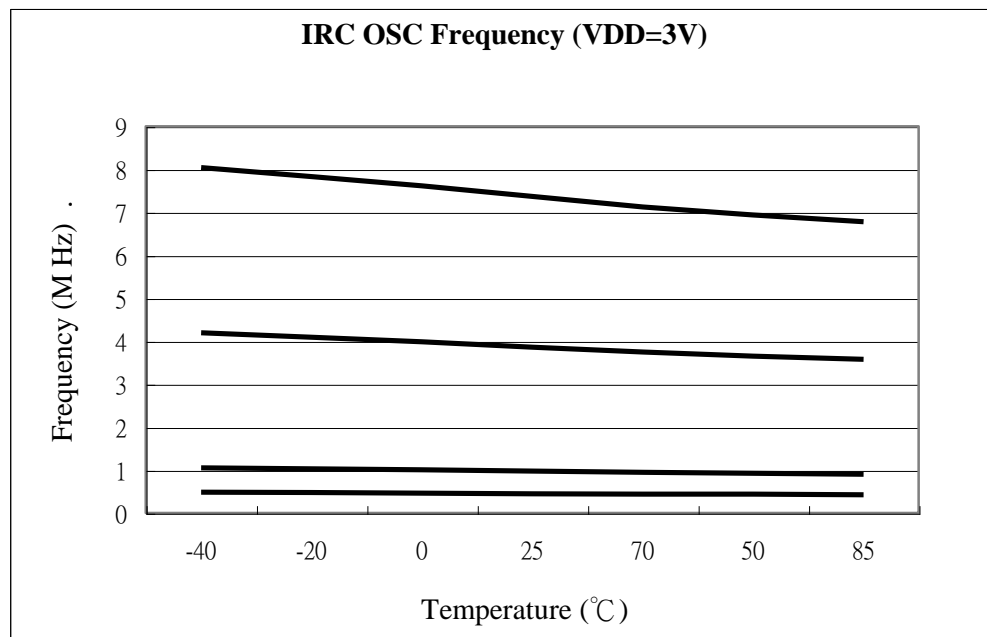


Figure 8-1 Internal RC OSC Frequency vs. Temperature, V_{DD}=3V

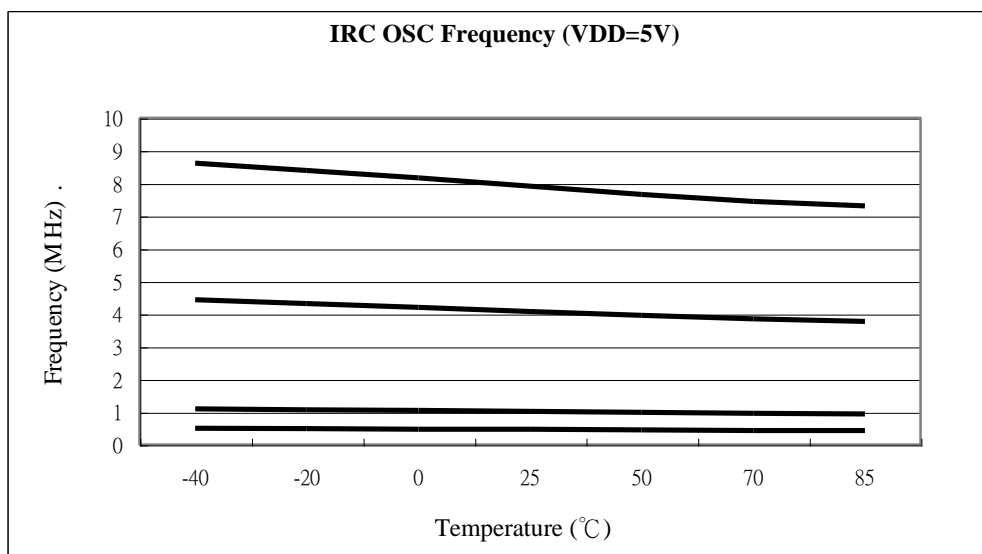


Figure 8-2 Internal RC OSC Frequency vs. Temperature, VDD=5V

9 AC Electrical Characteristics

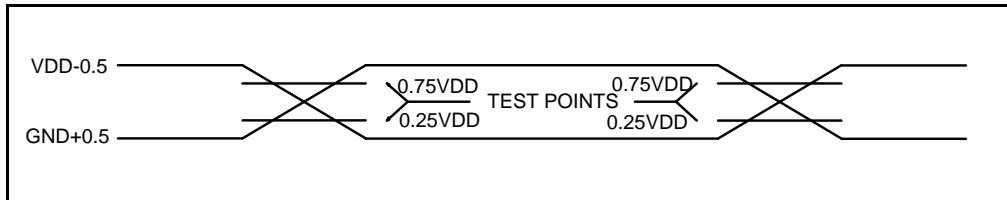
Ta=25°C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input time period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer duration	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns
Tdrc	ERC delay time	Ta = 25°C	1	3	5	ns

Note: * N = selected prescaler ratio

10 Timing Diagrams

AC Test Input/Output Waveform



Note: AC Testing: Input are driven at $VDD-0.5V$ for logic "1," and $GND+0.5V$ for logic "0"
Timing measurements are made at $0.75VDD$ for logic "1," and $0.25VDD$ for logic "0"

Figure 10-1a AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK="0")

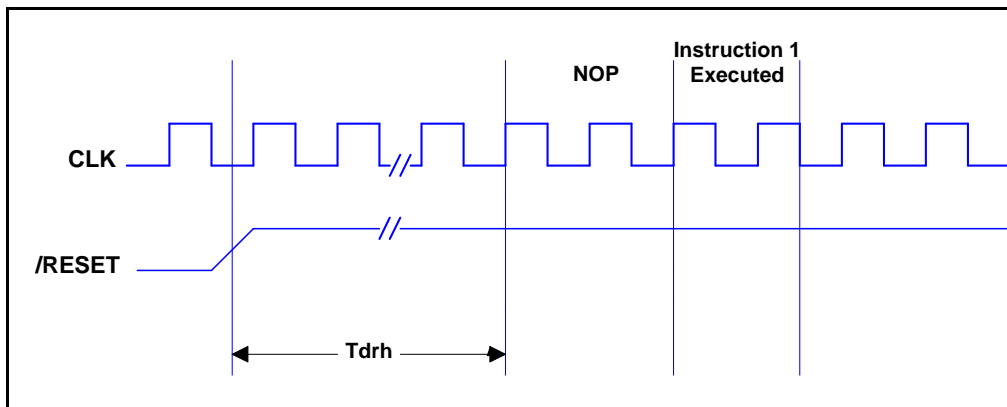


Figure 10-1b Reset Timing Diagram

TCC Input Timing (CLKS="0")

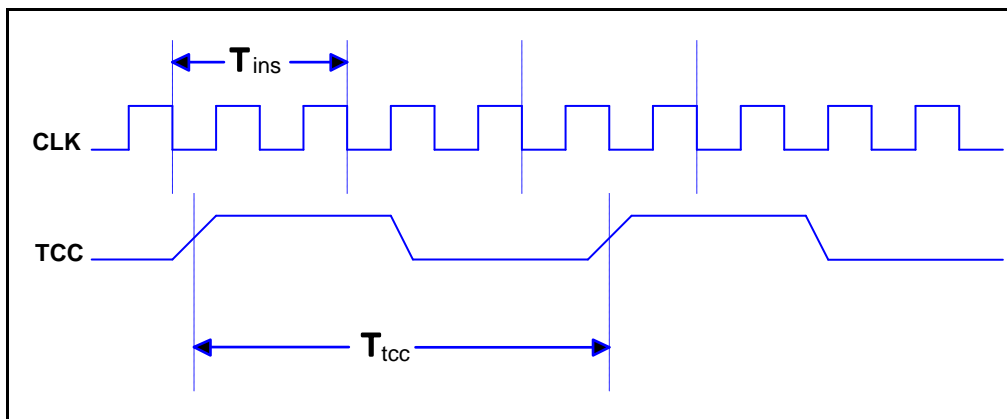


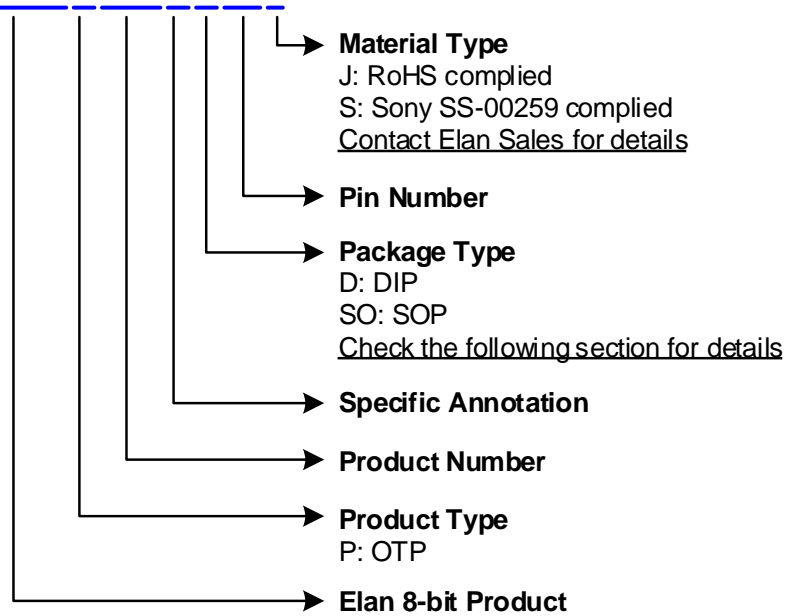
Figure 10-1c TCC Input Timing Diagram



APPENDIX

A Ordering and Manufacturing Information

EM78P418ND18J

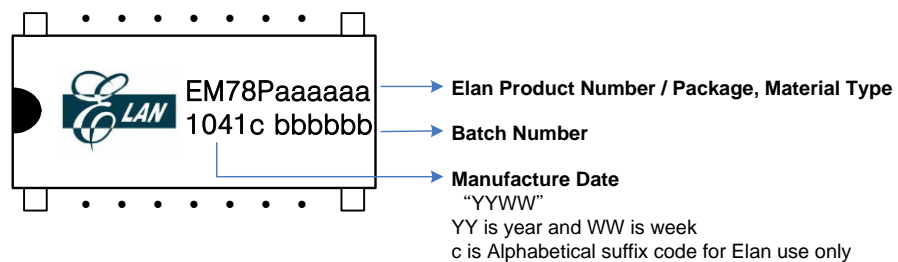


For example:

EM78P418ND18S

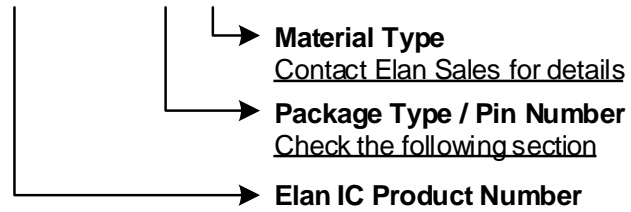
is EM78P418N with OTP program memory,
in 18-pin DIP 300mil package with Sony SS-00259 complied

IC Mark



Ordering Code

EM78P418ND18J





B Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P418ND18	DIP	18 pins	300 mil
EM78P418NSO18	SOP	18 pins	300 mil
EM78P418ND20	DIP	20 pins	300 mil
EM78P418NSO20	SOP	20 pins	300 mil
EM78P418NK24	Skinny DIP	24 pins	300 mil
EM78P418NSO24	SOP	24 pins	300 mil
EM78P418NSS24	SSOP	24 pins	150 mil

These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb contents less is than 100ppm and complies with Sony specifications.

Part No.	EM78P418NS/J
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity ($\mu\Omega$ -cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Package Information

C.1 EM78P418ND18

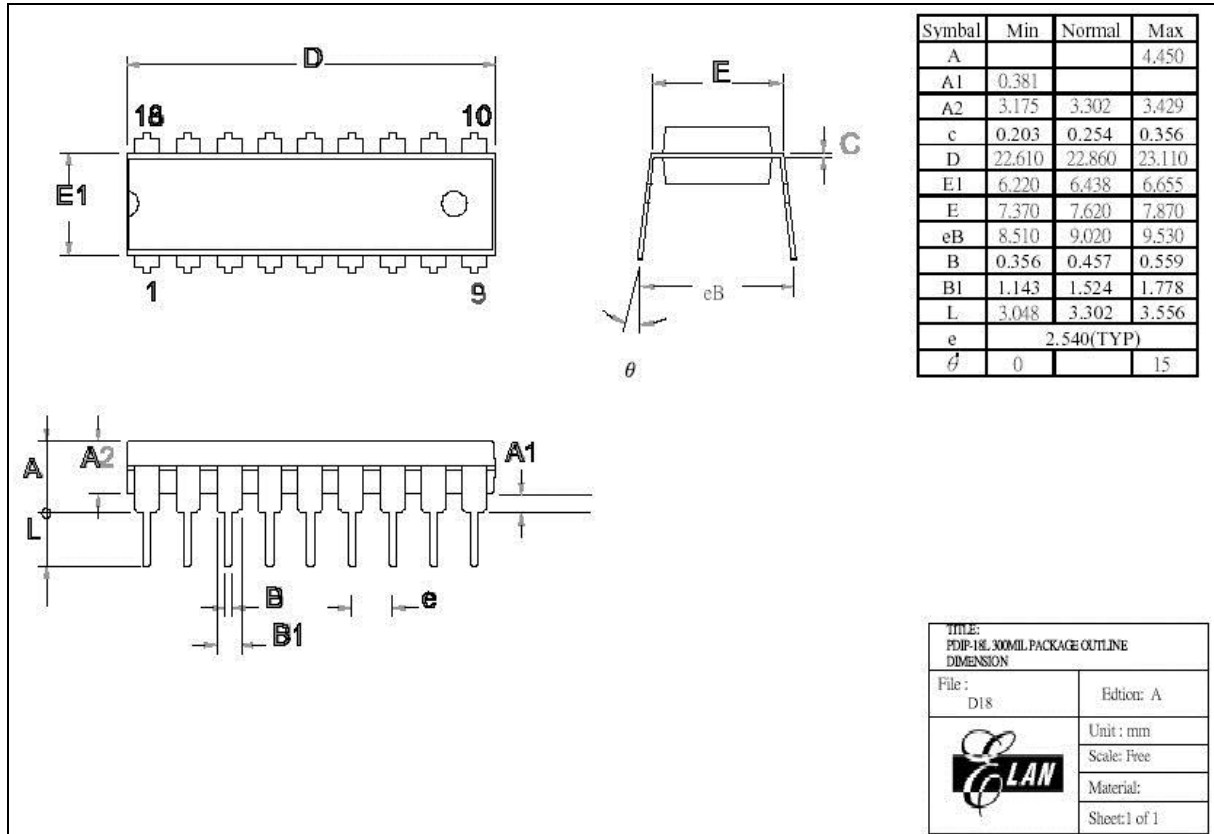


Figure C-1 EM78P418N 18-pin DIP Package Type

C.2 EM78P418NSO18

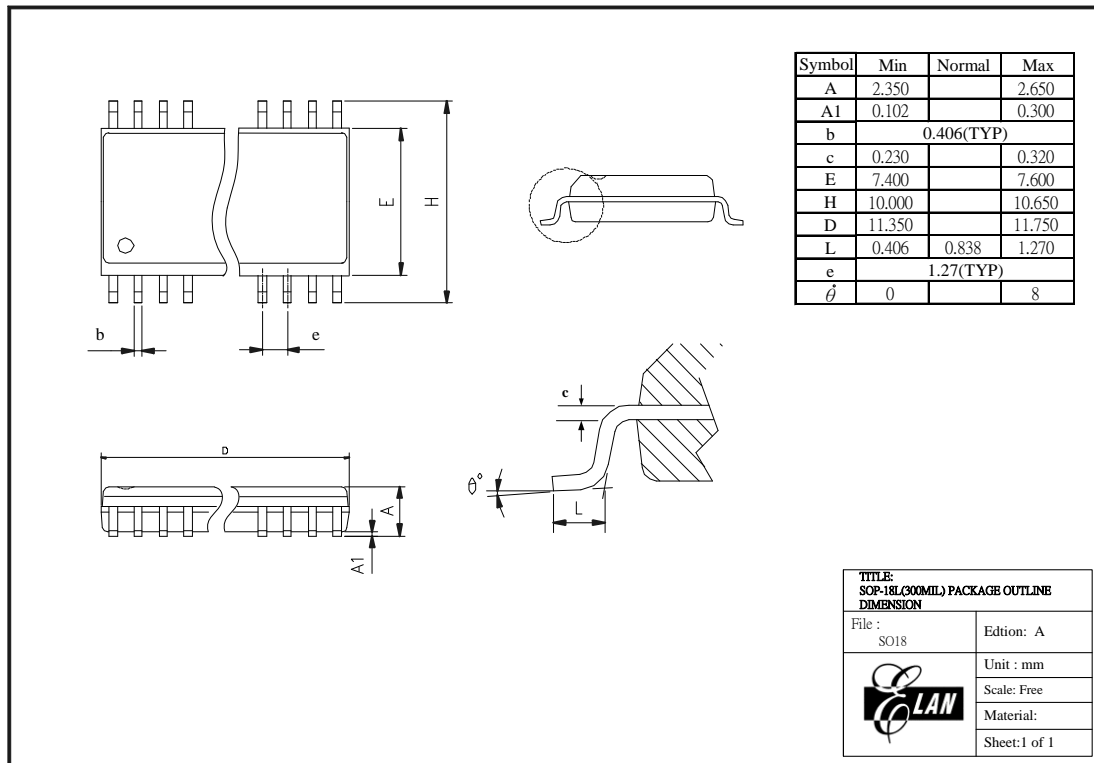


Figure C-2 EM78P418N 18-pin SOP Package Type

C.3 EM78P418ND20

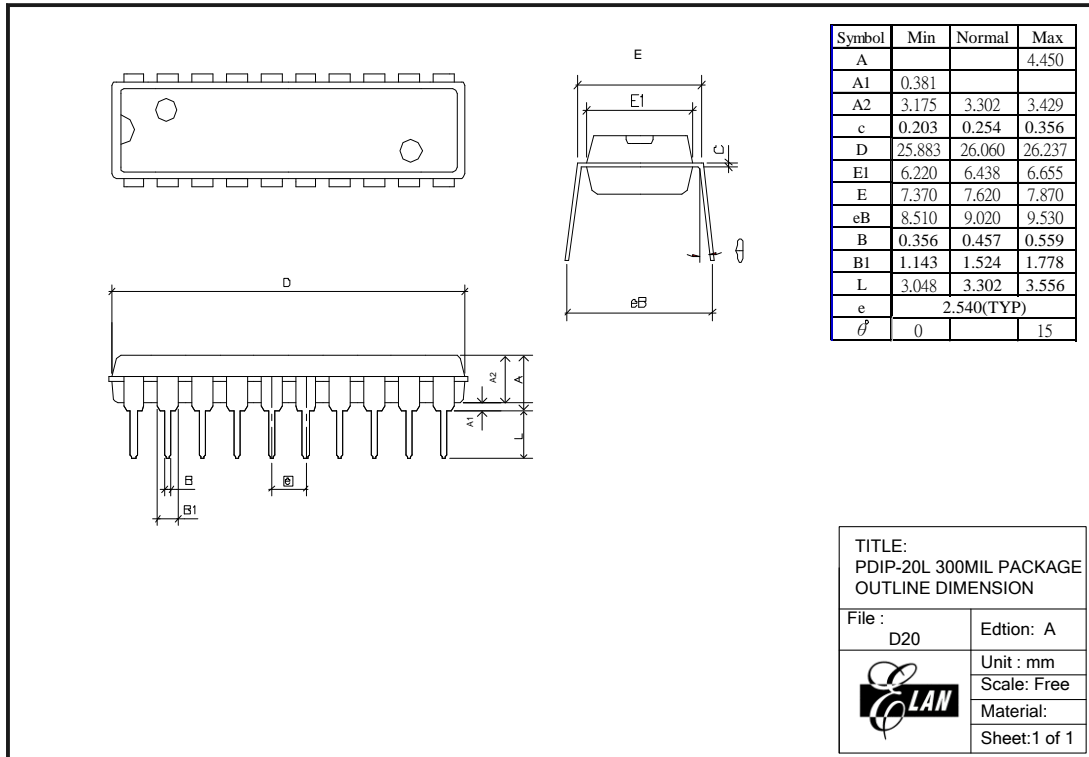


Figure C-3 EM78P418N 20-pin DIP Package Type

C.4 EM78P418NSO20

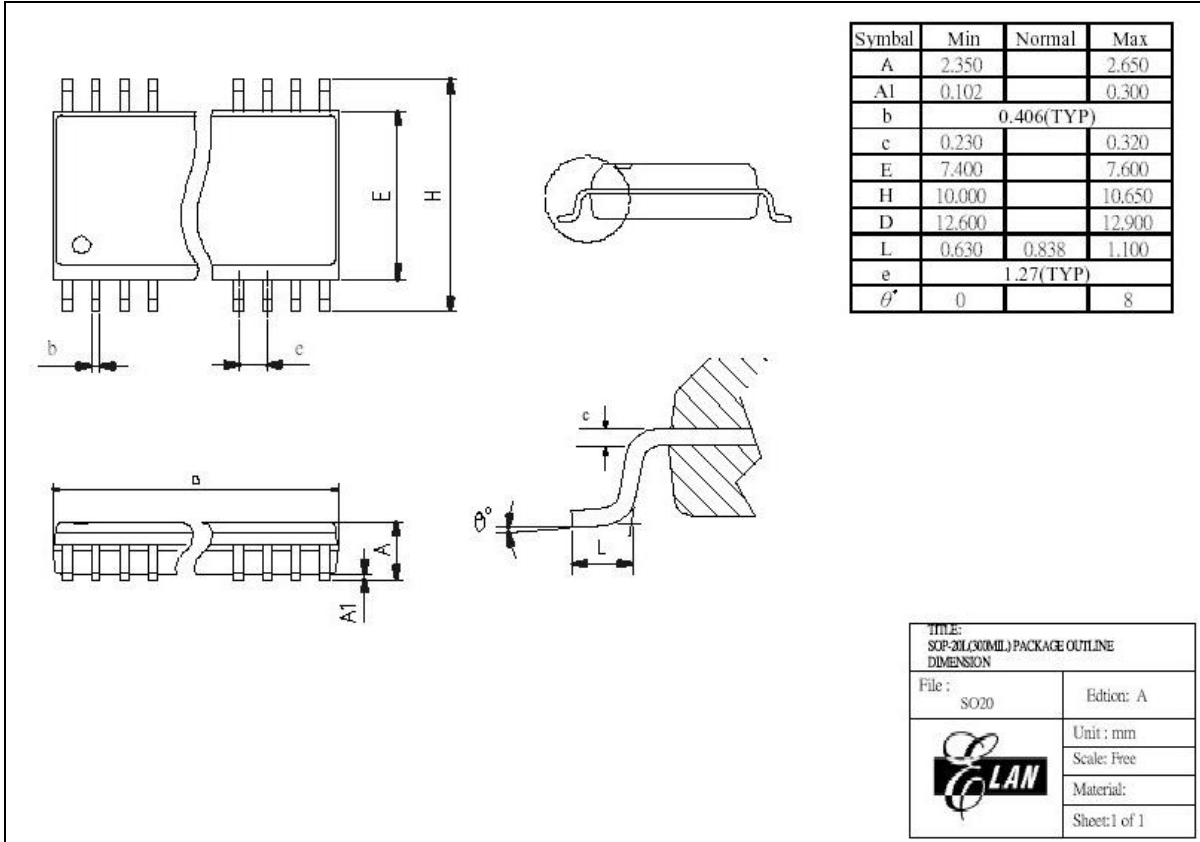


Figure C-4 EM78P418N 20-pin SOP Package Type

C.5 EM78P418NK24

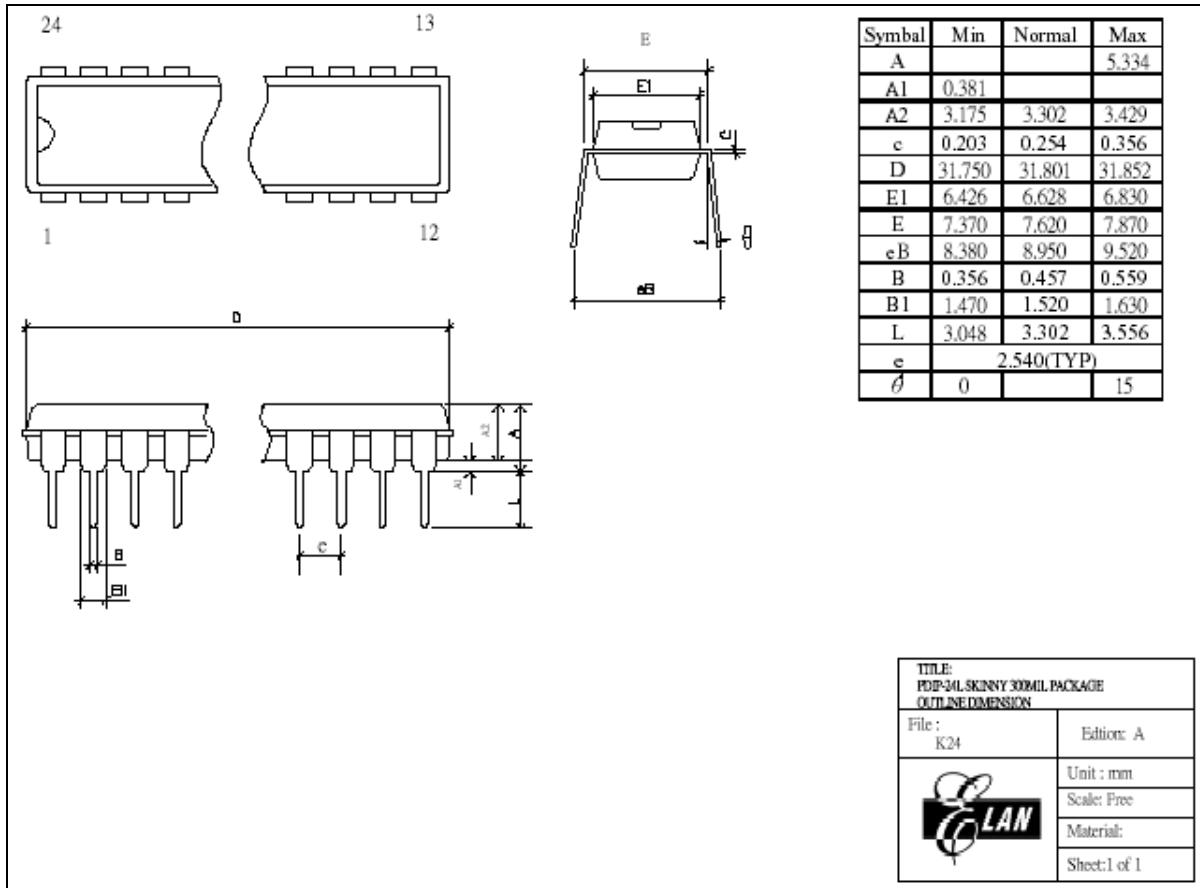


Figure C-5 EM78P418N 24-pin Skinny DIP Package Type

C.6 EM78P418NSO24

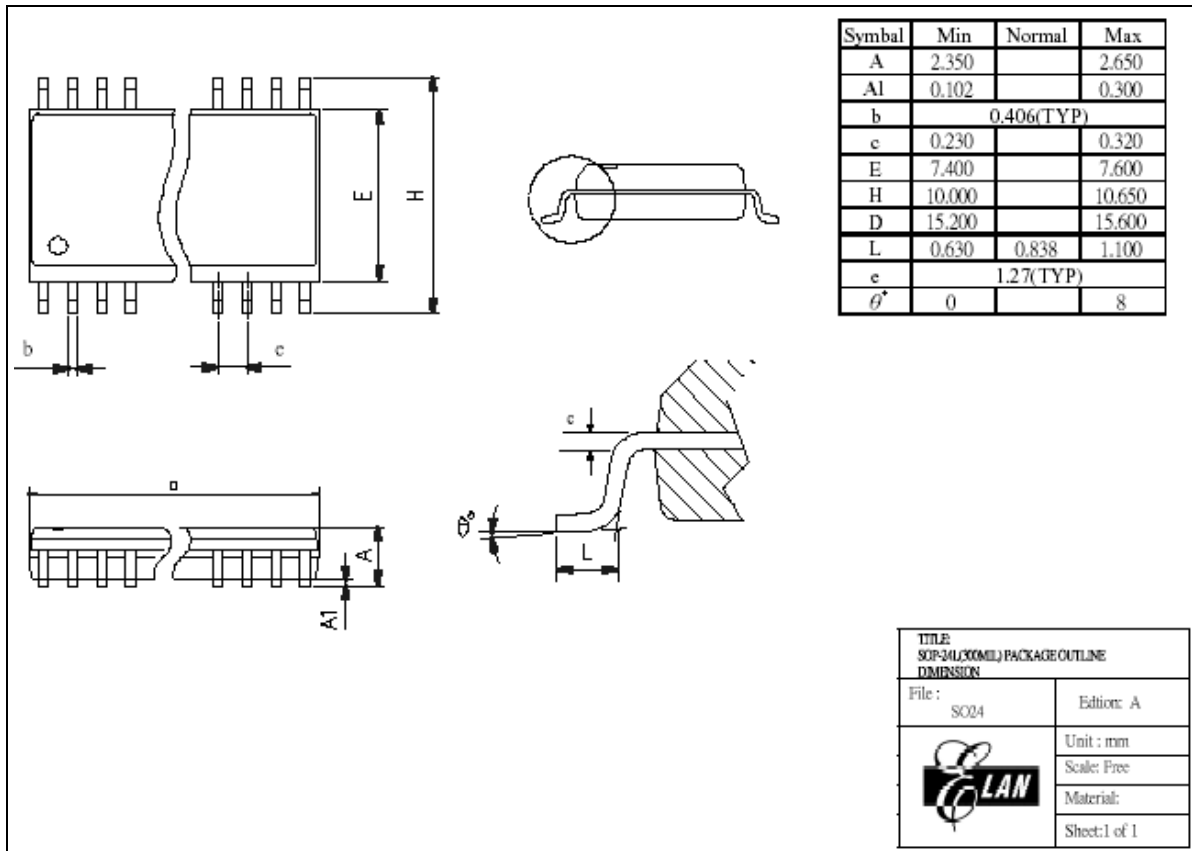


Figure C-6 EM78P418N 24-pin SOP Package Type

C.7 EM78P418NSS24

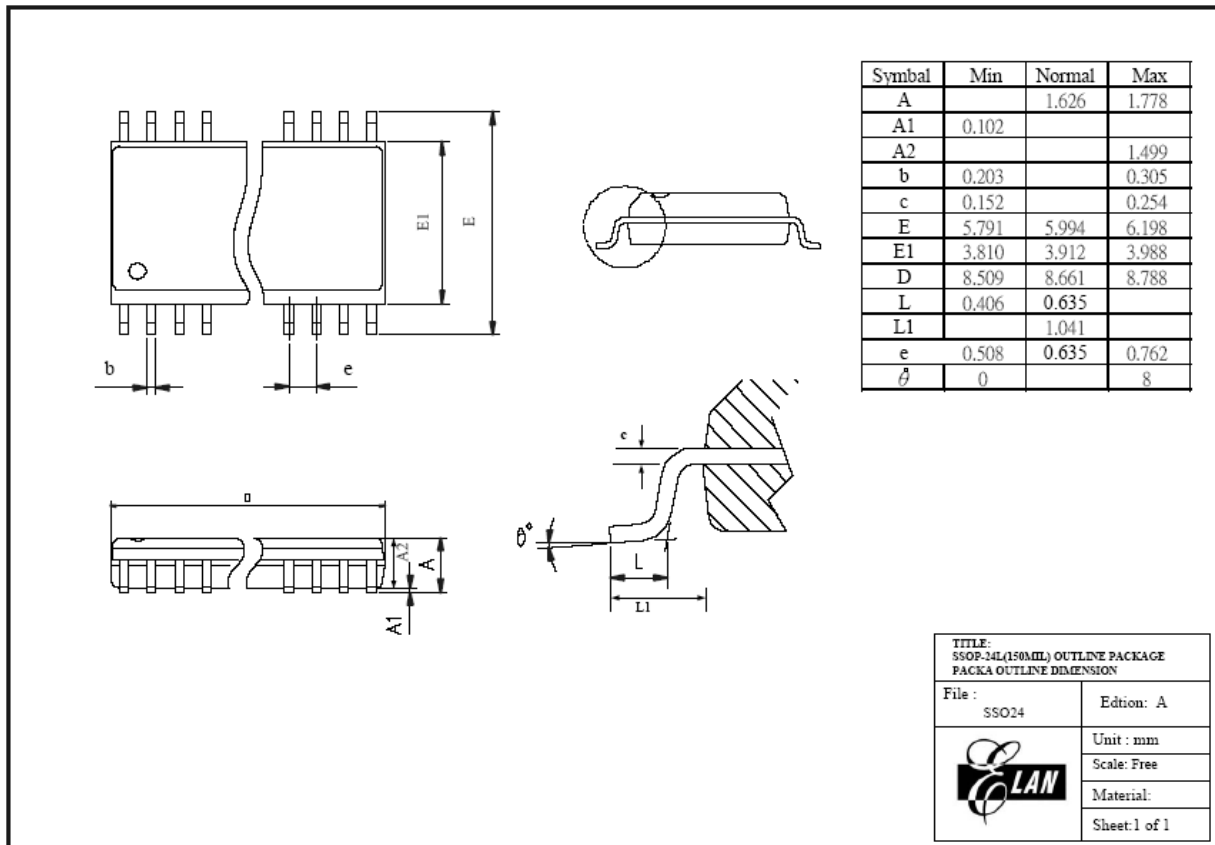


Figure C-7 EM78P418N 24-pin SSOP Package Type

D EM78P418N Program Pin

In the following IC diagram, “Pin # number” means the Pin to be connected to the Socket in DWTR.

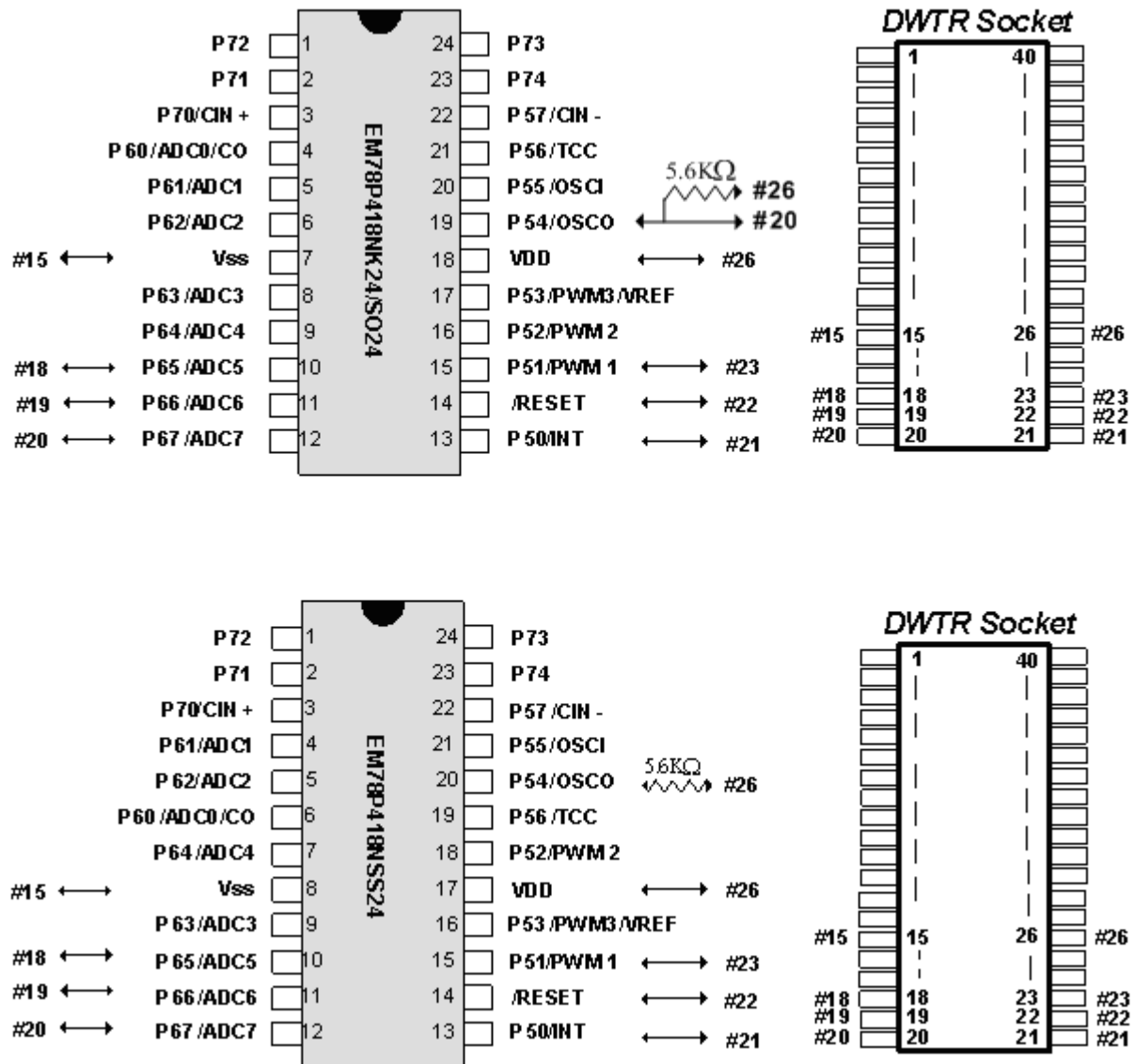


Figure D-1 Pin Assignment with corresponding pins assigned to the Socket in DWTR

E Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature= $245 \pm 5^{\circ}\text{C}$, for 5 seconds up to the stopper using a rosin-type flux	-
Pre-condition	Step 1: TCT, 65°C (15mins)~ 150°C (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C , TD (durance)=24 hrs	
	Step 3: Soak at 30°C /60% , TD (durance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness $\geq 2.5\text{mm}$ or Pkg volume $\geq 350 \text{ mm}^3$ ---- $225 \pm 5^{\circ}\text{C}$) (Pkg thickness $\leq 2.5 \text{ mm}$ or Pkg volume $\leq 350 \text{ mm}^3$ ---- $240 \pm 5^{\circ}\text{C}$)	
Temperature cycle test	-65° (15mins)~ 150°C (15mins), 200 cycles	-
Pressure cooker test	TA = 121°C , RH=100%, pressure=2 atm, TD (durance) = 96 hrs	-
High temperature / High humidity test	TA= 85°C , RH=85% , TD (durance)=168 , 500 hrs	-
High-temperature storage life	TA= 150°C , TD (durance)=500, 1000 hrs	-
High-temperature operating life	TA= 125°C , VCC=Max. operating voltage, TD (durance) =168, 500, 1000 hrs	-
Latch-up	TA= 25°C , VCC=Max. operating voltage, 150mA/20V	-
ESD (HBM)	TA= 25°C , $\geq \pm 3\text{KV} $	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD,
ESD (MM)	TA= 25°C , $\geq \pm 300\text{V} $	IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-)mode

E.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.

