EM78P458/459

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.7

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	–
1.1	Modified the ERC frequency	2003/03/06
1.2	Added AD and OP specs	2003/05/07
1.3	Changed the Power-on reset contents	2003/07/01
1.4	Added Device Characteristics in Section 6.5	2004/06/25
1.5	Updated the Package Types	2010/06/18
1.6	Modified the Pin description	2010/12/10
1.7	Deleted the 18-pin Package Type	2014/01/20

1 General Description

EM78P458 and EM78P459 are 8-bit microprocessors designed and developed with low-power and high-speed CMOS technology. It is equipped with a 4K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM).

With its OTP-ROM feature, it is able to offer a convenient way of developing and verifying user's programs. Moreover, user can take advantage of EMC Writer to easily program his development code.

2 Features

- CPU configuration
  - 4K×13 bits on-chip ROM
  - 84×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
- Low power consumption:
  - Less than 1.5 mA at 5V/4MHz
  - Typically 15 µA at 3V/32kHz
  - Typically 1 µA, during Sleep mode
- I/O port configuration
  - Two bidirectional I/O ports
  - Two clocks per instruction cycle
  - Seven programmable pull-high I/O pins
  - Eight Programmable pull-down I/O pins
  - Eight programmable open-drain I/O pins
- Operating voltage range: 2.3V~5.5V
- Operating temperature range: 0~70°C
- Operating frequency range (base on 2 clocks):
  - Crystal mode:

    DC~20MHz/2clks @ 5V

    DC~8MHz/2clks @ 3V
  - RC mode:

    DC~4 MHz/2clks @ 5V

    DC~4 MHz/2clks @ 3V
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 8-bit multi-channel Analog-to-Digital Converter with 8-bit resolution
  - Dual Pulse Width Modulation (PWM) with 10-bit resolution
  - One pair of comparators
  - Power down (Sleep) mode
- Six available interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - External interrupt
  - ADC completion interrupt
  - PWM period match completion
  - Comparator high interrupt
- Special features
  - Programmable free running watchdog timer
- Package type:
  - 20-pin DIP 300mil : EM78P458AP
  - 20-pin SOP 300mil : EM78P458AM
  - 24-pin skinny DIP 300mil : EM78P459AK

3 Pin Assignment

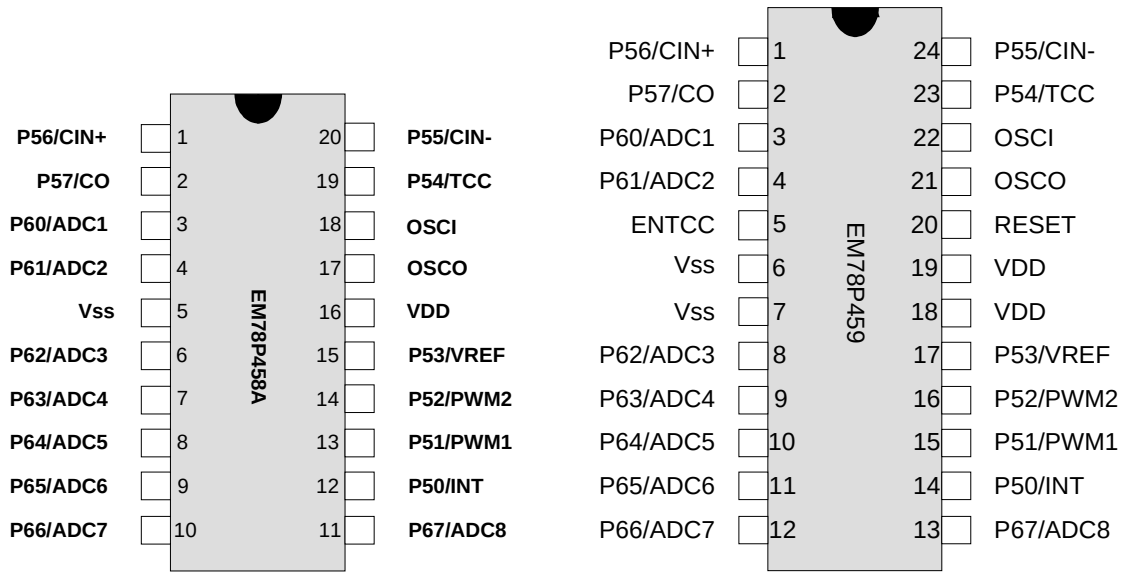


Figure 3-1 EM78P458A/459 Pin Assignment

4 Pin Description

Table 4-1 EM78P458/EM78P459 Pin Description

Name	Function	Input Type	Output Type	Description
P50/INT (VPP)	P50	ST	-	Input pin only
	INT	ST	-	External interrupt pin
	(VPP)	ST	-	VPP pin for Writer programming
P51/PWM1 (/OEB)	P51	ST	CMOS	Bidirectioinal I/O pin with programmable open-drain
	PWM1	-	CMOS	PWM1 output
	(/OEB)	ST	-	/OEB pin for Writer programming
P52/PWM2	P52	ST	CMOS	Bidirectioinal I/O pin with programmable open-drain
	PWM2	-	CMOS	PWM2 output
P53/VREF	P53	ST	CMOS	Bidirectioinal I/O pin with programmable pull-high
	VREF	AN	-	ADC external voltage reference
P54/TCC	P54	ST	CMOS	Bidirectioinal I/O pin with programmable open-drain
	TCC	ST	-	Real Time Clock/Counter clock input
P55/CIN-	P55	ST	CMOS	Bidirectioinal I/O pin with programmable pull-high
	CIN-	AN	-	Inverting end of comparator
P56/CIN+	P56	ST	CMOS	Bidirectioinal I/O pin with programmable pull-high
	CIN+	AN	-	Non-inverting end of comparator
P57/CO	P57	ST	CMOS	Bidirectioinal I/O pin with programmable open-drain
	CO	-	AN	Comparator Output
P60/ADC1	P60	ST	CMOS	Bidirectioinal I/O pin with programmable pull-down and pull-high
	ADC1	AN	-	ADC Input 1
P61/ADC2	P61	ST	CMOS	Bidirectioinal I/O pin with programmable pull-down and pull-high
	ADC2	AN	-	ADC Input 2
P62/ADC3	P62	ST	CMOS	Bidirectioinal I/O pin with programmable pull-down and pull-high
	ADC3	AN	-	ADC Input 3
P63/ADC4	P63	ST	CMOS	Bidirectioinal I/O pin with programmable pull-down and pull-high
	ADC4	AN	-	ADC Input 4

Name	Function	Input Type	Output Type	Description
P64/ADC5 (DATAIN)	P64	ST	CMOS	Bidirectioinal I/O pin with programmable pull-down and open-drain
	ADC5	AN	-	ADC Input 5
	(DATAIN)	ST	-	DATAIN pin for Writer programming
P65/ADC6 (DINCK)	P65	ST	CMOS	Bidirectioinal I/O pin with programmable pull-down and open-drain
	ADC6	AN	-	ADC Input 6
	(DINCK)	ST	-	DINCK pin for Writer programming
P66/ADC7 (ACLK)	P66	ST	CMOS	Bidirectioinal I/O pin with programmable pull-down and open-drain
	ADC7	AN	-	ADC Input 7
	(ACLK)	ST	-	ACLK pin for Writer programming
P67/ADC8 (/PGMB)	P67	ST	CMOS	Bidirectioinal I/O pin with programmable pull-down and open-drain
	ADC8	AN	-	ADC Input 8
	/PGMB	ST	-	/PGMB pin for Writer programming
OSCI	OSCI	XTAL	-	Clock input of crystal/ resonator oscillator
OSCO	OSCO	-	XTAL	Clock output of crystal/ resonator oscillator
ENTCC	ENTCC	ST	-	"**0**": Disable TCC "**1**": Enable TCC
RESET	RESET	ST	-	If it remains at logic low, the device will be in reset
VDD	VDD	POWER	-	Power
VSS	VSS	POWER	-	Ground

Legend: *ST: Schmitt Trigger input* *AN: analog pin*
XTAL: oscillation pin for crystal / resonator *CMOS: CMOS output*

5 Functional Description

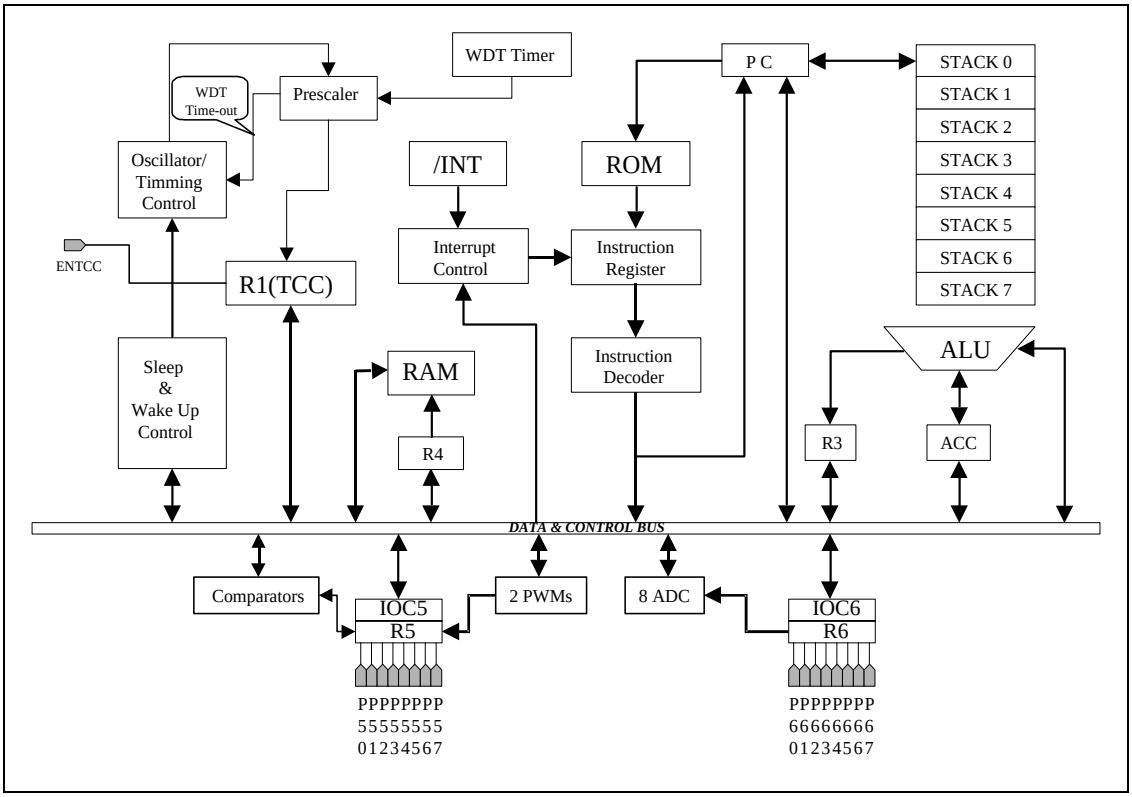


Figure 5-1 Functional Block Diagram of EM78P458/459

5.1 Operational Registers

5.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

5.1.2 R1 (Time Clock/Counter)

- Increased by an external signal edge through the TCC pin, or by the instruction cycle clock.
- The signals to increase the counter are determined by Bit 4 and Bit 5 of the CONT register.
- Writable and readable as any other registers.

5.1.3 R2 (Program Counter) and Stack

- R2 and hardware stacks are 12-bit wide. The structure is depicted in Figure 5-2.
- Generates 4K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are set to all "0"s during a Reset condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and tenth bits of the PC are cleared.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.
- Any instruction that is written to R2 (e.g. "ADD R2, A", "MOV R2, A", "BC R2, 6",·etc.) will cause the ninth bit and the tenth bit (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.
- In the case of EM78P458/459, the most two significant bits (A11 and A10) will be loaded with the content of PS1 and PS0 in the status register (R3) upon the execution of a "JMP", "CALL", or any other instructions set which write to R2.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instructions which write to R2, need one more instruction cycle.

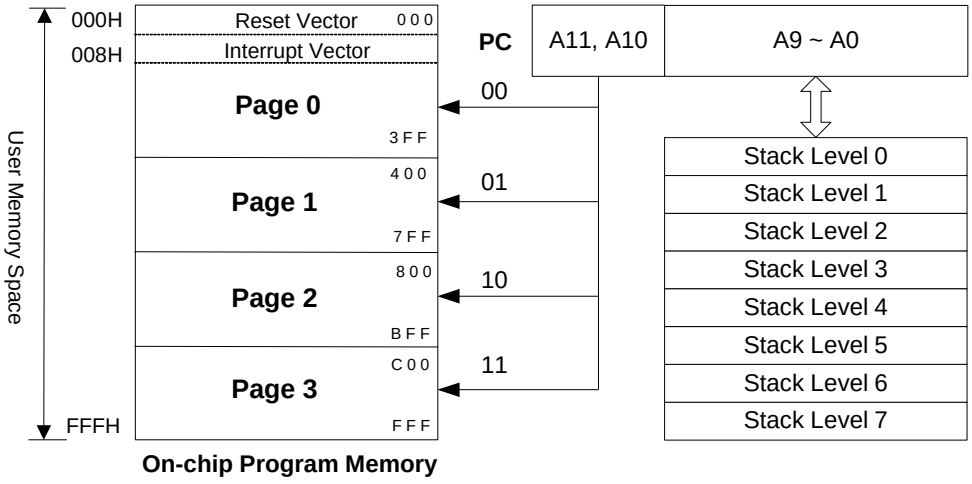


Figure 5-2 Program Counter Organization

Address	PAGE Registers	IOC PAGE Registers	IOC PAGE Registers
00	R0 (IAR)	Reserve	Reserve
01	R1 (TCC)	Reserve	Reserve
02	R2 (PC)	Reserve	Reserve
03	R3 (Status)	Reserve	Reserve
04	R4 RSR)	Reserve	Reserve
05	R5 (Port 5)	IOC50 (I/O Port Control Register)	IOC51 (PWMCON)
06	R6 (Port 6)	IOC60 (I/O Port Control Register)	IOC61 (DT1L)
07	R7 General Registers	Reserve	IOC71 (DT1H)
08	R8 General Registers	Reserve	IOC81 (PRD1)
09	R9 (ADCON)	IOC90 (GCON)	IOC91 (DT2L)
0A	RA (ADDATA)	IOCA0 (AD-CMPCON)	IOCA1 (DT2H)
0B	RB General Registers	IOCB0 (Pull-down Control Register)	IOCB1 (PRD2)
0C	RC General Registers (Only two bits)	IOCC0 (Open-drain Control Register)	IOCC1 (DL1L)
0D	RD General Registers	IOCD0 (Pull-high Control Register)	IOCD1 (DL1H)
0E	RE General Registers (Only two bits)	IOCE0 (WDT Control Register)	IOCE1 (DL2L)
0F	RF (Interrupt status)	IOCF0 (Interrupt Mask Register)	IOCF1 (DL2H)
10 : 1F	General Registers		
20 : 3F	Bank 0	Bank 1	

Figure 5-3 Data Memory Configuration

5.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPOUT	PS1	PS0	T	P	Z	DC	C

Bit 7 (CMPOUT): Result of the comparator output.

Bits 6 ~ 5 (PS1 ~ PS0): Page select bits. PS0~PS1 are used to select a program memory page. When executing a "JMP", "CALL", or other instructions which cause the program counter to be changed (e.g. MOV R2, A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will always be to the page from the place where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

PS1	PS0	Program Memory Page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

Bit 4 (T): Time-out bit. Set to "**1**" by the "SLEP" and "WDTC" commands or during Power on and reset to "**0**" by WDT time-out.

Bit 3 (P): Power-down bit. Set to "**1**" during power-on or by a "WDTC" command and reset to "**0**" by a "SLEP" command.

Bit 2 (Z): Zero flag. Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

5.1.5 R4 (RAM Select Register)

Bit 7: General-Purpose read/write bit.

Bit 6: Used to select Bank 0 or Bank 1.

Bits 0 ~ 5: Used to select registers (Address: 00~3F) in indirect address mode.

5.1.6 R5 ~ R6 (Port 5 ~ Port 6)

- R5 and R6 are I/O registers.

5.1.7 R7 ~ R8

- All of these are 8-bit General-Purpose Registers.

5.1.8 R9 (ADCON: Analog-to-Digital Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	IOCS	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7~ Bit 6 Unused, read as '0'.

Bit 5 (IOCS): Select the Segment of the I/O control register.

0: Segment 0 (IOC50~IOCF0) selected

1: Segment 1 (IOC51~IOCF1) selected

Bit 4 (ADRUN): ADC starts to RUN

0: Reset on completion of the conversion. This bit cannot be reset by software.

1: A/D conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to save power even while the CPU is operating.

1: ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select.

000 = AN0

001 = AN1

010 = AN2

011 = AN3

100 = AN4

101 = AN5

110 = AN6

111 = AN7

These can only be changed when the ADIF bit and the ADRUN bit are both LOW.

5.1.9 RA (ADDATA: Converted value of ADC)

When A/D conversion is completed, the result is loaded into the ADDATA. The START//END bit is cleared, and the ADIF is set.

5.1.10 RB (8-bit General-Purpose Register)

5.1.11 RC (2-bit Register, Bit 0 and Bit 1)

5.1.12 RD (8-bit General-Purpose Register)

5.1.13 RE (2-bit Register, Bit 0 and Bit 1)

5.1.14 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	CMPIF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF

Note: *"**1**" means with interrupt request, and "**0**" means no interrupt occurs.*

Bit 7: Unused, read as '0'

Bit 6 (CMPIF): High-compared interrupt flag. Set when a change occurs in the Comparator output, reset by software.

Bit 5 (PWM2IF): PWM2 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 4 (PWM1IF): PWM1 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 3 (ADIF): Interrupt flag for analog-to-digital conversion. Set when AD conversion is completed, reset by software.

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

- RF can be cleared by instruction but cannot be set.
- IOCF0 is the interrupt mask register.
- Note that to read RF will result to "logic AND" of RF and IOCF0.

5.1.15 R10 ~ R3F

- All of these are 8-bit General-Purpose Registers.

5.2 Special Purpose Registers

5.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. The accumulator is not an addressable register.

5.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 7 (INTE): INT signal edge

0: interrupt occurs at a rising edge on the INT pin

1: interrupt occurs at a falling edge on the INT pin

Bit 6 (INT): Interrupt Enable flag

0: masked by DISI or hardware interrupt

1: enabled by the ENI/RETI instructions

Bit 5 (TS): TCC signal source

0: internal instruction cycle clock. If P54 is used as I/O pin, TS must be "**0**".

1: transition on the TCC pin

Bit 4 (TE): TCC signal edge

0: increment if the transition from low to high takes place on the TCC pin

1: increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PAB): Prescaler assigned bit

0: TCC

1: WDT

Bit 2 ~ Bit 0 (PSR2 ~ PSR0): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

The CONT register is both readable and writable.

5.2.3 IOC50 ~ IOC60 (I/O Port Control Register)

- "**1**" puts the relative I/O pin into high impedance, while "**0**" defines the relative I/O pin as output.
- IOC50 and IOC60 registers are both readable and writable.

5.2.4 IOC90 (GCON: I/O Configuration and Control of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OP2E	OP1E	G22	G21	G20	G12	G11	G10

Bit 7 (OP2E): Enable the gain amplifier which input is connected to P64 and output is connected to the 8-1 analog switch.

0: OP2 is off (default value), and bypasses the input signal to the ADC

1: OP2 is on

Bit 6 (OP1E) Enable the gain amplifier whose input is connected to P60 and output is connected to the 8-1analog switch.

0: OP1 is off (default value), and bypasses the input signal to the ADC

1: OP1 is on

Bit 5 ~ Bit 3 (G22 ~ G20): Select the gain of OP2.

000 = IS x 1 (default value)

001 = IS x 2

010 = IS x 4

011 = IS x 8

100 = IS x 16

101 = IS x 32

Legend: IS = input signal

Bit 2 ~ Bit 0 (G12 ~ G10): Select the gain of OP1.

000 = IS x 1 (default value)

001 = IS x 2

010 = IS x 4

011 = IS x 8

100 = IS x 16

101 = IS x 32

Legend: IS = input signal

5.2.5 IOCA0 (AD-CMPCON)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CE	COE	IMS2	IMS1	IMS0	CKR1	CKR0

Bit 7(VREFS): Input source of the Vref of the ADC.

0: The Vref of the ADC is connected to Vdd (default value), and the P53/VREF pin carries out the function of P53.

1: The Vref of the ADC is connected to P53/VREF.

Bit 6 (CE): Comparator enable bit

0: Comparator is off (default value)

1: Comparator is on.

Bit 5 (COE): Set P57 as the output of the comparator

0: the comparator acts as an OP if CE=1

1: act as a comparator if CE=1

Bit 4 ~ Bit 2 (IMS2 ~ IMS0): Input Mode Select. ADC configuration definition bit.

The following Table shows the characteristics of each pin of R6.

Table 5-1 Description of AD Configuration Control Bits

IMS2:IMS0	P60	P61	P62	P63	P64	P65	P66	P67
000	A	D	D	D	D	D	D	D
001	A	A	D	D	D	D	D	D
010	A	A	A	D	D	D	D	D
011	A	A	A	A	D	D	D	D
100	A	A	A	A	A	D	D	D
101	A	A	A	A	A	A	D	D
110	A	A	A	A	A	A	A	D
111	A	A	A	A	A	A	A	A

Bit 1 ~ Bit 0 (CKR1 ~ CKR0): Prescaler of oscillator clock rate of ADC

00 = 1: 4 (default value)

01 = 1: 16

10 = 1: 64

11 = The oscillator clock source of ADC is from the WDT ring oscillator frequency.

(frequency=256/18ms 14.2kHz)

5.2.6 IOCB0 (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

Bit 7 (/PD7): Control bit used to enable pull-down of the P67 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD6): Control bit used to enable pull-down of the P66 pin.

Bit 5 (/PD5): Control bit used to enable pull-down of the P65 pin.

Bit 4 (/PD4): Control bit used to enable pull-down of the P64 pin.

Bit 3 (/PD3): Control bit used to enable pull-down of the P63 pin.

Bit 2 (/PD2): Control bit used to enable pull-down of the P62 pin.

Bit 1 (/PD1): Control bit used to enable pull-down of the P61 pin.

Bit 0 (/PD0): Control bit used to enable pull-down of the P60 pin.

The IOCB0 register is both readable and writable.

5.2.7 IOCC0 (Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0

Bit 7 (OD7): Control bit used to enable open-drain of the P57 pin.

0: Enable open-drain output

1: Disable open-drain output

Bit 6 (OD6): Control bit used to enable open-drain of the P54 pin.

Bit 5 (OD5): Control bit used to enable open-drain of the P52 pin.

Bit 4 (OD4): Control bit used to enable open-drain of the P51 pin.

Bit 3 (OD3): Control bit used to enable open-drain of the P67 pin.

Bit 2 (OD2): Control bit used to enable open-drain of the P66 pin.

Bit 1 (OD1): Control bit used to enable open-drain of the P65 pin.

Bit 0 (OD0): Control bit used to enable open-drain of the P64 pin.

The IOCC0 register is both readable and writable.

5.2.8 IOCD0 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	-	/PH3	/PH2	/PH1	/PH0

Bit 7 (/PH7): Control bit used to enable pull-high of the P56 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH6): Control bit used to enable pull-high of the P55 pin.

Bit 5 (/PH5): Control bit used to enable pull-high of the P53 pin.

Bit 4: Not used

Bit 3 (/PH3): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH2): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH1): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH0): Control bit used to enable pull-high of the P60 pin.

The IOCD0 register is both readable and writable.

5.2.9 IOCE0 (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	-	-	-	-

Bit 7 (WDTE): Control bit used to enable the Watchdog Timer.

0: Disable WDT

1: Enable WDT

The WDTE is both readable and writable

Bit 6 (EIS): Control bit used to define the function of the P50 (/INT) pin.

0: P50, input pin only

1: /INT, external interrupt pin. In this case, the I/O control bit of P50 (Bit 0 of IOC50) must be set to "**1**".

When EIS is "**0**", the path of the /INT is masked. When EIS is "1", the status of the /INT pin can also be read by way of reading Port 5 (R5). Refer to Figure 5-6.

EIS is both readable and writable.

Bits 5 ~ 0: Not used.

5.2.10 IOCF0 (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	CMPIE	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE

Bit 7: Unimplemented, read as '0'.

Individual interrupt is enabled by setting its associated control bit in the IOCF0 to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 5-10.

Bit 6 (CMPIE): CMPIF interrupt enable bit.

0: Disable CMPIF interrupt

1: Enable CMPIF interrupt

Bit 5 (PWM2IE): PWM2IF interrupt enable bit.

0: Disable PWM2 interrupt

1: Enable PWM2 interrupt

Bit 4 (PWM1IE): PWM1IF interrupt enable bit.

0: Disable PWM1 interrupt

1: Enable PWM1 interrupt

Bit 3 (ADIE): ADIF interrupt enable bit.

0: Disable ADIF interrupt

1: Enable ADIF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit.

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit.

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit.

0: Disable TCIF interrupt

1: Enable TCIF interrupt

The IOCF0 register is both readable and writable.

5.2.11 IOC51 (PWMCON)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

Bit 7 (PWM2E): PWM2 enable bit

0: PWM2 is off (default value), and its related pin carries out the P52 function.

1: PWM2 is on, and its related pin will be set to output automatically.

Bit 6 (PWM1E): PWM1 enable bit

0: PWM1 is off (default value), and its related pin carries out the P51 function.

1: PWM1 is on, and its related pin will be set to output automatically.

Bit 5 (T2EN): TMR2 enable bit

0: TMR2 is off (default value).

1: TMR2 is on.

Bit 4 (T1EN): TMR1 enable bit

0: TMR1 is off (default value).

1: TMR1 is on.

Bit 3 ~ Bit 2 (T2P1 ~ T2P0): TMR2 clock prescale option bits.

T2P1	T2P0	Prescale
0	0	1:2 (Default)
0	1	1:8
1	0	1:32
1	1	1:64

Bit 1 ~ Bit 0 (T1P1 ~ T1P0): TMR1 clock prescale option bits.

T1P1	T1P0	Prescale
0	0	1:2 (Default)
0	1	1:8
1	0	1:32
1	1	1:64

5.2.12 IOC61 (DT1L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM1 Duty Cycle)

A specified value keeps the output of PWM1 to remain at high until the value matches with TMR1.

5.2.13 IOC71 (DT1H: Most Significant Byte (Bit 1 ~ Bit 0) of PWM1 Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI1	SIGN1	VOF1[2]	VOF1[1]	VOF1[0]	-	PWM1[9]	PWM1[8]

Bit 7 (CALI1): Calibration enable bit

0: Disable calibration

1: Enable calibration

Bit 6 (SIGN1): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3: (VOF1[2]:VOF1[0]): Offset voltage bits

Bit 1 ~ Bit 0: (PWM1[9] ~ PWM1[8]): Most Significant Byte of PWM1 Duty Cycle

A specified value keeps the PWM1 output to remain at high until the value matches with TMR1.

5.2.14 IOC81 (PRD1: Period of PWM1)

The content of IOC81 is a period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

5.2.15 IOC91 (DT2L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM2 Duty Cycle)

A specified value keeps the of PWM1 output to remain at high until the value matches with TMR2.

5.2.16 IOCA1 (DT2H: Most Significant Byte (Bit 1 ~ Bit 0) of PWM2 Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI2	SIGN2	VOF2[2]	VOF2[1]	VOF2[0]	-	PWM2[9]	PWM2[8]

Bit 7 (CALI2): Calibration enable bit

0: Disable Calibration

1: Enable Calibration

Bit 6 (SIGN2): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3: (VOF2[2]:VOF2[0]): Offset voltage bits

Bit 1 ~ Bit 0: (PWM2[9] ~ PWM2[8]): Most Significant Bytes of PWM1 Duty Cycle

A specified value keeps the PWM2 output to remain at high until the value matches with TMR2.

5.2.17 IOCB1 (PRD2: Period of PWM2)

The content of IOCB1 is a period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

5.2.18 IOCC1 (DL1L: Least Significant Byte (Bit 7 ~ Bit 0) of the Duty Cycle Latch of PWM1)

The content of IOCC1 is read-only.

5.2.19 IOCD1 (DL1H: Most Significant Byte (Bit 1 ~ Bit 0) of the Duty Cycle Latch of PWM1)

The content of IOCD1 is read-only.

5.2.20 IOCE1 (DL2L: Least Significant Byte (Bit 7 ~ Bit 0) of the Duty Cycle Latch of PWM2)

The content of IOCE1 is read-only.

5.2.21 IOCF1 (DL2H: Most Significant Byte (Bit 1 ~ Bit 0) of the Duty Cycle Latch of PWM2)

The content of IOCF1 is read-only.

5.3 TCC/WDT and Prescaler

An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available either for the TCC or WDT only at any given time, and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescale ratio. The prescaler is cleared each time the instruction is written to TCC in TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the WDTC or SLEP instructions. Figure 5-4 depicts the circuit diagram of TCC/WDT.

- R1 (TCC) is an 8-bit timer/counter. The TCC clock source can be internal or external clock input (edge selectable from TCC pin). If TCC signal source is from an internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). Referring to Figure 5-4, selection of CLK=Fosc/2 or CLK=Fosc/4 depends on the Code Option bit CLKS. CLK=Fosc/2 if CLKS bit is "0", and CLK=Fosc/4 if CLKS bit is "1".
- If TCC signal source is from an external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin.
- The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to WDTE bit of IOCE0 register. Without prescaler, the WDT time-out period is approximately 18 ms[1].

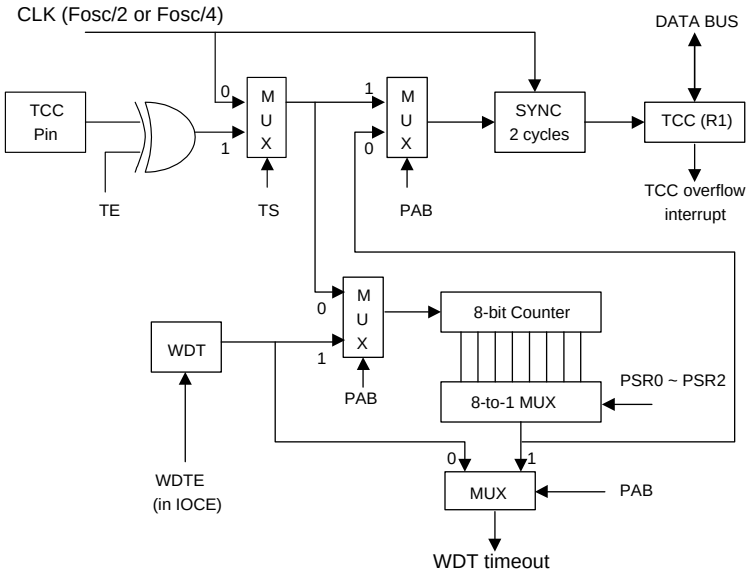


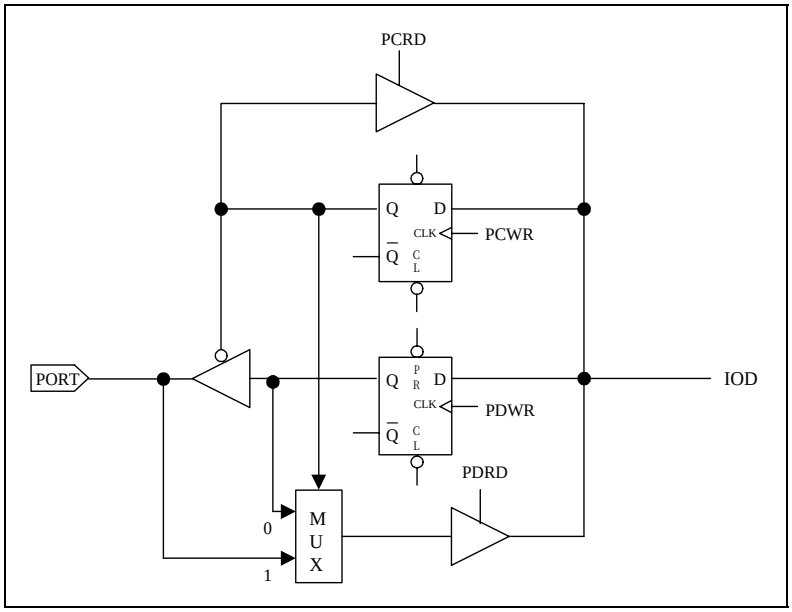
Figure 5-4 Block Diagram of TCC and WDT

[1] VDD=5V, Setup time period = 18 ms ± 30%

VDD=3V, Setup time period = 22 ms ± 30%

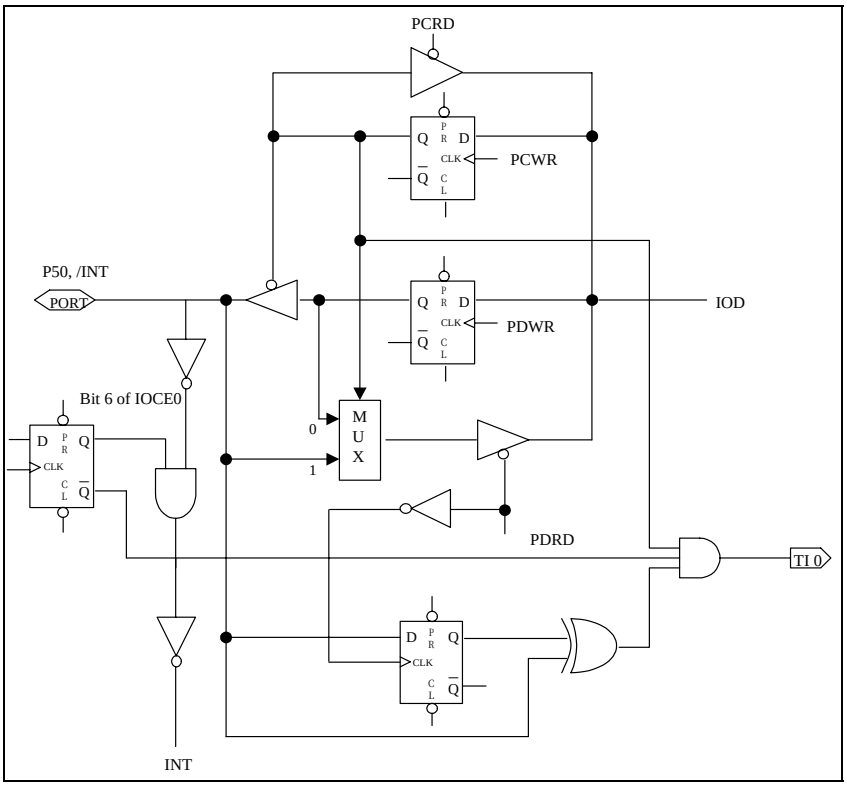
5.4 I/O Ports

Port 5, Port 6, and the I/O registers are bi-directional tri-state I/O ports. The function of Pull-high, Pull-down, and Open-drain can be set internally by IOCB0, IOCC0, and IOCD0, respectively. Port 6 features an input status changed interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC50 ~ IOC60). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in the following Figure 5-5, Figure 5-6, and Figure 5-7 respectively.



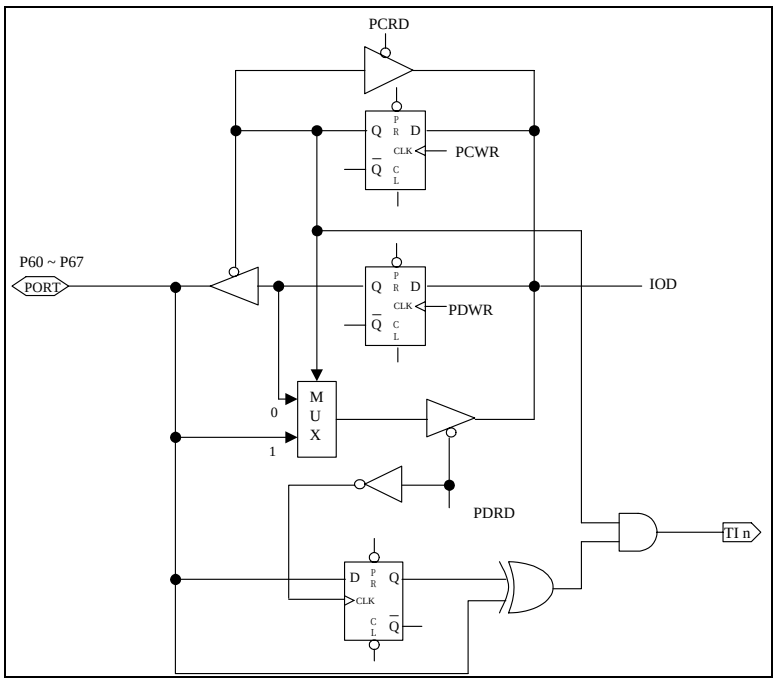
Note: *Pull-down is not shown in the figure.*

Figure 5-5 Circuit of I/O Port and I/O Control Register for Port 5



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 5-6 Circuit of I/O Port and I/O Control Register for P50 (/INT)



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 5-7 Circuit of I/O Port and I/O Control Register for P60~P67

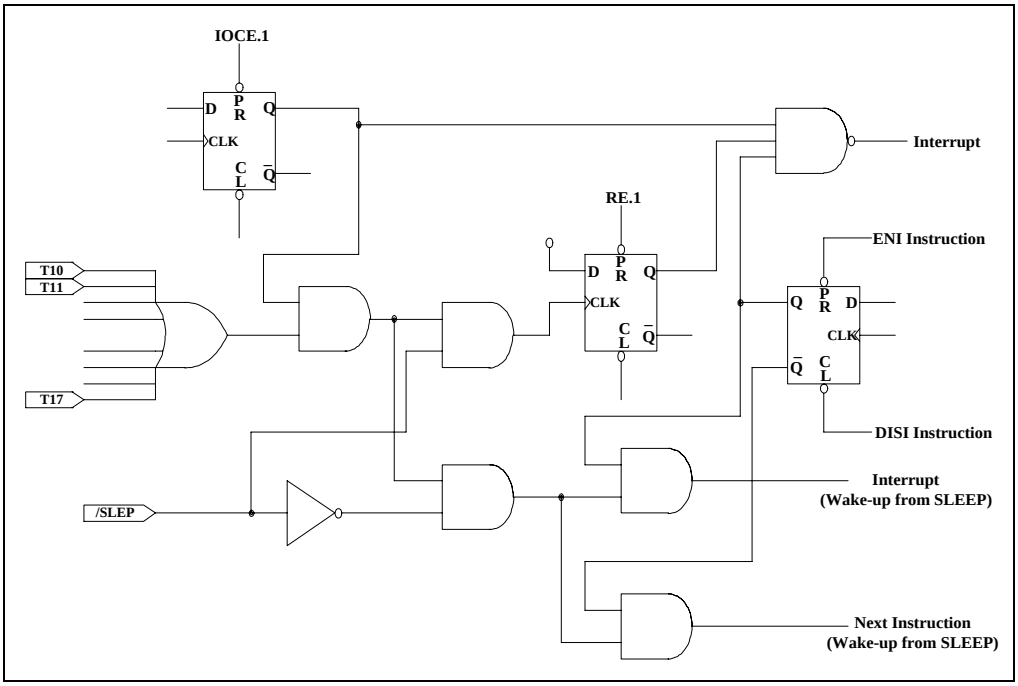


Figure 5-8 Block Diagram of Port 6 with Input Changed Interrupt/Wake-up

Table 5-2 Usage of Port 6 Input Changed Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change	(II) Port 6 Input Status Change Interrupt
(a) Before SLEEP	1. Read I/O Port 6 (MOV R6,R6)
1. Disable WDT	2. Execute "ENI"
2. Read I/O Port 6 (MOV R6,R6)	3. Enable interrupt (Set IOCF0.1)
3. Execute "ENI" or "DISI"	4. IF Port 6 changed (Interrupt)
4. Enable interrupt (Set IOCF0.1)	→ Interrupt Vector (008H)
5. Execute "SLEP" instruction	
(b) After wake-up	
1. IF "ENI" → Interrupt Vector (008H)	
2. IF "DISI" → Next instruction	

5.5 Reset and Wake-up

5.5.1 Reset and Wake-up Function

A reset is initiated by one of the following events:

(1) Power-on reset

(2) /RESET pin input "low"

(3) WDT Time-out (if enabled)

The device is kept in a Reset condition for a period of approximately 18 ms (one oscillator start-up timer period) after a reset is detected. Once a Reset occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "**0**".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "**1**" except for the Bit 6 (INT flag).
- The bits of the IOCB0 register are set to all "**1**".
- The IOCC0 register is cleared.
- The bits of the IOCD0 register are set to all "**1**".
- Bit 7 of the IOCE0 register is set to "**1**", and Bit 6 is cleared.
- Bits 0~6 of RF register and Bits 0~6 of IOCF0 register are cleared.

Executing the “SLEP” instruction will assert the sleep (power down) mode. While entering sleep mode, the WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by**:**

(1) External reset input on /RESET pin

(2) WDT time-out (if enabled)

(3) Port 6 Input Status Changed (if enabled)

(4) Comparator high

(5) ADC complete

The first two cases will cause the EM78P458/459 to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3 is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x8 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up.

Only one of Cases 2 to 4 can be enabled before entering into sleep mode. That is,

[a] If Port 6 Input Status Change Interrupt is enabled before SLEP , WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78P458/459 can be awakened only by Case 1 or Case 3.

[b] If WDT is enabled before SLEP, Port 6 Input Status Changed Interrupt must be disabled. Hence, the EM78P458/459 can be awakened only by Case 1 or Case 2. Refer to the section on Interrupt for further details.

[c] If Comparator High Interrupt is enabled before SLEP, WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78P458/459 can be awakened only by Case 1 or Case 4.

If Port 6 Input Status Change Interrupt is used to wake up the EM78P458/459 (as in Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @0Bxx000110   ; Select internal TCC clock
CONTW
CLR R1               ; Clear TCC and prescaler
MOV A, @0Bxxxx1110   ; Select WDT prescaler
CONTW
WDTC                 ; Clear WDT and prescaler
MOV A, @0B0xxxxxxx   ; Disable WDT
IOW RE
MOV R6, R6           ; Read Port 6
MOV A, @0B00000x1x   ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)        ; Enable (or disable) global interrupt
SLEP                 ; Sleep
NOP
```

Similarly, if the Comparator High Interrupt is used to wake up the EM78P458/459 (as in Case [c] above), the following instructions must be executed before SLEP:

```
MOV A, @0Bxx000110   ; Select internal TCC clock
CONTW
CLR R1               ; Clear TCC and prescaler
MOV A, @0Bxxxx1110   ; Select WDT prescaler
CONTW
WDTC                 ; Clear WDT and prescaler
MOV A, @0B0xxxxxxx   ; Disable WDT
IOW RE
MOV A, @0B01xxxxxx   ; Enable comparator high interrupt
IOW RF
ENI (or DISI)        ; Enable (or disable) global interrupt
SLEP                 ; Sleep
NOP
```

One problem user must be aware of, is that after waking up from sleep mode, the WDT function will be enabled automatically. The WDT operation (being enabled or disabled) should be handled appropriately by software after waking up from sleep mode.

5.5.2 The Status of T, and P of the Status Register

A Reset condition is initiated by one of the following events:

(1) Power-on condition

(2) High-low-high pulse on the /RESET pin, or

(3) Watchdog Timer time-out

The values of T and P, as listed in Table 5-3, are used to check how the processor wakes up. Table 5-4 shows the events, which may affect the status of T and P.

Table 5-3 Values of RST, T, and P after RESET

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

*P: Previous status before reset

Table 5-4 Status of RST, T and P being affected by Events

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

*P: Previous value before reset

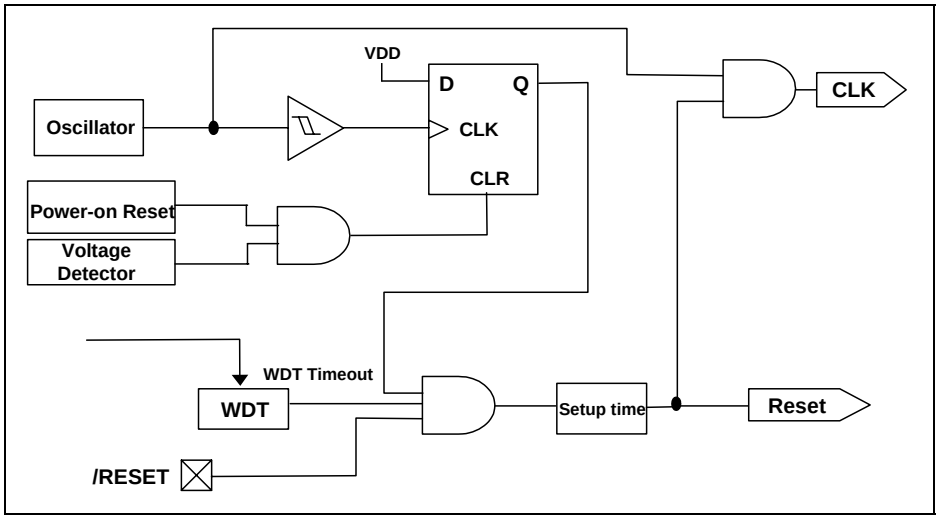


Figure 5-9 Block Diagram of Reset Controller

5.6 Interrupt

The EM78P458/459 has six interrupts as listed below:

(1) TCC overflow interrupt

(2) Port 6 Input Status Change Interrupt

(3) External interrupt [(P50, /INT) pin].

(4) Analog to Digital conversion completed.

(5) When TMR1/TMR2 matches with PRD1/PRD2 respectively in PWM.

(6) When the comparator outputs change.

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g. "MOV R6, R6") is necessary. Each Port 6 pin will have this feature if its status changes. Any pin configured as output or P50 pin configured as /INT is excluded from this function. Port 6 Input Status Change Interrupt will wake up the EM78P458/459 from the sleep mode if it is enabled prior to going into sleep mode by executing SLEP. When the controller wakes-up, it will continue to execute the succeeding program if the global interrupt is disabled, or branches out to the Interrupt Vector 008H if global interrupt is enabled.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from Address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF0 (refer to Figure 5-10). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (when enabled), the next instruction will be fetched from Address 001H.

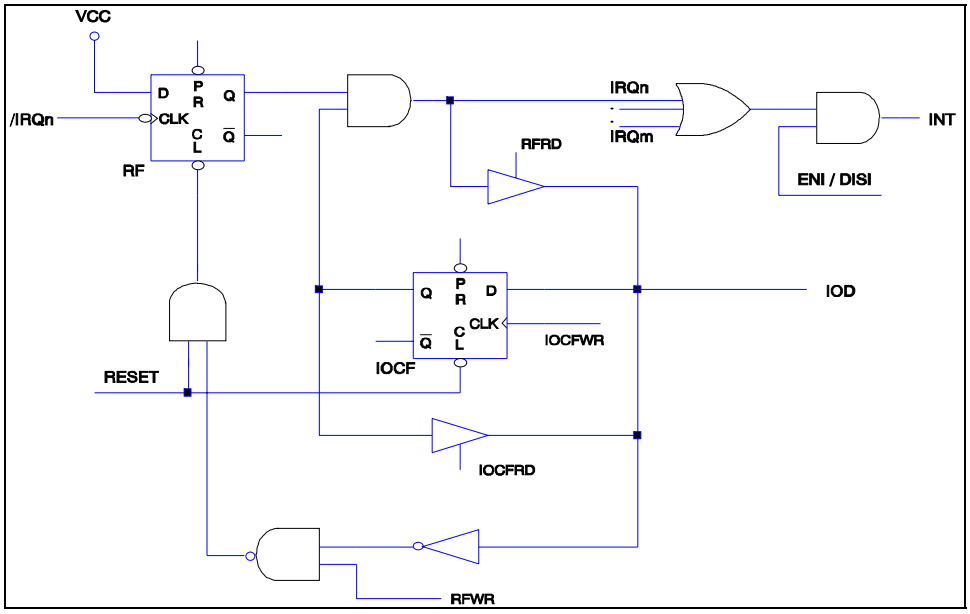


Figure 5-10 Interrupt Input Circuit

5.7 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 8-bit analog multiplexer, three control registers (ADCON/R9, AD-CMP-CON/IOCA0, GCON/IOC90), one data register (ADDATA/RA) and an ADC with 8-bit resolution. The functional block diagram of the ADC is shown in Figure 5-11. The analog reference voltage (Vref) and analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATA. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS0, ADIS1, and ADIS2.

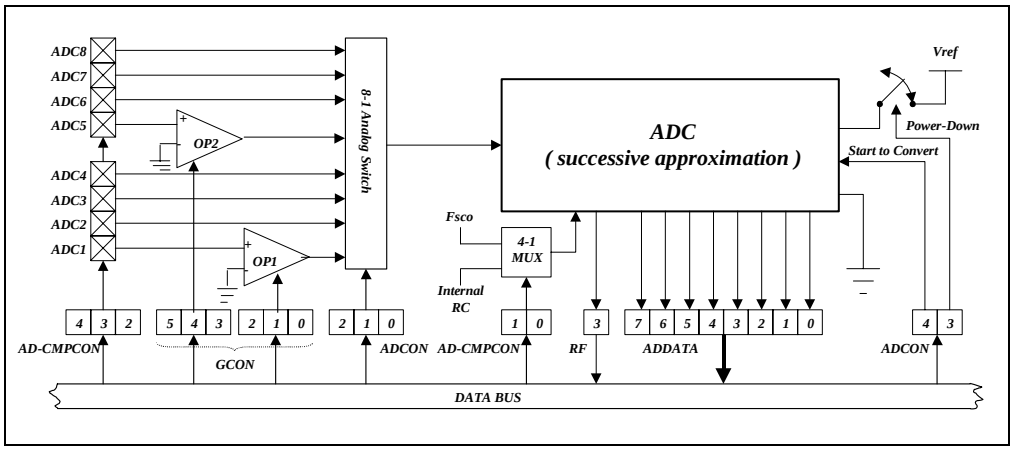


Figure 5-11 Functional Block Diagram of Analog-to-Digital Conversion

5.7.1 ADC Control Register (ADCON/R9, AD-CMP-CON/IOCA0, GCON/IOC90)

5.7.1.1 ADCON/R9

The ADCON register controls the operation of the A/D conversion and determines which pin should be currently active.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	-	-	IOCS	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
*Init_Value	0	0	0	0	0	0	0	0

**Init_Value: Initial value at power on reset*

- **ADRUN (Bit 4):** ADC starts to RUN.

  0: Reset on completion of the conversion. This bit cannot be reset by software.

  1: A/D conversion is started. This bit can be set by software.

- **ADPD (Bit 3):** ADC Power-down Mode.

  0: Switch off the resistor reference to save power even when the CPU is operating.

  1: ADC is operating

- **ADIS2 ~ ADIS0 (Bits 2 ~ 0):** Analog Input Select

  000 = AN0

  001 = AN1

  010 = AN2

  011 = AN3

  100 = AN4

  101 = AN5

  110 = AN6

  111 = AN7

Change occurs only when the ADIF bit and the ADRUN bit are both LOW.

5.7.1.2 AD-CMP-CON/IOCA0

The AD-CMP-CON register individually defines the pins of Port 6 as analog input or as digital I/O.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	VREFS	CE	COE	IMS2	IMS1	IMS0	CKR1	CKR0
*Init_Value	0	0	0	0	0	0	0	0

**Init_Value: Initial value at power-on reset*

- **VREFS (Bit 7):** The input source of the Vref of the ADC.

  0: The Vref of the ADC is connected to Vdd (default value), and the P53/VREF pin carries out the function of P53.

  1: The Vref of the ADC is connected to P53/VREF.

- **CE (Bit 6):** Control bit used to enable the comparator.

  0: Disable the comparator

  1: Enable the comparator

- **COE (Bit 5):** Set P57 as the output of the comparator

  0: the comparator functions as an OP if CE=1

  1: functions as a comparator if CE=1

- **IMS2 ~ IMS0 (Bit 4 ~ Bit 2):** ADC configuration definition bit.

- **CKR1 and CKR0 (Bit 1 and Bit 0):** Conversion time select.

  00 = Fosc/4

  01 = Fosc/16

  10 = Fsco/64

  11 = The oscillator clock source of ADC is from the WDT ring oscillator frequency.

  (frequency=256/18ms 14.2kHz)

5.7.1.3 GCON/IOC90

As shown in Figure 5-11, OP1 and OP2, the gain amplifiers, are located in the middle of the analog input pins (ADC1 and ADC5) and the 8-1 analog switch. The GCON register controls the gains.

Table 5-5 Table 7 Shows the Gains and the Operating Range of ADC

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	OP2E	OP1E	G22	G21	G20	G12	G11	G10
*Init_Value	0	0	0	0	0	0	0	0

**Init_Value: Initial value at power-on reset*

Table 5-6 Gains and the Operating Range of ADC

G10:G12/G20:G22	Gain	Operating Voltage Range
000	1	0 ~ Vref
001	2	0 ~ (1/2)Vref
010	4	0 ~ (1/4)Vref
011	8	0 ~ (1/8)Vref
100	16	0 ~ (1/16)Vref
101	32	0 ~ (1/32)Vref

NOTE

Vref cannot be less than 3 volts.

5.7.2 ADC Data Register (ADDATA/RA)

When A/D conversion is completed, the result is loaded to the ADDATA. The START/END bit is cleared, and the ADIF is set.

5.7.3 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 1 µs for each KΩ of the analog source impedance and at least 1 µs for the low-impedance source. After the analog input channel is selected, this acquisition time must be done before conversion can be started.

5.7.4 A/D Conversion Time

CKR0 and CKR1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the accuracy of A/D conversion. For the EM78P458/459, the conversion time per bit is 4 µs. Table 5-6 shows the relation between Tct and the maximum operating frequencies.

Table 5-7 Tct vs. the Maximum Operation Frequency

CKR0:CKR1	Operation Mode	Max. Operating Frequency
00	Fsco/4	1 MHz
01	Fsco/16	4 MHz
10	Fsco/64	16 MHz
11	Internal RC	-

5.7.5 A/D Operation during Sleep Mode

In order to reduce power consumption, A/D conversion remains operational during sleep mode, and is intended to implement the internal RC clock source mode. As the SLEP instruction is executed, all the operations of the MCU will stop except for the A/D conversion. The RUN bit will be cleared and the result will be fed to the ADDATA when conversion is completed. If the ADIE is enabled, the device will wake up. Otherwise, A/D conversion will be shut off, no matter what the status of ADPD bit is.

5.7.6 Programming Steps/Considerations

5.7.6.1 Programming Steps

Follow these steps to obtain data from the ADC:

(1) Write to the three bits (IMS2 ~ IMS0) on the AD-CMP-CON1 register to define the characteristics of R6: Digital I/O, analog channels, and voltage reference pin.

(2) Write to the ADCON register to configure the AD module:

(a) Select the A/D input channel (ADAS2 ~ ADAS0)

(b) Select the proper gains by writing to the GCON register (optional)

(c) Define the A/D conversion clock rate (CKR1:CKR0)

(d) Set the ADPD bit to "**1**" to begin sampling.

(3) Put "ENI" instruction, if interrupt function is employed.

(4) Set the ADRUN bit to "**1**".

(5) Wait for either the interrupt flag to be set or the ADC interrupt to occur.

(6) Read ADDATA, the conversion data register.

(7) Clear the interrupt flag bit (ADIF).

(8) For the next conversion, go to Step 1 or Step 2 as required. At least 2 Tct is required before the next acquisition starts.

NOTE

To obtain an accurate value, it is necessary to avoid any data transition on the I/O pins during AD conversion.

5.7.6.2 Demonstration Programs

```
; To define the general registers
R_0 == 0                ; Indirect addressing register
PSW == 3                ; Status register
PORT5 == 5
PORT6 == 6
R_F== 0XF               ; Interrupt status register

; To define the control register
IOC50 == 0X5            ; Control Register of Port 5
IOC60 == 0X6            ; Control Register of Port 6
C_INT== 0XF             ; Interrupt Control Register

;ADC Control Registers
ADDATA == 0xA           ; The contents are the results of ADC

ADCON R== 0x9           ; 7  6   5     4      3     2      1     0
                        ; -  -  IOCS  ADRUN  ADPD  ADIS2  ADIS1 ADIS0
ADCONC== 0xA            ;  7    6  5    4     3     2      1     0
                        ; VREFS  X  X  IMS2  IMS1  IMS0   CKR1  CKR0
GCON == 0x9             ;  7     6     5    4    3    2    1    0
                        ; OPE2  OPE1  G22  G21  G20  G12  G11  G10
;To define bits
;In ADCONR
ADRUN == 0x4            ; ADC is executed as the bit is set
ADPD == 0x3             ; Power Mode of ADC

ORG 0                   ; Initial address
JMP INITIAL             ;

ORG 0x08                ; Interrupt vector
```

```
(User program)

CLR R_F                  ; To clear the ADCIF bit
BS ADCONR, ADRUN         ; To start to execute the next AD
                         ; conversion if necessary
RETI
INITIAL:
MOV A, @0BXXXX1XXX       ; Enable the interrupt function of ADC,
“X” by application
IOW C_INT
MOV A, @0xXX             ; Interrupt disabled:<6>
CONTW
MOV A, @0B00000000       ; To employ Vdd as the reference voltage,
                         ; to define P60 as IOW ADCONC analog
                         ; input and set the clock rate at fosc/4
En_ADC:
MOV A, @0BXXXXXXX1       ; To define P60 as an input pin, and the
                         ; others are dependent IOW PORT6 on
                         ; applications
MOV A, @0B01000101       ; To enable the OP1, and set the gain as
                         ; 32
 IOW GCON
BS ADCONR, ADPD          ; To disable the power-down mode of ADC
ENI                      ; Enable the interrupt function
BS ADCONR, ADRUN         ; Start to run the ADC
; If the interrupt function is employed, the following three lines
may be ignored
POLLING:
JBC ADCONR, ADRUN        ; To check the ADRUN bit continuously;
JMP POLLING              ; ADRUN bit will be reset as the AD
                         ; conversion is completed
(User program)
:
:
:
```

5.8 Dual Sets of PWM (Pulse Width Modulation)

5.8.1 Overview

In PWM mode, both PWM1 and PWM2 pins produce up to 10-bit resolution PWM output (see Figure 5-12 for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output pin high. The baud rate of the PWM is the inverse of the period. Figure 5-13 depicts the relation between a period and a duty cycle.

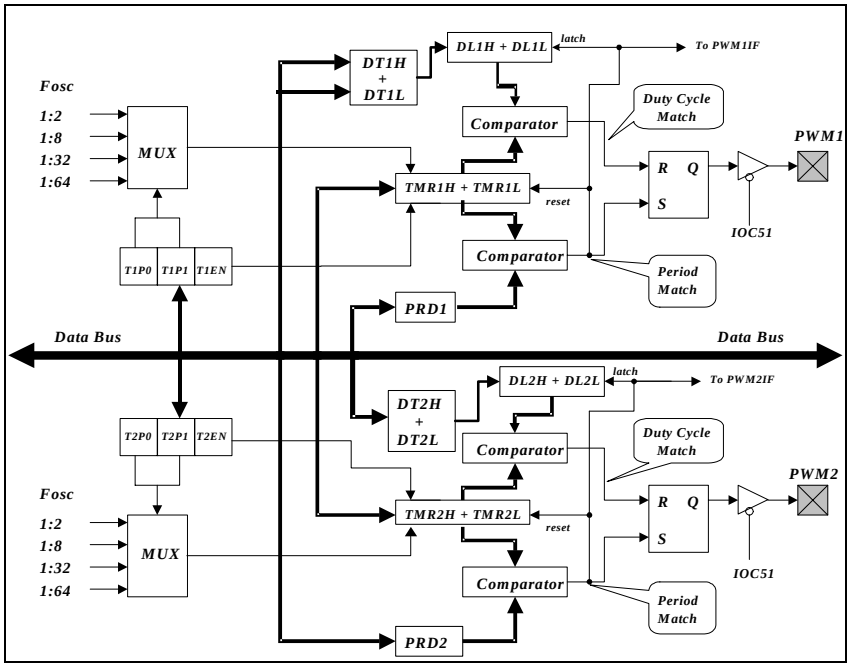


Figure 5-12 Dual PWMs Functional Block Diagram

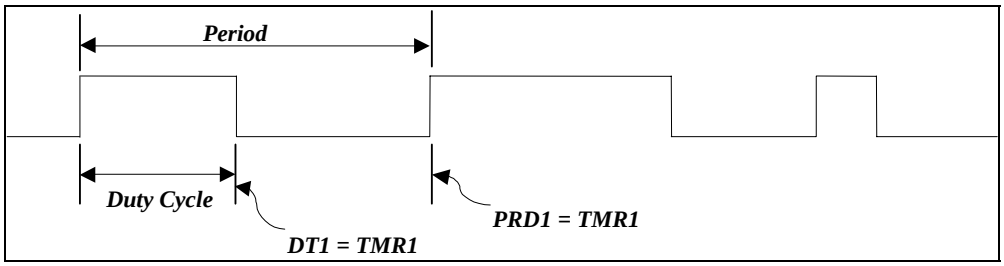


Figure 5-13 PWM Output Timing Diagram

5.8.2 Increment Timer Counter (TMRX: TMR1H/TWR1L or TMR2H/TWR2L)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written to, and cleared at any reset conditions. If employed, they can be turned down for power saving purposes by setting T1EN bit [PWMCON<4>] or T2EN bit [PWMCON<5>] to 0.

5.8.3 PWM Period (PRDX: PRD1 or PRD2)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared.
- The PWMX pin is set to "**1**".
- The PWM duty cycle is latched from DT1/DT2 to DTL1/DTL2.

NOTE

The PWM output will not be set if the duty cycle is 0.

- The PWMXIF pin is set to "**1**".

The following formula describes how to calculate the PWM period:

$$Period = (PRDX + 1) \times 4 \times \left(\frac{1}{Fosc}\right) \times (TMRX \ \text{Prescale value})$$

5.8.4 PWM Duty Cycle (DTX: DT1H/DT1L and DT2H/ DT2L; DTL: DL1H/DL1L and DL2H/DL2L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DTL until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

$$Duty\ Cycle = (DTX) \times \left(\frac{1}{Fosc}\right) \times (TMRX \ \text{Prescale value})$$

5.8.5 Comparator X

To change the output status while the match occurs, the TMRXIF flag will be set at the same time.

5.8.6 PWM Programming Procedure/Steps

(1) Load PRDX with the PWM period.

(2) Load DTX with the PWM Duty Cycle.

(3) Enable interrupt function by writing IOCF0, if required.

(4) Set PWMX pin to be output by writing a desired value to IOC51.

(5) Load a desired value to IOC51 with TMRX precsaler value and enable both PWMX and TMRX.

5.9 Timer

5.9.1 Overview

Timer 1 (TMR1) and Timer 2 (TMR2) (TMRX) are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written to, and cleared at any reset conditions.

5.9.2 Functional Description

Figure 5-14 shows the TMRX block diagram. Each signal and blocks are described as follows:

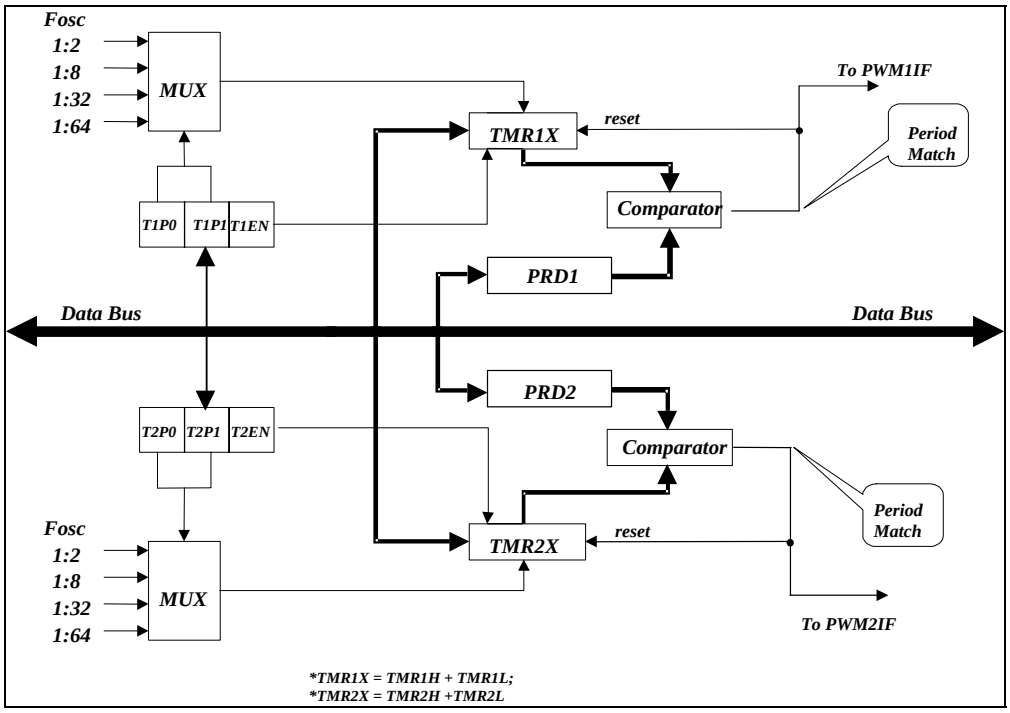


Figure 5-14 TMRX Block Diagram

Fosc: Input clock

Prescaler (T1P0 and T1P1/T2P1 and T2P0): Options of 1:2, 1:8, 1:32, and 1:64 are defined by TMRX. It is cleared when any type of reset occurs.

TMR1X and TMR2X (TMR1H/TWR1L and TMR2H/TMR2L): Timer X registers; TMRX is increased until it matches with PRDX, and then it is reset to "**0**". TMRX cannot be read.

PRDX (PRD1 and PRD2): PWM period register

Comparator X (Comparator 1 and Comparator 2): To reset TMRX while a match occurs and the TMRXIF flag is set at the same time.

5.9.3 Programming the Related Registers

When defining TMRX, refer to the operation of its related registers as shown in Table 9. It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, Bit 7 and Bit 6 of the PWMCON register must be set to '**0**'.

Table 5-8 Related Control Registers of TMR1 and TMR2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC51	PWMCON/IOC51	PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

5.9.4 Timer Programming Procedure/Steps

(1) Load PRDX with the Timer period.

(2) Enable the interrupt function by writing IOCF0, if required

(3) Load a desired value to PWMCON with the TMRX prescaler value and enable both TMRX and disable PWMX.

5.10 Comparator

EM78P458/459 has one comparator, which has two analog inputs and one output. The comparator can be employed to wake up from the sleep mode. Figure 5-15 shows the comparator circuit.

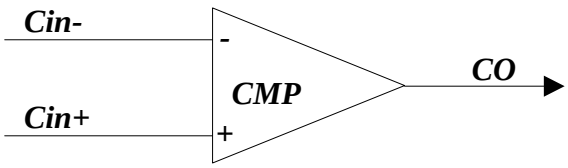


Figure 5-15 Comparator Operating Mode

5.10.1 External Reference Signal

The analog signal that is presented at Cin- is compared to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly.

- The reference signal must be between Vss and Vdd.
- The reference voltage can be applied to either pi of the comparator.
- Threshold detector applications may be of the same reference.
- The comparator can operate from the same or different reference source.

5.10.2 Comparator Outputs

- The compared result is stored in the CMPOUT of R3.
- The comparator outputs are output to P57 by programming Bit 5 <COE> of the AD-CMPCON register to 1.
- P57 must be defined as output if implemented as the comparator output.
- Figure 5-16 shows the comparator output block diagram.

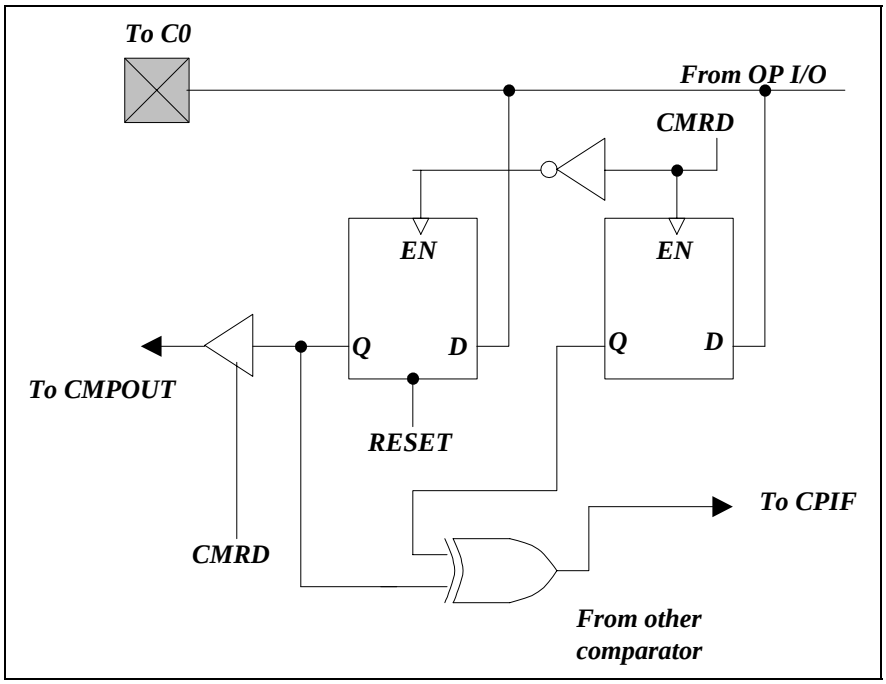


Figure 5-16 Output Configuration of a Comparator

5.10.3 Used as an Operation Amplifier

The comparator can be used as an operation amplifier if a feedback resistor is externally connected from the input to the output. In this case, the Schmitt trigger can be disabled for power saving by setting CE to "**1**" and COE to "**0**".

5.10.4 Interrupt

- CMPIE (IOCF0.6) must be enabled.
- Interrupt occurs at a rising edge of the comparator output pin.
- The actual change on the pin can be determined by reading the Bit CMPOUT, R3<7>.
- CMPIF (RF.6), the comparator interrupt flag, can only be cleared by software.

5.10.5 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- Power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

5.11 Initialized Values after Reset

Table 5-9 Summary of the Registers Initialized Values

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCB0	Bit Name	/PD7	/PD6	*/PD5	*/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCC0	Bit Name	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCD0	Bit Name	/PH7	/PH6	/PH5	-	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCE0	Bit Name	WDTE	EIS	-	-	-	-	-	-
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	1	1	1	1	1	1
N/A	IOCF0	Bit Name	X	CMPIE	PMW2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	P	P	P	P	P	P	P

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC90 (GCON)	Bit Name	OP2E	OP1E	G22	G21	G20	G12	G11	G10
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCA0 (AD-CMP CON)	Bit Name	VREFS	CE	COE	IMS2	IMS1	IMS0	CKR1	CKR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC51 (PWM CON)	Bit Name	PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC61 (DT1L)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC71 (DT1H)	Bit Name	CALI1	SIGN1	VOF1[2]	VOF1[1]	VOF1[0]	-	PWM 1[9]	PWM 1[8]
		Power-on	0	1	1	0	0	0	0	0
		/RESET and WDT	0	1	1	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	0	P	P
N/A	IOC81 (PRD1)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC91 (DT2L)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCA1 (DT2H)	Bit Name	CALI2	SIGN2	VOF2[2]	VOF2[1]	VOF2[0]	-	PWM 2[9]	PWM 2[8]
		Power-on	0	1	1	0	0	0	0	0
		/RESET and WDT	0	1	1	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	0	P	P
N/A	IOCB1 (PRD2)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCC1 (DL1L)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCD1 (DL1H)	Bit Name	X	X	X	X	X	X	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	P	P
N/A	IOCE1 (DL2L)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCF1 (DL2H)	Bit Name	X	X	X	X	X	X	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	Jump to Address 0x08 or continue to execute next instruction							
0x03	R3 (SR)	Bit Name	CMPOUT	PS1	PS0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Changed	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	BS7	BS6	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x05	R5 (P5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x06	R6 (P6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07 ~ 0x08	R7~R8	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x09	R9 (ADCON)	Bit Name	X	X	IOCS	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x0A	RA (ADDDATA)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x0B	RB (TMR1L)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x0C	RC (TMR1H)	Bit Name	X	X	X	X	X	X	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	P	P
0x0D	RD (TMR2L)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x0E	RE (TMR2H)	Bit Name	X	X	X	X	X	X	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	P	P
0x0F	RF (ISR)	Bit Name	X	CMPIF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	P	P	P	P	P	P	P
0x10~ 0x3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P

Legend: *"x" = not used* *"P" = previous value before reset*

"u" = unknown or don't care *"t" = check Table 4-3*

5.12 Oscillator

5.12.1 Oscillator Modes

The EM78P458 and EM78P459 can be operated in four different oscillator modes, such as High Crystal oscillator mode (HXT), Low Crystal oscillator mode (LXT), External RC oscillator mode (ERC), and RC oscillator mode with Internal capacitor (IC). Users can select one of those by programming the Mask Option. The up-limited operating frequency of the crystal/resonator on the different VDD is listed in Table 5-10.

Table 5-10 Summary of the Maximum Operating Speeds

Conditions	VDD	Max. Fxt (MHz)
Two clocks	2.3	4
	3.0	8
	5.0	20

5.12.2 Crystal Oscillator/Ceramic Resonators (Crystal)

EM78P458/459 can be driven by an external clock signal through the OSCI pin as shown in Figure 5-17 below.

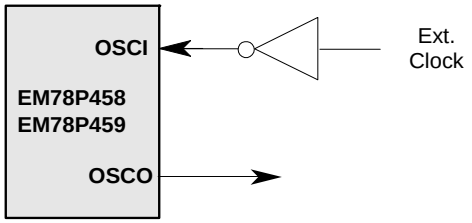


Figure 5-17 Circuit for External Clock Input

In the most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 5-18 depicts such a circuit. The same applies to the HXT mode and the LXT mode. Table 5-11 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to their specifications for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

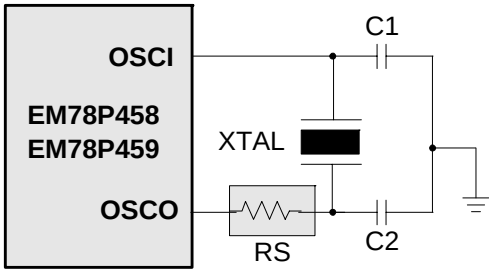


Figure 5-18 Circuit for Crystal/Resonator

Table 5-11 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

5.12.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Figure 5-19) could offer users with an effective cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be lesser than 20pF, and that the value of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB layout, have certain effect on the system frequency.

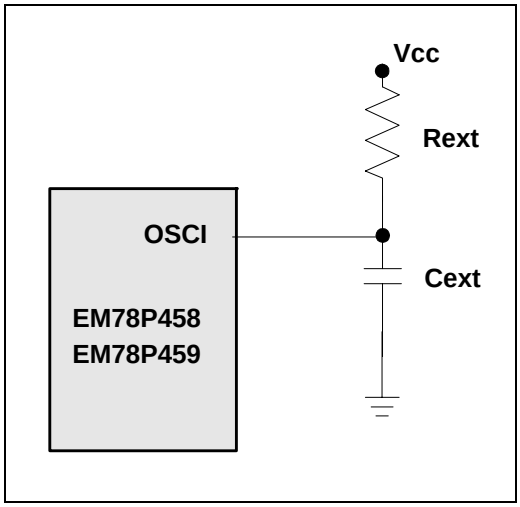


Figure 5-19 Circuit for External RC Oscillator Mode

Table 5-12 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.57 MHz	2.94 MHz
	5.1k	2.63 MHz	1.92 MHz
	10k	1.30 MHz	1.22 MHz
	100k	150kHz	153kHz
100 pF	3.3k	1.43 MHz	1.35 MHz
	5.1k	980kHz	877kHz
	10k	520kHz	465kHz
	100k	57kHz	54kHz
300 pF	3.3k	510kHz	470kHz
	5.1k	340kHz	320kHz
	10k	175kHz	170kHz
	100k	19kHz	19kHz

Note: 1. Measured on DIP packages

2. Design reference only

5.12.4 RC Oscillator Mode with Internal Capacitor

If both precision and cost are taken into consideration, EM78P257A/B also offers a special oscillation mode. It is equipped with an internal capacitor and an external resistor (connected to Vcc). The internal capacitor functions as temperature compensator. In order to obtain a more accurate frequency, a precise resistor is recommended.

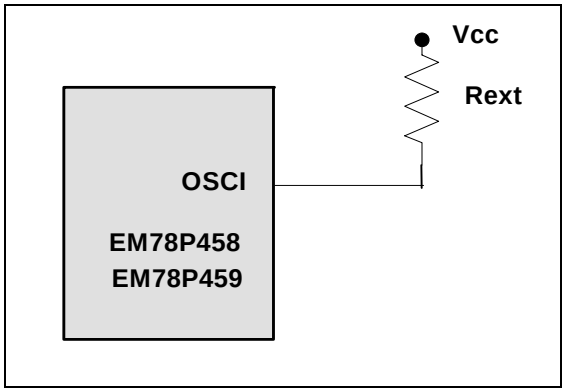


Figure 5-20 Circuit for Internal C Oscillator Mode

Table 5-13 R Oscillator Frequencies

Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
51k	2.22 MHz	2.17 MHz
100k	1.15 MHz	1.14 MHz
300k	375kHz	370 kHz

Note: 1. These are measured in DIP packages.

2. The values are for design reference only.

5.13 Power-on Considerations

Any microcontroller is not warranted to start proper operation before the power supply stabilizes in a steady state.

The EM78P458/459 POR voltage range is 1.2V~1.8V. Under customer application, when power is OFF, Vdd must drop to below 1.2V and remain OFF for 10 µs before power can be switched ON again. This way, the EM78P458/459 will reset and work normally. The extra external reset circuit will work well if Vdd can rise at a very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

5.13.1 External Power-on Reset Circuit

The circuits shown in Figure 5-21 use an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time. Because the current leakage from the /RESET pin is ± 5 µA, it is recommended that R should not be greater than 40K. In this way, the voltage at Pin /RESET is held below 0.2V. The diode (D) acts as a short circuit at power-down. The capacitor, C, is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

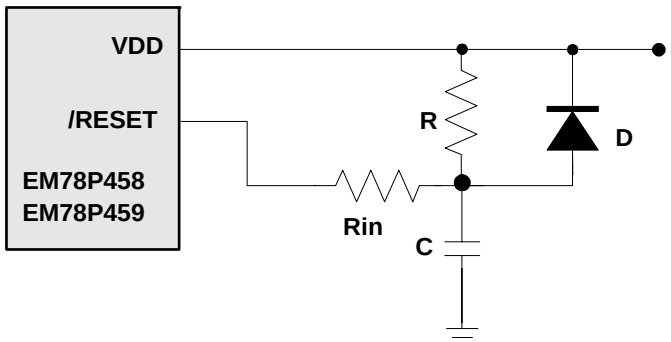


Figure 5-21 External Power on Reset Circuit

5.13.2 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 5-22 and Figure 5-23 show how to build a residue-voltage protection circuit.

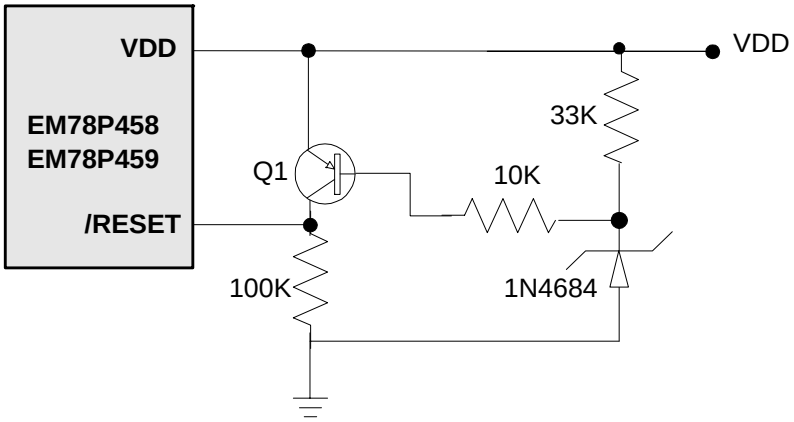


Figure 5-22 Residue Voltage Protection Circuit 1

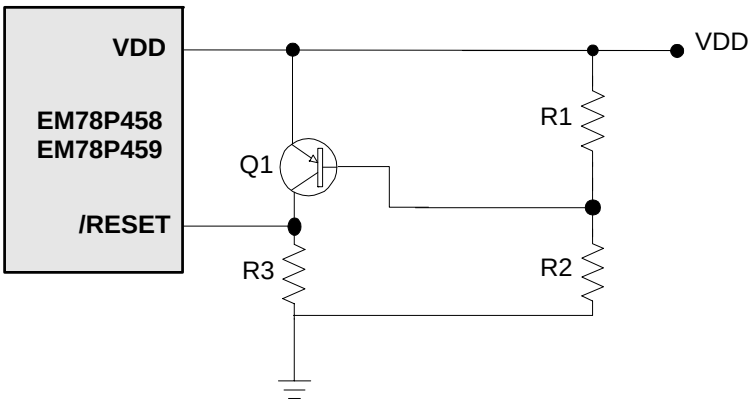


Figure 5-23 Residue Voltage Protection Circuit 2

5.14 Code Option

The EM78P458/459 has one Code Option word and one Customer ID word which are not part of the normal program memory.

5.14.1 Code Option Register (Word 0)

Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bits 5~0
Mnemonic	MS	/ENWDT	CLKS	/PTB	HLF	RCT	HLP	ID
1	Crystal Type	Disable	Four clocks	Disable	High frequency	1	High power	-
0	RC Type	Enable	Two clocks	Enable	Low frequency	0	Low power	-

Bit 12 (MS): Oscillator type selection

0: RC type

1: Crystal type

Bit 11 (/ENWTD): Watchdog timer enable bit

0: Enable

1: Disable

Bit 10 (CLKS): Clocks of each instruction cycle

0: Two clocks

1: Four clocks

Refer to the section on Instruction Set.

Bit 9 (/PTB): Protect bit

0: Enable

1: Disable

Bit 8 (HLF): Crystal frequency selection

0: Low frequency

1: High frequency

Bit 7 (RCT): Resistor Capacitor

0: Inter C, External R

1: External RC

Bit 6 (HLP): Power consumption selection

0: Low power

1: High power

Bit 5 ~ Bit 0 (ID[5]~ID[0]): Customer's ID

5.15 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

■ **Instruction Set Convention:**

R = *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b = *Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k = *8 or 10-bit constant or literal value*

Table 5-14 List of the Instruction Set of EM78P458/459

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note[1]>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note[1]>
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note[2]>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note[3]>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP], 001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC
0 0000 0010 0000	0020	TBL	R2+A → R2 Bits 8~9 of R2 unchanged	Z,C,DC

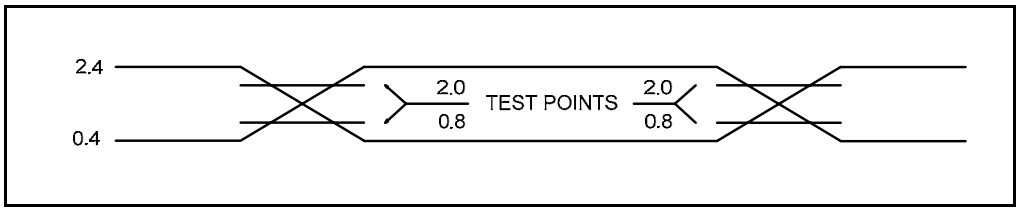
Note: [1] *This instruction is applicable to IOC50~IOC60, IOC90 ~ IOCF0, IOC51~ IOCF1 only.*

[2] *This instruction is not recommended for RF operation.*

[3] *This instruction **cannot** operate under RF operation.*

5.16 Timing Diagrams

AC Test Input/Output Waveform



Note: *AC Testing: Input is driven at 2.4V for Logic "**1**" and 0.4V for Logic "**0**"*
*Timing measurements are made at 2.0V for Logic "**1**" and 0.8V for Logic "**0**"*

Figure 5-24a AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK="0")

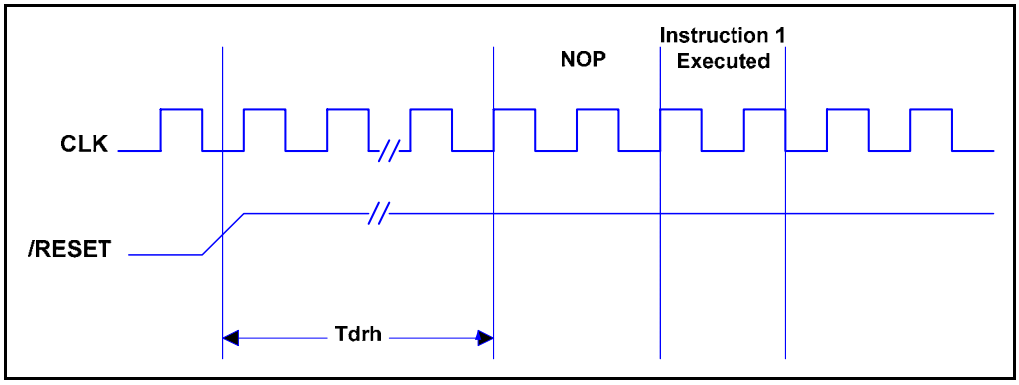


Figure 5-24b Reset Timing Diagram

TCC Input Timing (CLKS="0")

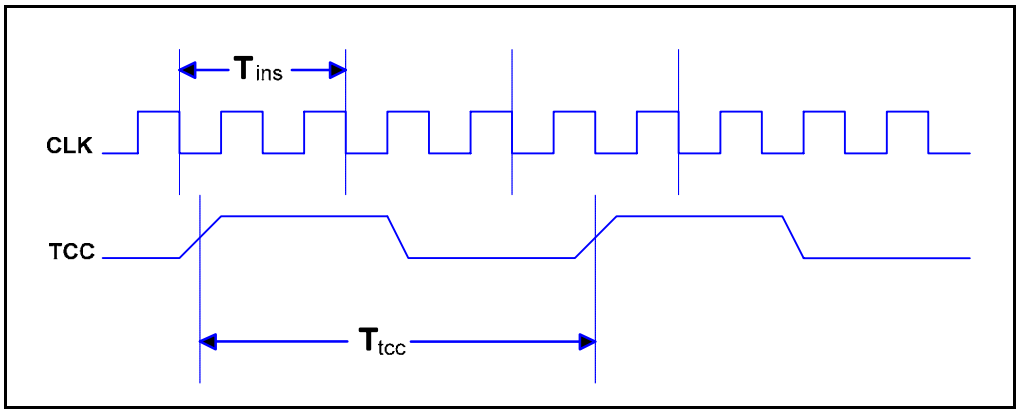


Figure 5-24c TCC Input Timing Diagram

6 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V

7 Electrical Characteristics

7.1 DC Electrical Characteristics

Ta=0°C ~ 70°C, VDD=5.0V ± 5%, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	XTAL: VDD to 3V	Two cycles with two clocks	DC	–	8	MHz
	XTAL: VDD to 5V		DC	–	20	MHz
	RC: VDD to 5V	R: 5.1KΩ, C: 100pF	F±30%	760	F±30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	µA
VIH1	Input High Voltage, VDD=5V	Ports 5, 6	2.0	–		V
VIL1	Input Low Voltage, VDD=5V	Ports 5, 6	–	–	0.8	V
VIHT1	Input High Threshold Voltage, VDD=5V	/RESET, TCC	2.0	–	–	V
VILT1	Input Low Threshold Voltage,VDD=5V	/RESET, TCC	–	–	0.8	V
VIHX1	Clock Input High Voltage,VDD=5V	OSCI	2.5	–		V
VILX1	Clock Input Low Voltage,VDD=5V	OSCI	–	–	1.0	V
VIH2	Input High Voltage,VDD=3V	Ports 5, 6	1.5	–	–	V
VIL2	Input Low Voltage,VDD=3V	Ports 5, 6	–	–	0.4	V
VIHT2	Input High Threshold Voltage,VDD=3V	/RESET, TCC	1.5	–	–	V
VILT2	Input Low Threshold Voltage,VDD=3V	/RESET, TCC	–	–	0.4	V
VIHX2	Clock Input High Voltage,VDD=3V	OSCI	1.5	–		V
VILX2	Clock Input Low Voltage,VDD=3V	OSCI	–	–	0.6	V
VOH1	Output High Voltage (Ports 5, 6)	IOH = -12.0 mA	2.4	–	–	V
VOL1	Output Low Voltage (P51~P57, P60~P63, P66~P67)	IOL = 12.0 mA	–	–	0.4	V
VOL2	Output Low Voltage (P64,P65)	IOL = 16.0 mA	–	–	0.4	V
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-100	-240	µA
IPD	Pull-down current	Pull-down active, input pin at VDD	25	50	120	µA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ISB	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	–	10	µA
ISB	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	–	1	µA
ICC1	Operating supply current (VDD=3V) at two clocks	/RESET='High', Fosc=32kHz (Crystal type, two clocks), Output pin floating, WDT disabled	–	15	30	µA
ICC2	Operating supply current (VDD=3V) at two clocks	/RESET='High', Fosc=32kHz (Crystal type, two clocks), Output pin floating, WDT enabled	–	19	35	µA
ICC3	Operating supply current (VDD=5.0V) at two clocks	/RESET='High', Fosc = 2 MHz (Crystal type, two clocks), Output pin floating	–	–	2	mA
ICC4	Operating supply current (VDD=5.0V) at two clocks	/RESET='High', Fosc = 4 MHz (Crystal type, two clocks), Output pin floating	–	–	4.0	mA

7.2 AC Electrical Characteristics

Ta=0°C ~ 70°C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type RC type	100 500	–	DC DC	ns ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	9	18	30	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	9	18	30	ms
Tset	Input pin setup time	–	–	0	–	ms
Thold	Input pin hold time	–	–	20	–	ms
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ms

**N = selected prescaler ratio*

7.3 A/D Converter Characteristics

Vdd = 3.0V to 5.5V, Vss = 0V, Ta = 0 to 70°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VAREF	Analog reference voltage	VAREF – VASS ≥ 2.5V	3.0	–	Vdd	V
VASS			–	–	Vss	V
VAI	Analog input voltage	–	VASS	–	VAREF	V
IAI	Analog supply current	Vdd=VAREF=5.0V, VASS =0.0V	500	700	1000	μA
RN	Resolution	Vdd=VAREF=5.0V, VASS =0.0V	6	7	8	Bits
LN	Linearity error	Vdd = 2.5 to 5.5V Ta=25°C	0	±2	±4	LSB
DNL	Differential nonlinear error	Vdd = 2.5 to 5.5V Ta=25°C	0	±0.5	±0.9	LSB
FSE	Full scale error	Vdd=VAREF=5.0V, VASS =0.0V	±0	±2	±4	LSB
OE	Offset error	Vdd=VAREF=5.0V, VASS =0.0V	±0	±1	±2	LSB
ZAI	Recommended impedance of analog voltage source	–	0	8	10	KΩ
TAD	A/D clock period	Vdd=VAREF=5.0V, VASS =0.0V	3	3.5	4	μs
TCN	A/D conversion time	Vdd=VAREF=5.0V, VASS =0.0V	10	–	10	TAD
ADIV	A/D OP input voltage range	Vdd=VAREF=5.0V, VASS =0.0V	0	–	5	V
ADOV	A/D OP output voltage swing	Vdd=VAREF=5.0V, VASS =0.0V, RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
ADSR	A/D OP slew rate	Vdd=VAREF=5.0V, VASS =0.0V	0.1	0.3	–	V/μs
PSR	Power Supply Rejection	Vdd=5.0V±0.5V	±0	–	±2	LSB

NOTE

1. *These parameters are characterized but not tested.*
2. *These parameters are for design reference only and are not tested.*
3. *It will not consume any current other than minor leakage current, when A/D is off.*
4. *The A/D conversion result never decrease with an increase in the input voltage, and has no missing code.*
5. *The Specifications are subject to change without prior notice.*

7.4 Comparator (OP) Characteristics

Vdd = 5.0V,Vss=0V,Ta=0 to 70°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SR	Slew rate	–	0.1	0.2	–	V/µs
IVR	Input voltage range	Vdd =5.0V, VSS =0.0V	0	–	5	V
OVS	Output voltage swing	Vd =5.0V, VSS =0.0V, RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
Iop	Supply current of OP	–	250	350	500	µA
PSRR	Power-supply Rejection Ration for OP	Vdd= 5.0V, VSS =0.0V	50	60	70	dB
Vos	Offset voltage	Vdd= 5.0V, VSS =0.0V	–	±10	±20	mV
Vs	Operating range	–	2.5	–	5.5	V

NOTE

1. These parameters are characterized but not tested.

2. These parameters are for design reference only and are not tested.

3. The Specifications are subject to change without prior notice.

7.5 Device Characteristics

The graphic provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristics illustrated herein are not guaranteed for its accuracy. In some graphic, the data maybe out of the specified warranted operating range.

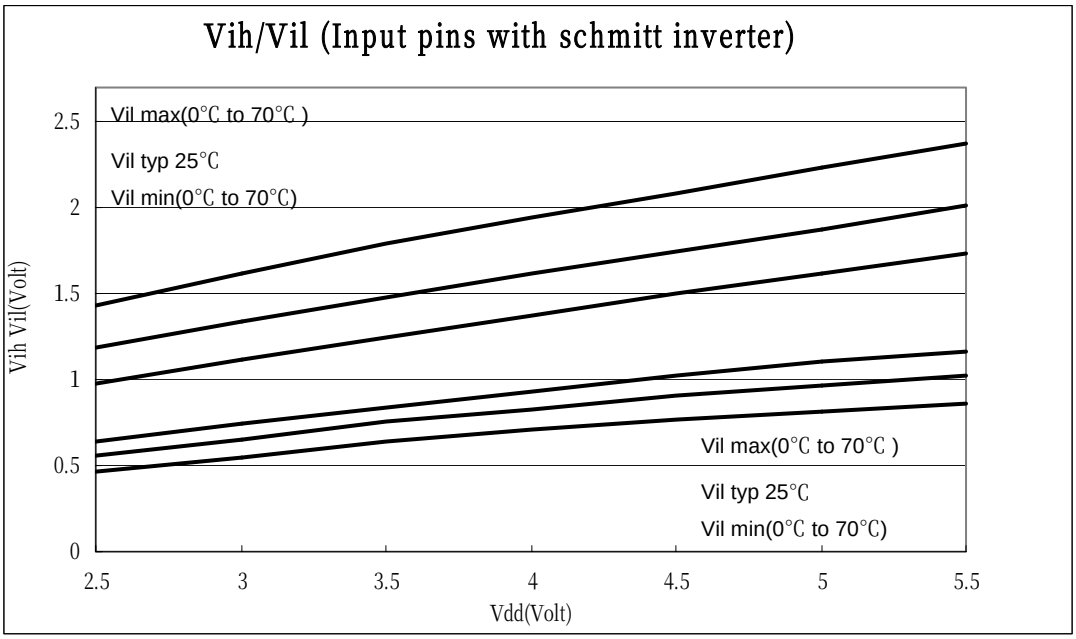


Figure 7-1 Vih, Vil of P50 Vs VDD

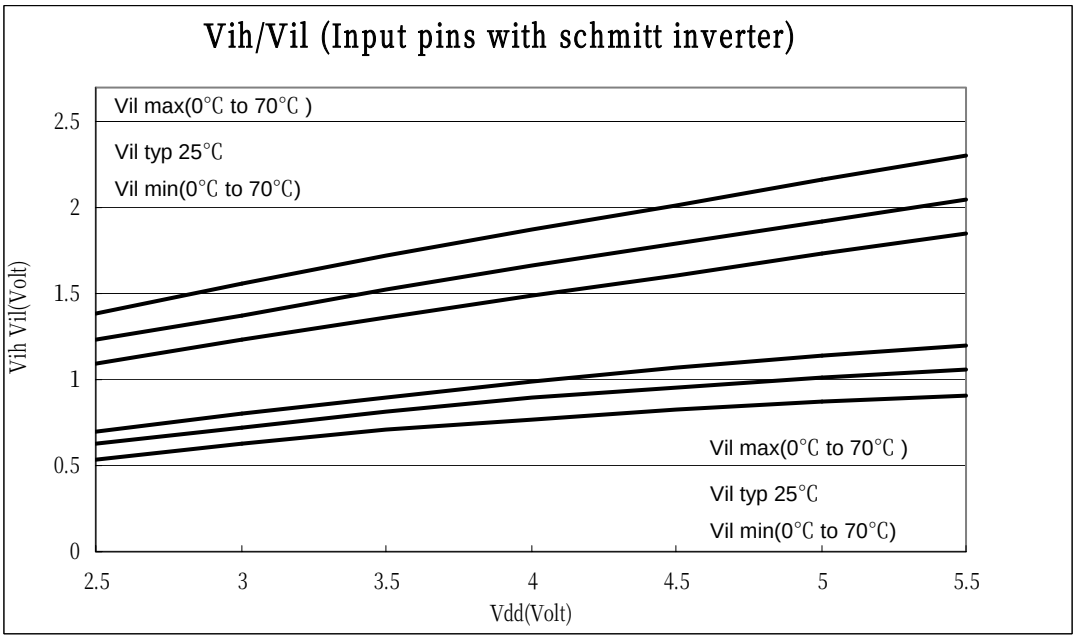


Figure 7-2 Vih, Vil of P51, P52, P54 Vs VDD

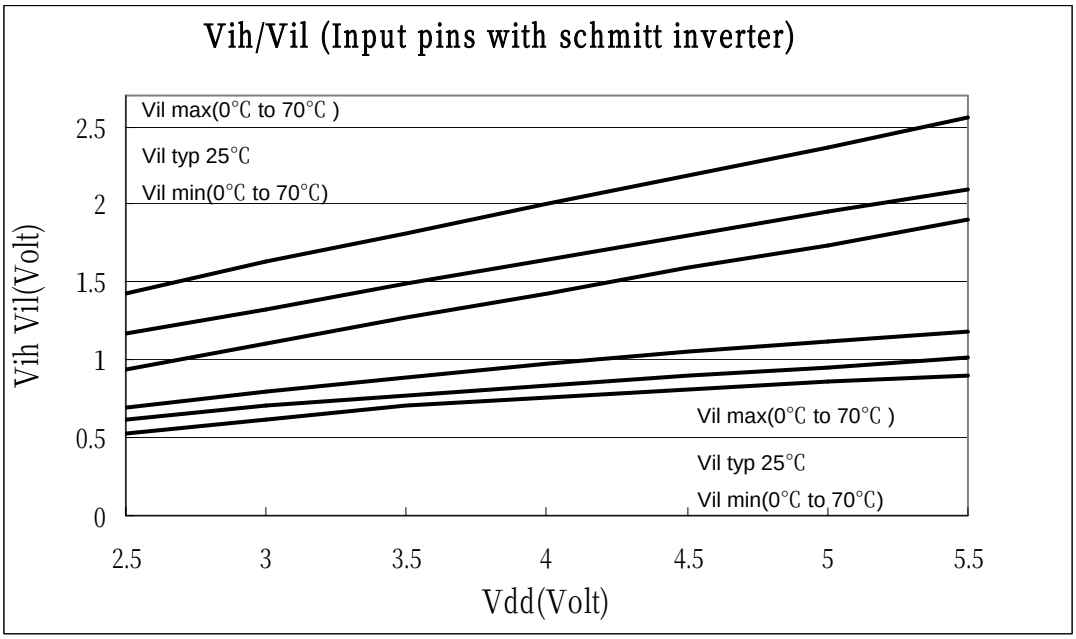


Figure 7-3 Vih, Vil of P53, P55~P57,P60~P67 Vs VDD

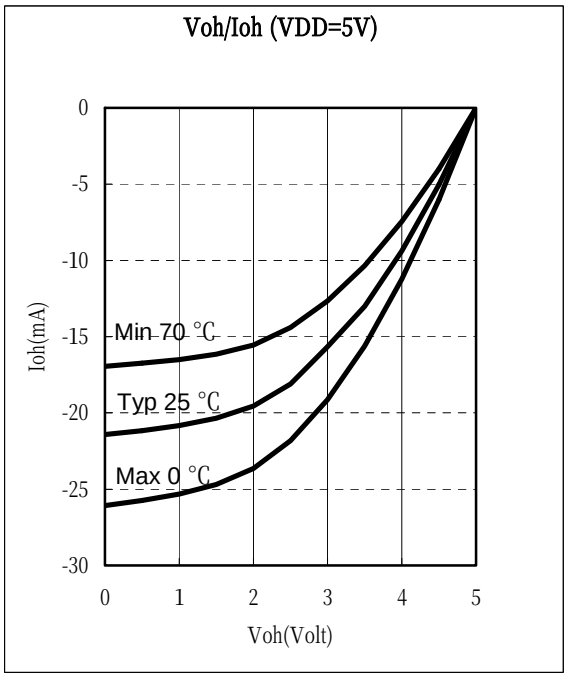


Figure 7-4 Port 5, Port 6, Voh vs. Ioh, VDD=5V

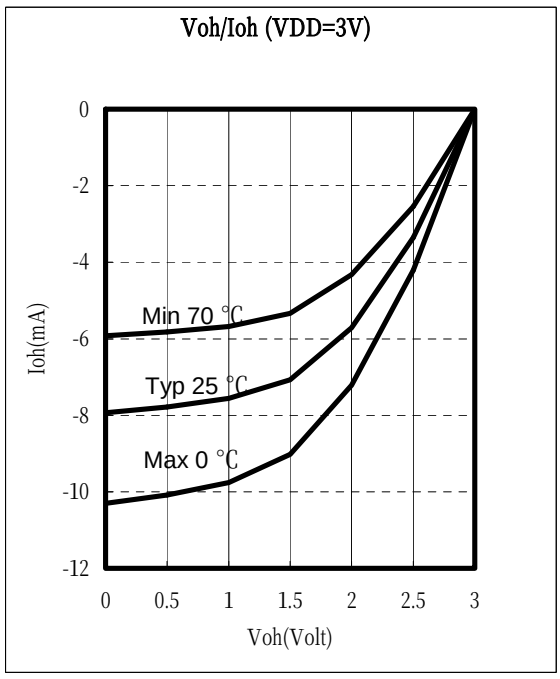


Figure 7-5 Port 5, Port 6, Voh vs. Ioh, VDD=3V

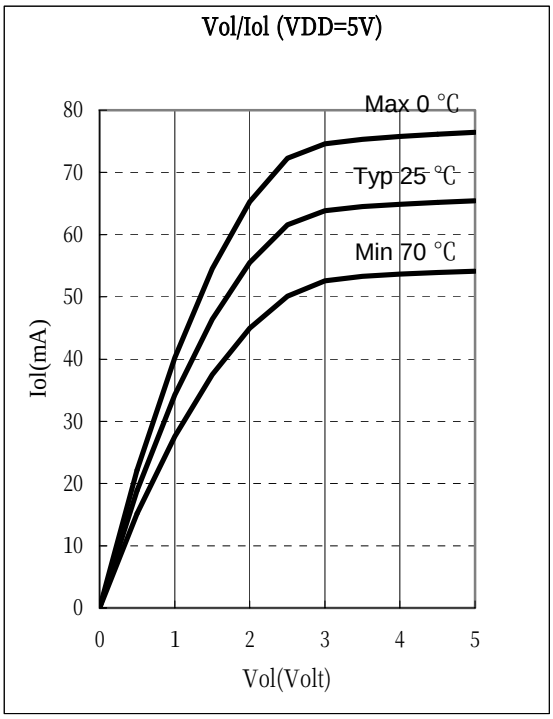


Figure 7-6 Port 5, and P60~P63, P66, P67 Vol, VDD=3V

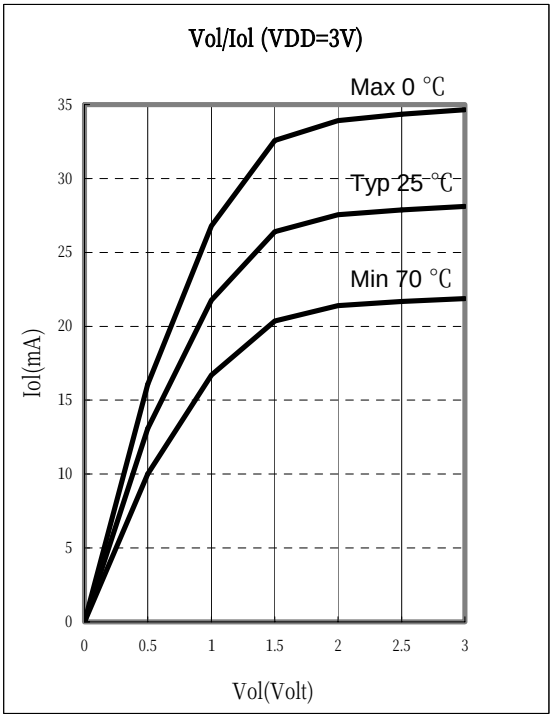


Figure 7-7 Port 5, and P60~P63, P66, P67 Vol VDD=5V

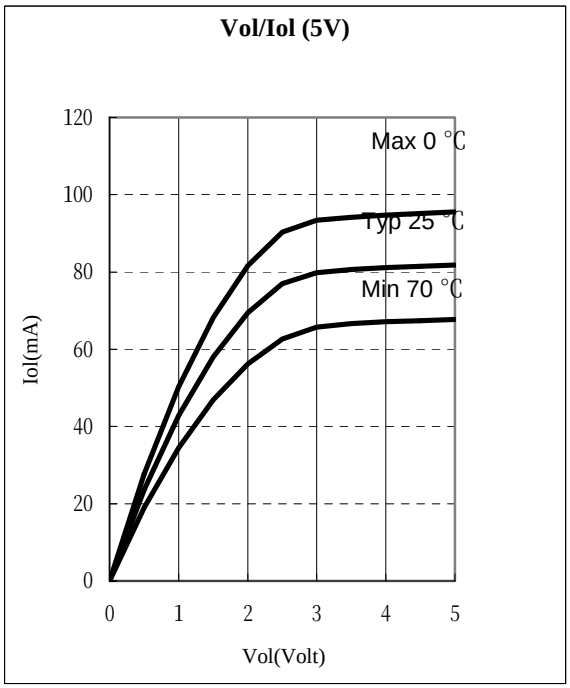


Figure 7-8 P64, P65 Vol vs. Iol, VDD=5V

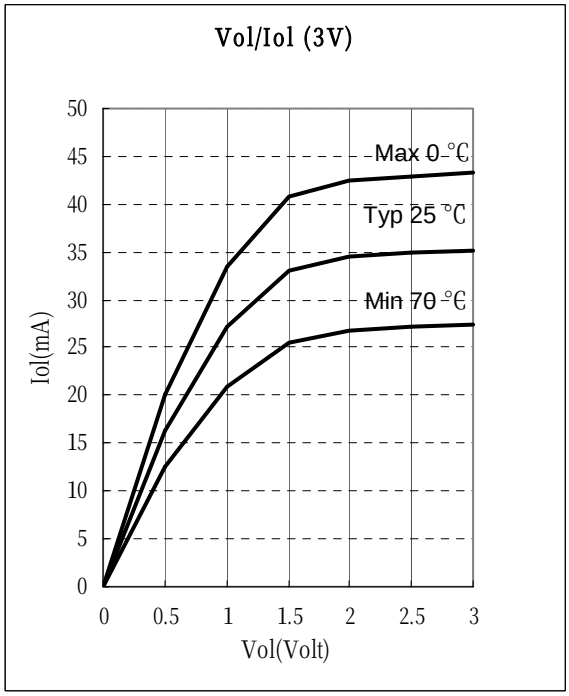


Figure 7-9 P64, P65 Vol vs. Iol, VDD=3V

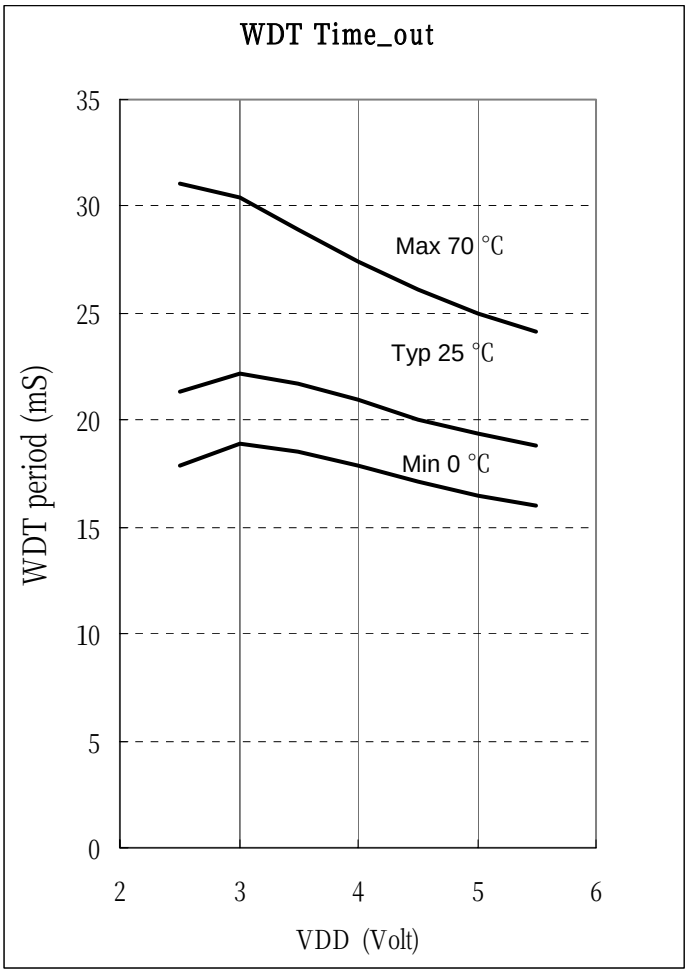


Figure 7-10 WDT Time Out Period vs. VDD, Prescaler Set to 1:1

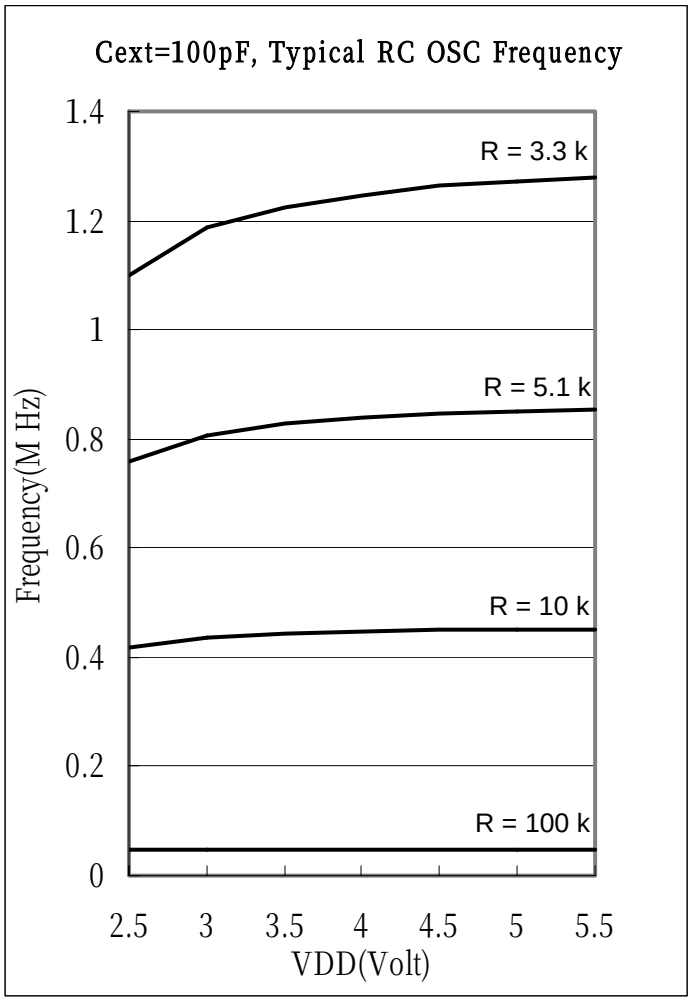


Figure 7-11 Typical RC OSC Frequency vs. VDD （Cext=100pF, Temperature at 25°C）

Four conditions exist with the operating current ICC1 to ICC4. The conditions are as follows：

ICC1：VDD=3V, Fosc=32kHz, 2 clocks, WDT disable.

ICC2：VDD=3V, Fosc=32kHz, 2 clocks, WDT enable.

ICC3：VDD=5V, Fosc=2 MHz, 2 clocks, WDT enable.

ICC4：VDD=5V, Fosc=4 MHz, 2 clocks, WDT enable.

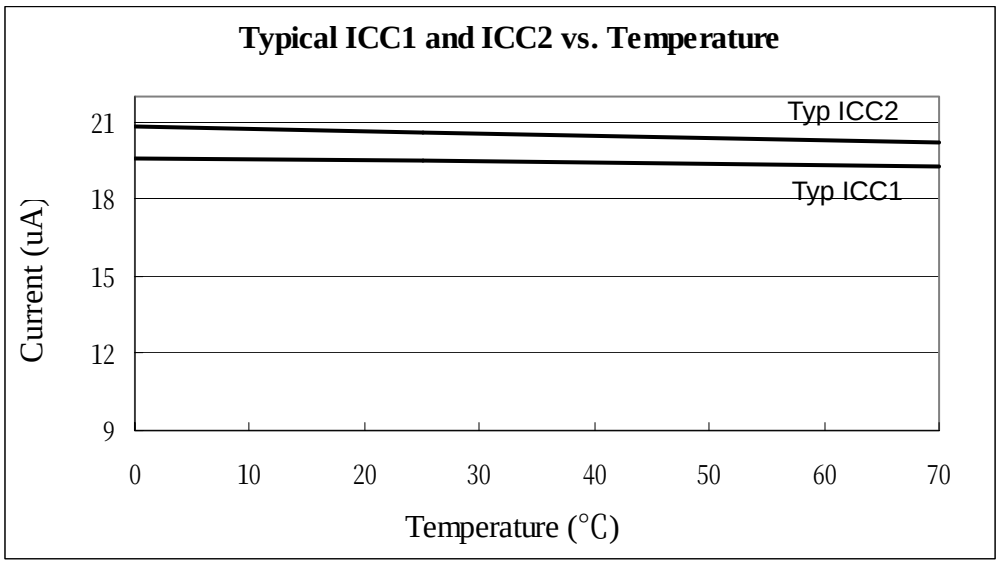


Figure 7-12 Typical Operating Current（ICC1 and ICC2） vs. Temperature

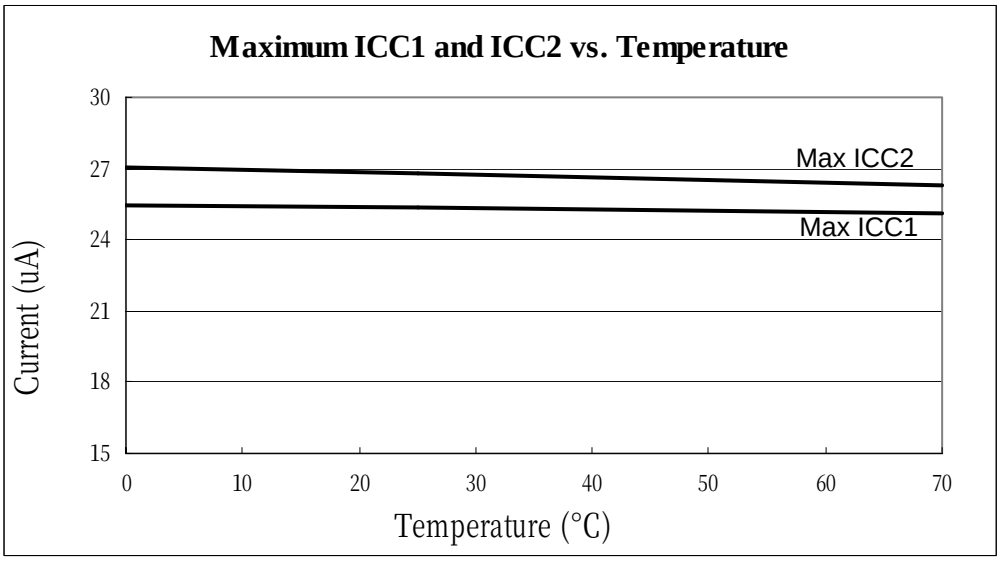


Figure 7-13 Maximum Operating Current（ICC1 and ICC2） vs. Temperature

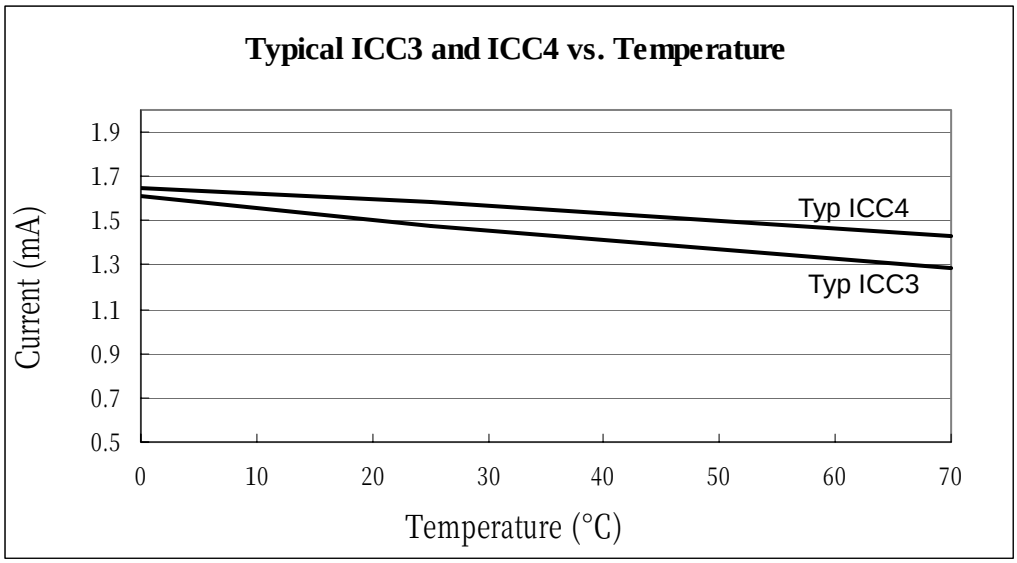


Figure 7-14 Typical Operating Current（ICC3 and ICC4） vs. Temperature

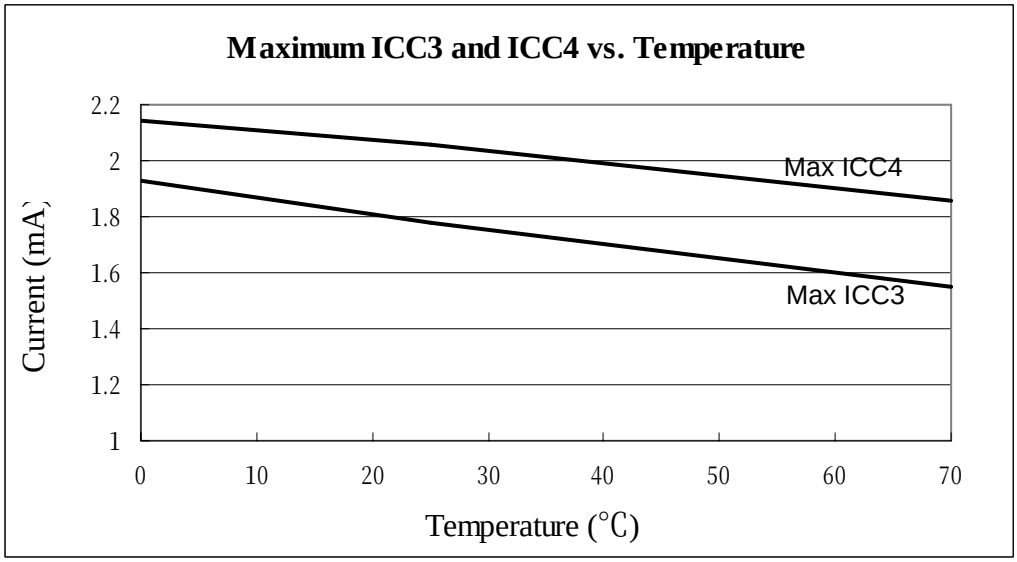


Figure 7-15 Maximum Operating Current（ICC3 and ICC4） vs. Temperature

Two conditions exist with the standby current ISB1 and ISB2. These conditions are as follows:

ISB1：VDD=5V, WDT disable

ISB2：VDD=5V, WDT enable

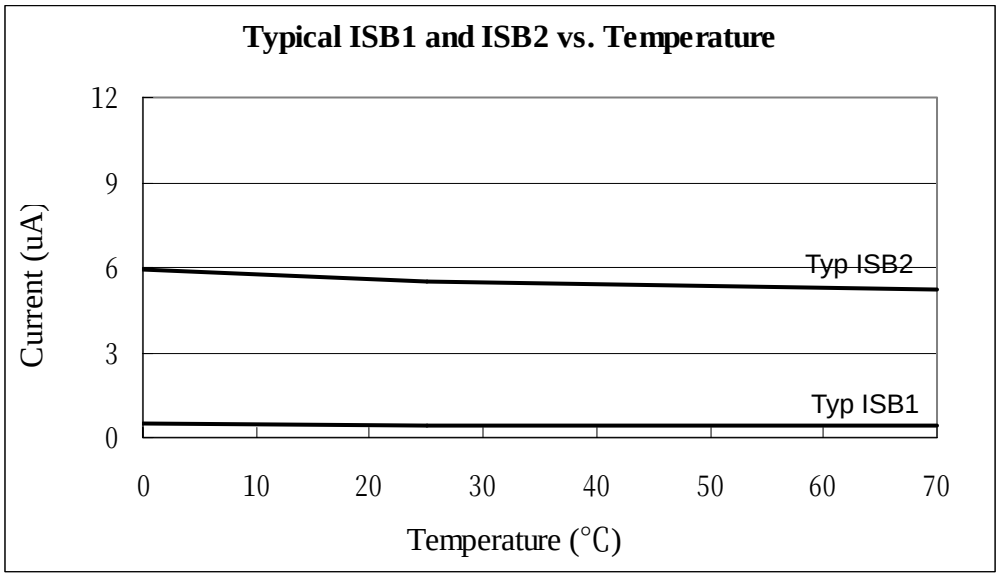


Figure 7-16 Typical Standby Current（ISB1 and ISB2） vs. Temperature

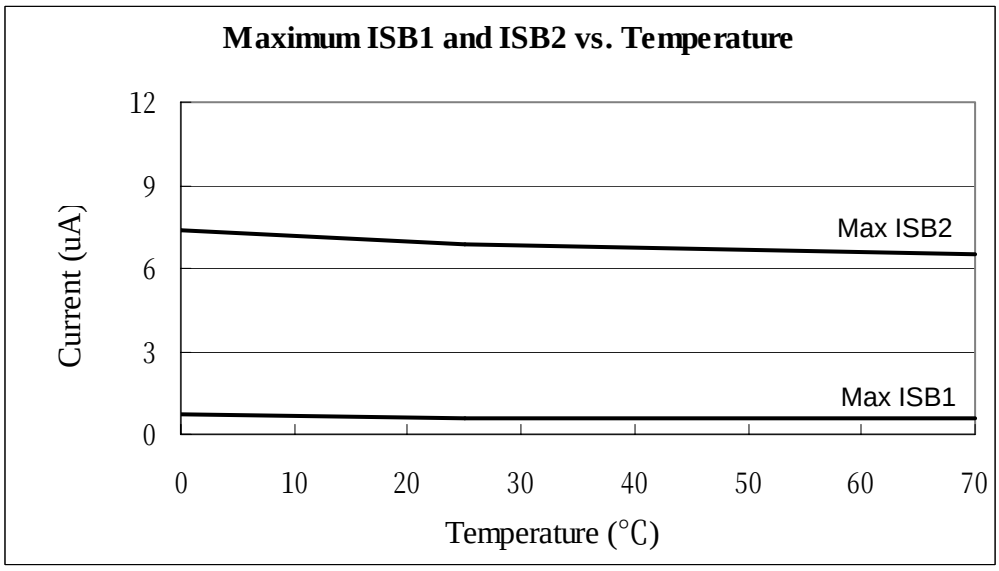


Figure 7-17 Maximum Standby Current（ISB1 and ISB2） vs. Temperature

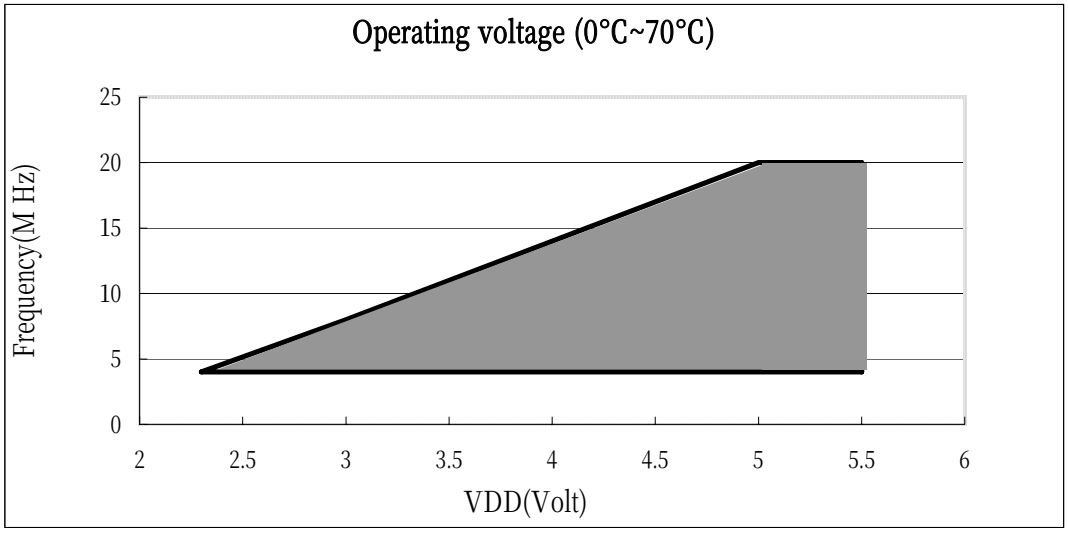


Figure 7-18 Operating Voltage in Temperature Range from 0°C to 70°C

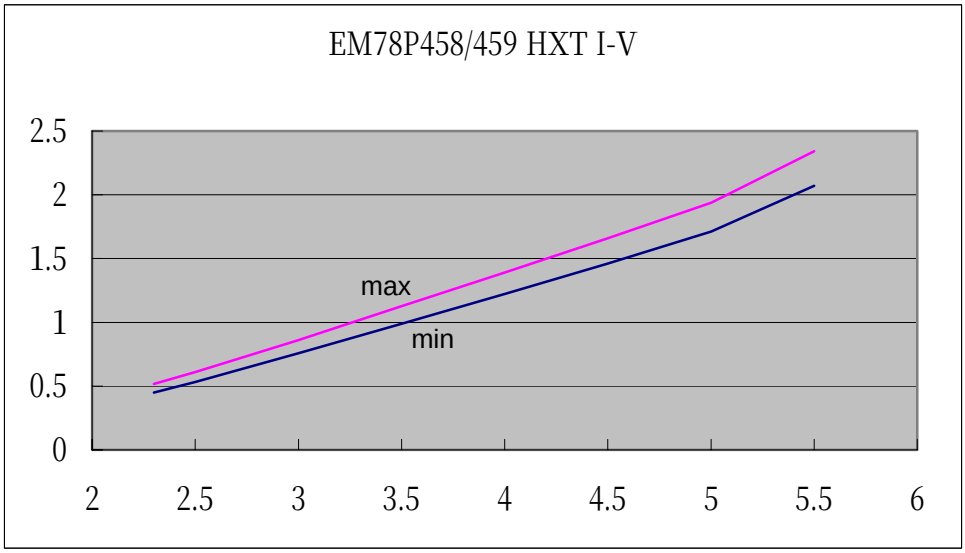


Figure 7-19 EM78P458/459 I-V Curve Operating at 4 MHz

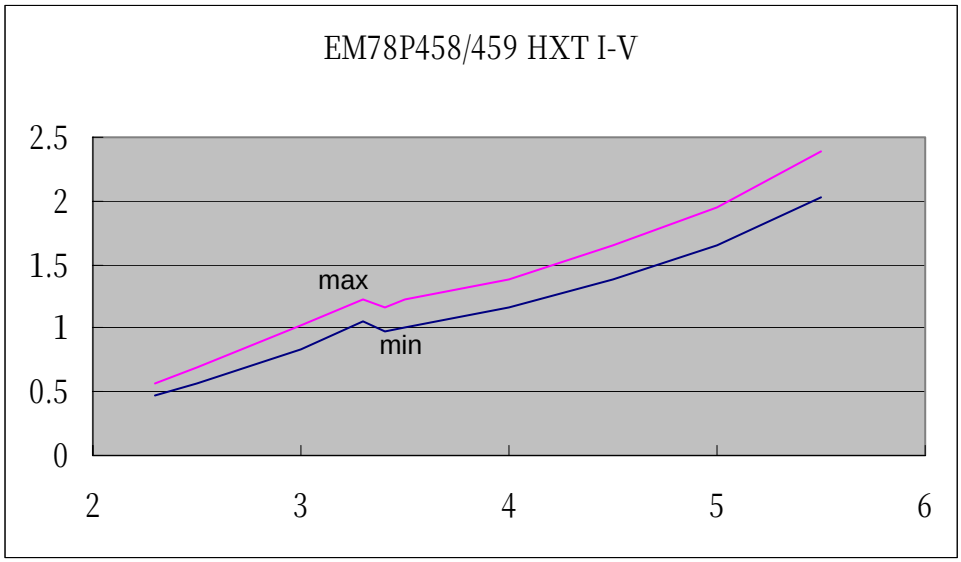


Figure 7-20 EM78P458_G/459-G I-V Curve Operating at 4 MHz

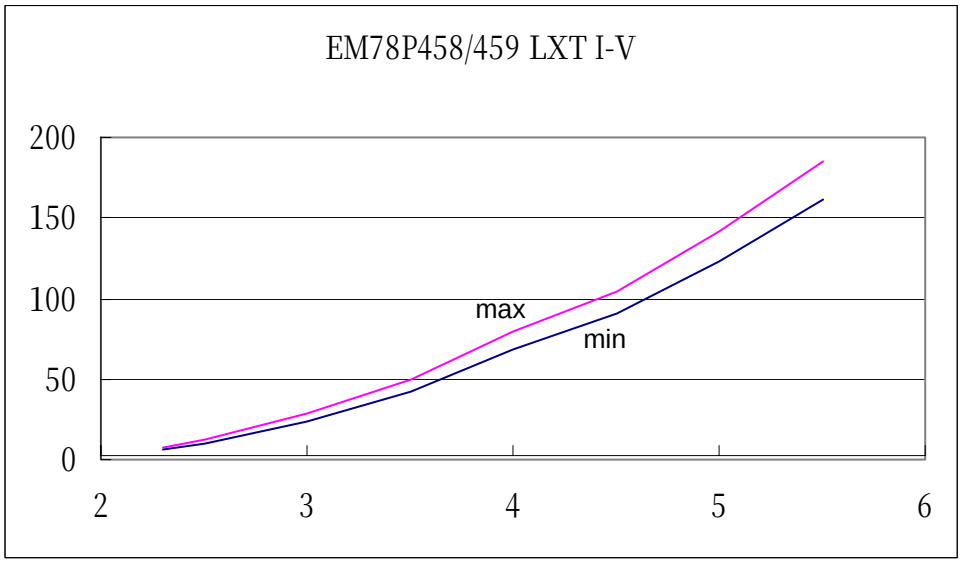


Figure 7-21 EM78P458/459 I-V Curve Operating at 32.768 kHz

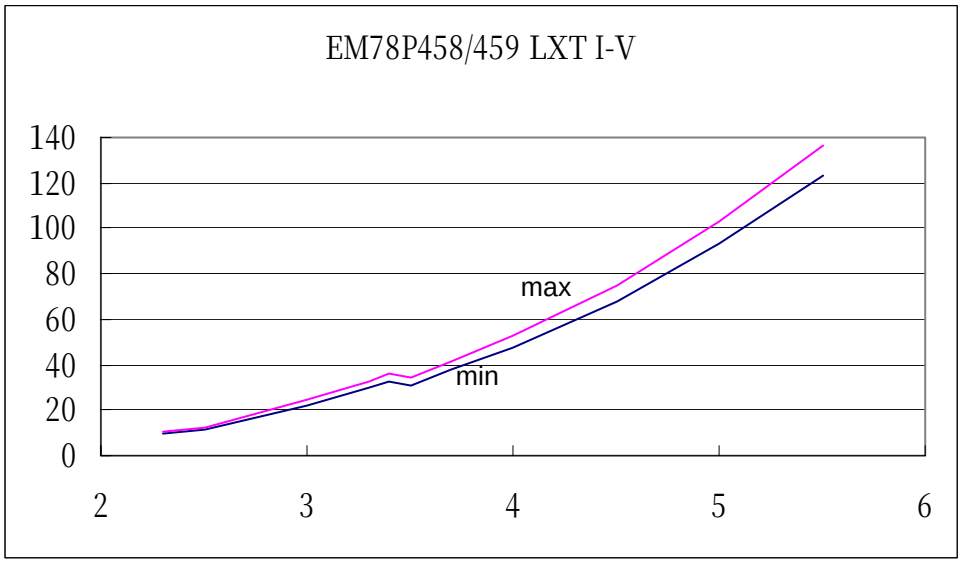


Figure 7-22 EM78P458_G/459_G I-V Curve Operating at 32.768kHz

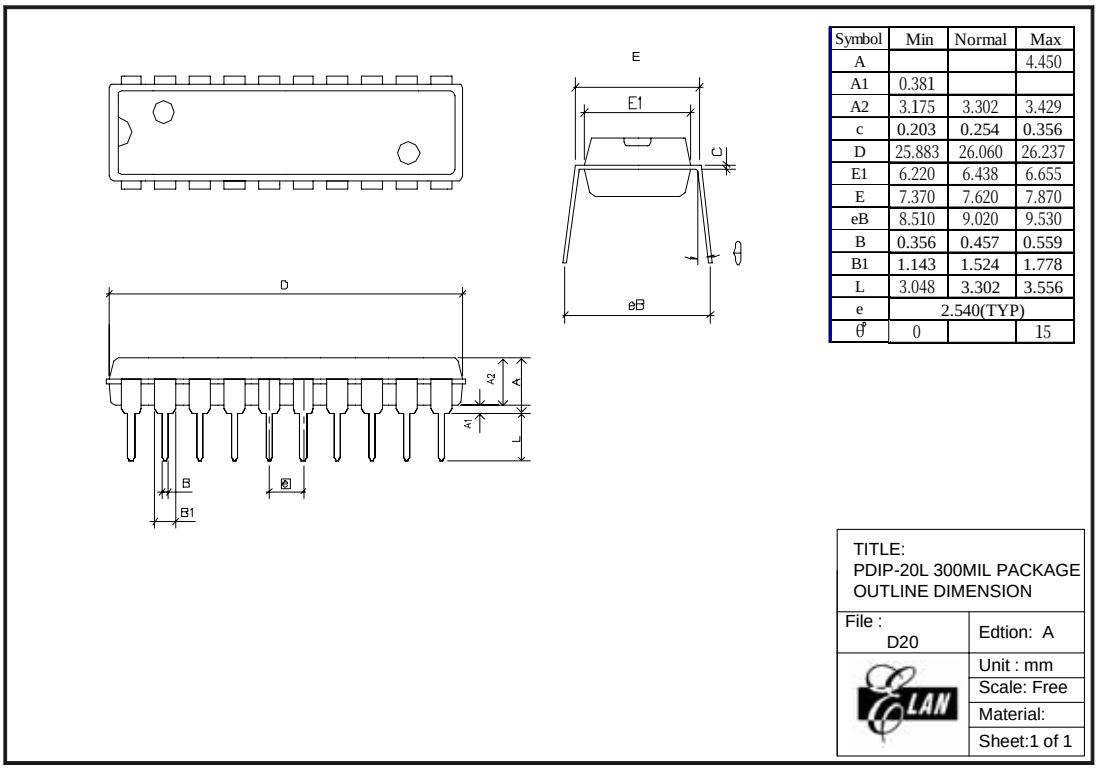
APPENDIX

A Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P458AP	DIP	20 pins	300 mil
EM78P458AM	SOP	20 pins	300 mil
EM78P459AK	Skinny DIP	24 pins	300 mil

B Package Information

20-Lead Plastic Dual in line (PDIP) — 300 mil

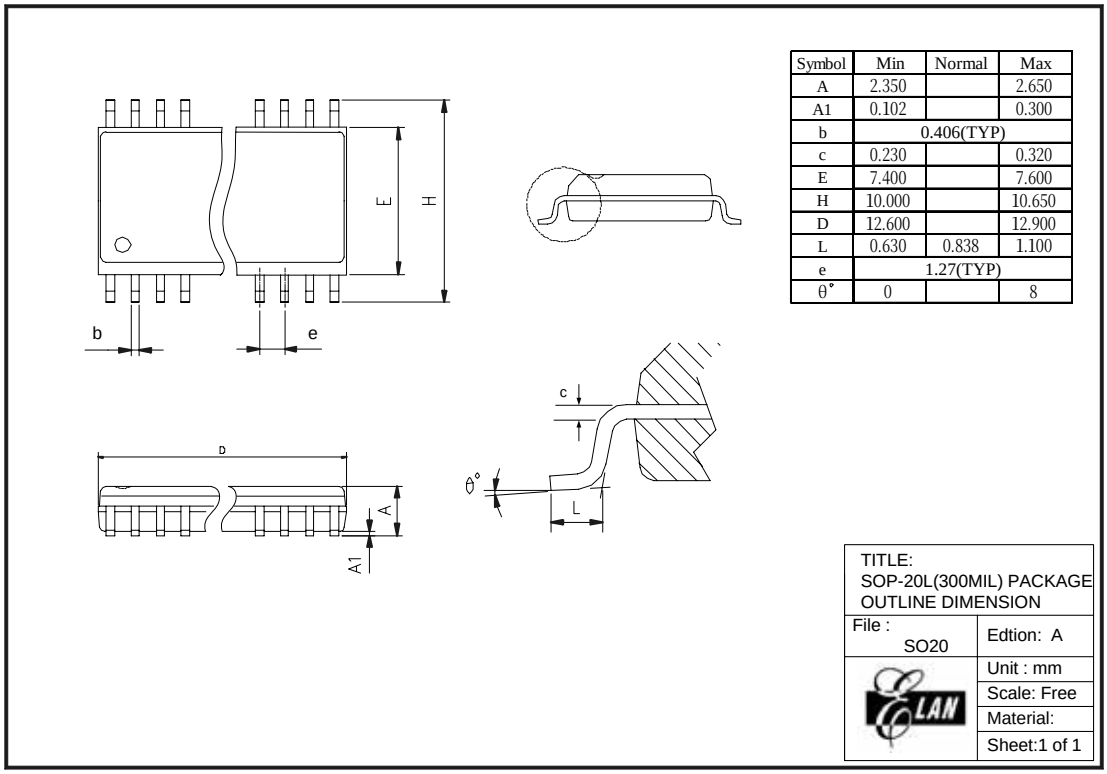


Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

TITLE:
PDIP-20L 300MIL PACKAGE
OUTLINE DIMENSION

File : D20 | Edtion: A
Unit : mm
Scale: Free
Material:
Sheet:1 of 1

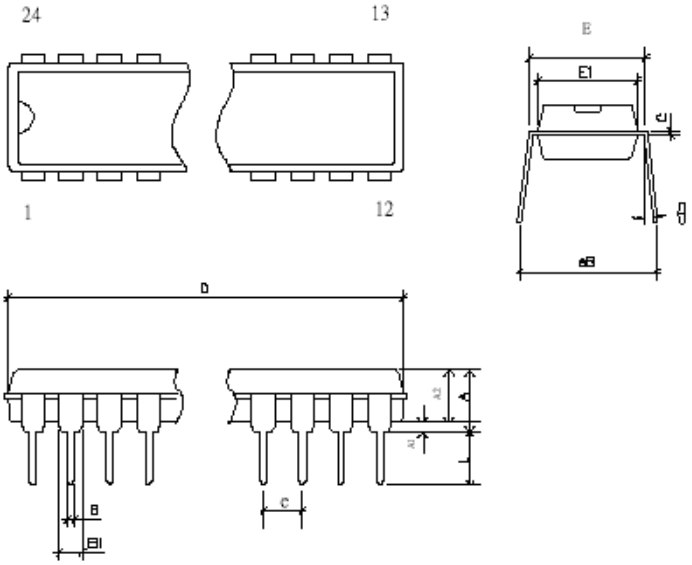
20-Lead Plastic Small Outline (SOP) — 300 mil



Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

24-Lead Plastic Dual in line (PDIP) — 300 mil



Symbol	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	31.750	31.801	31.852
E1	6.426	6.628	6.830
E	7.370	7.620	7.870
eB	8.380	8.950	9.520
B	0.356	0.457	0.559
B1	1.470	1.520	1.630
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-24L SKINNY 300MIL PACKAGE OUTLINE DIMENSION	
File : K24	Edition: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1