EM78P469

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.3

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2008/04/16
1.1	1. Added an important note about LCD control in Section 12 – *Application Note.* 2. Modified the P90~P94 location in AQ64L and AL64J, See Package Type.	2008/05/26
1.2	Corrected the Features description from 84K×13 to 8K×13 on-chip Electrical One Time Programmable Read Only Memory (OTP-ROM).	2008/09/24
1.3	1. Added TS/TCS in the Application Note 2. Removed any unsuitabie words and improved the text contents.	2009/02/03

1 General Description

The EM78P469 is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. Integrated onto a single IC are on-chip Watchdog Timer (WDT), Data RAM, ROM, programmable real time clock counter, internal/external interrupt, power-down mode, LCD driver IROUT function and tri-state I/O.

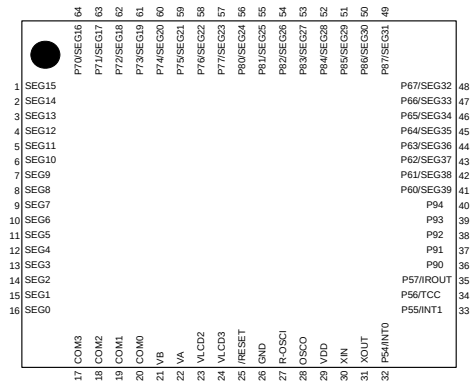
2 Features

- CPU configuration
  - 8K×13 on-chip Electrical One Time Programmable Read Only Memory (OTP-ROM)
  - 144 bytes general purpose register
  - 512×8 bits on-chip data RAM
  - 8-level stacks for subroutine nesting
- I/O port configuration
  - Up to 33 bidirectional tri-state I/O ports
- Operating voltage: 2.3V ~ 5.5V
- Operating temperature: -20℃~+85℃
- Operating mode:
  - Normal mode
  - Green mode
  - Idle mode
  - Sleep mode
    - Input port wake-up function (Port 6, Port 8)
    - 8 interrupt sources: 2 external, 6 internal
- Dual clock operation or PLL operation mode
- Oscillation mode
  - Crystal/RC oscillation circuit selected by Code option for system clock
  - 32.768kHz Crystal/RC oscillation circuit selected by Code option for sub-oscillation
- Peripheral configuration
  - 8-bit real time clock/counter (TCC)
  - One IROUT/PWM generator
  - Four sets of 8-bit auto reload counter/timer can be used as interrupt sources
  - 16-bit counter: Combined CNT1 with CNT2
  - Programmable free running on-chip Watchdog Timer (WDT)
- LCD Circuit
  - Common driver pins: 4
  - Segment driver pins: 40
  - LCD Bias: 1/3, 1/2 bias
  - LCD Duty: 1/4, 1/3, 1/2 duty
- Package type:
  - 44-pin QFP : EM78P469Q44J
  - 44-pin LQFP : EM78P469L44J
  - 64-pin QFP : EM78P469AQ64BJ
  - 64-pin QFP : EM78P469BQ64BJ
  - 64-pin LQFP : EM78P469AL64J
  - 64-pin LQFP : EM78P469BL64J

3 Applications

- Remote control for air conditioners
- Health care
- Home appliances

5 Package Type



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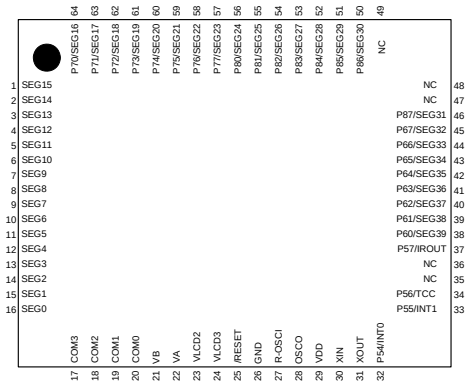

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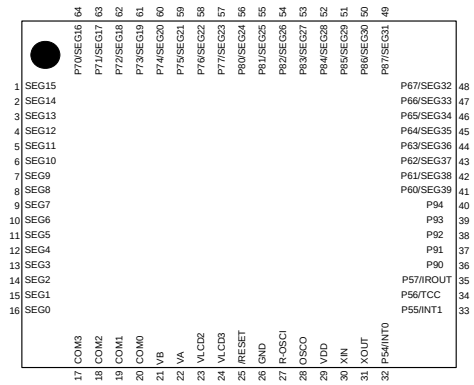

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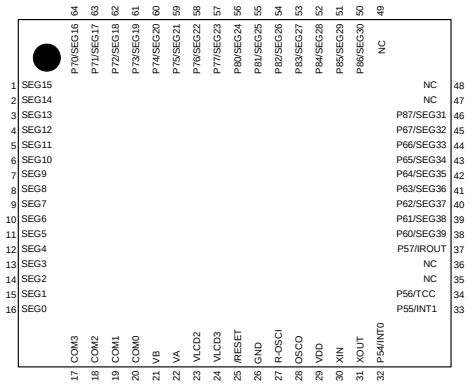

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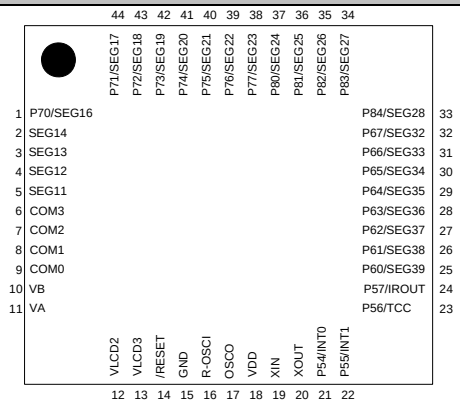

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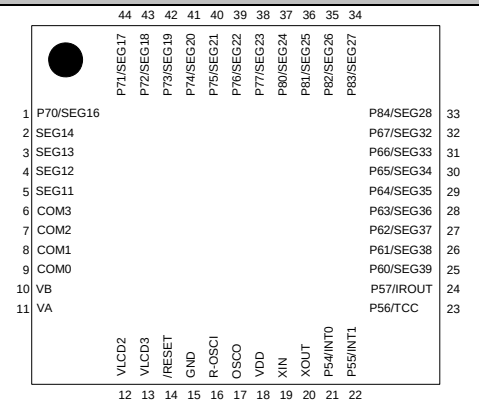

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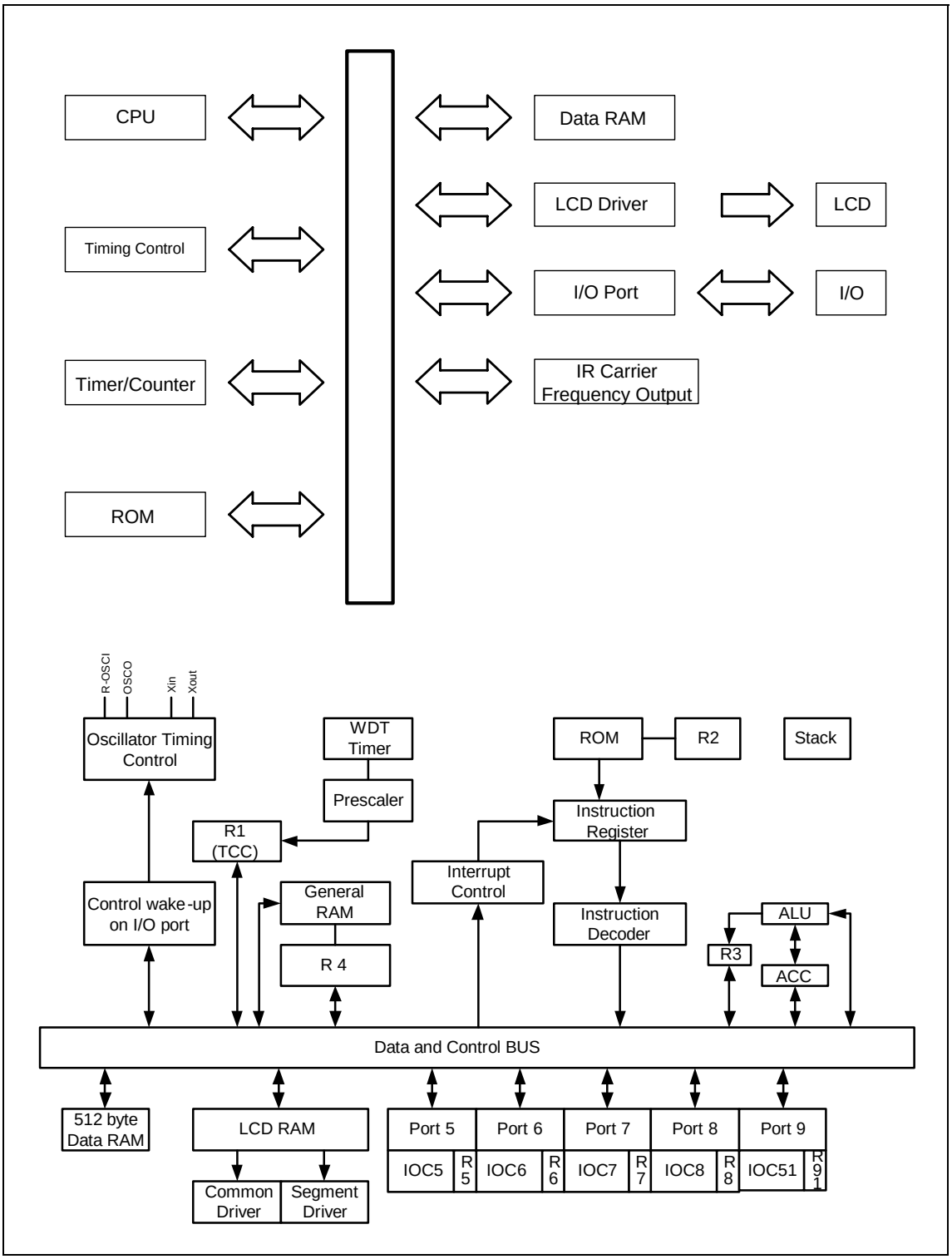
5 Functional Block Diagram



7 Pin Description

Pin	I/O Type	Description
P5.4/INT0 P5.5/INT1	I/O	General purpose I/O pin-shared with external interrupt. INT0 interrupt source can be set as falling or rising edge by IOC7 Page 1 Register Bit 7 (INT_EDGE). INT1, an interrupt source is a falling edge signal. All pins can wake-up from sleep mode when the status of the pin changes.
P5.6/TCC	I/O	General purpose I/O pin-shared with external counter input. This pin can wake-up from sleep mode and idle mode while the status of the pin changes.
P5.7/IROUT	I/O	General purpose I/O or IR mode output pin, capable of sinking 30 mA. This pin can wake-up from sleep mode and idle mode while the status of the pin changes.
P9.0~P9.4	I/O	General purpose I/O pin
R-OSCI	I	In crystal mode: crystal input In RC mode: resistor pull-high In PLL mode: connect a capacitance to GND
OSCO	O	In crystal mode: crystal output In RC mode: instruction clock output
Xin	I	In crystal mode: Input pin for sub-oscillator. Connect to a 32.768kHz crystal RC mode: resistor pull high
Xout	O	In crystal: Connect to a 32.768kHz crystal
/RESET	I	Low active. If set as /RESET and remains at logic low, the device will be reset.
SEG32 / P6.7 ~ SEG39 / P6.0	O/(I/O)	General purpose I/O pin or LCD segment output pin. Pull-high/ pull-down/ Open drain while set to general purpose I/O pin. All pins can wake up from sleep mode and idle mode when the status of the pin changes while set as general purpose I/O pin.
COM3~0	O	LCD common output pin
SEG0~SEG15	O	LCD segment output pin
SEG16 / P7.0 ~ SEG23 / P7.7	O/(I/O)	LCD segment output pin. Can shared with general purpose I/O pin
SEG24 / P8.0 ~ SEG31 / P8.7	O/(I/O)	LCD segment output pin -shared with general I/O pin. When used as general purpose I/O, can wake-up from sleep mode and idle mode while the status of the pin changes.
VA, VB	–	Connect the capacitors for LCD bias voltage
VLCD2	–	One of LCD bias voltage
VLCD3	–	One of LCD bias voltage
VDD	I	Power supply pin
GND	I	System ground pin
OTP Programming		
/RESET	I	VPP
P54	I	ACLK
P55	I	DINCLK
P56	I/O	DATAIN
P60	I	PGMB
P61	I	/OEB
VDD	I	VDD
GND	I	GND

8 Functional Description

8.1 Operational Registers

8.1.1 Bank 0 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

8.1.2 Bank 0 R1 (TCC)

Incremented by an external signal edge applied to TCC, or by the instruction cycle clock. Written and read by the program as any other register.

8.1.3 Bank 0 R2 (Program Counter)

The configuration structure generates 8K×13 on-chip ROM addresses to the relative programming instruction codes. The structure is depicted in Figure 3.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

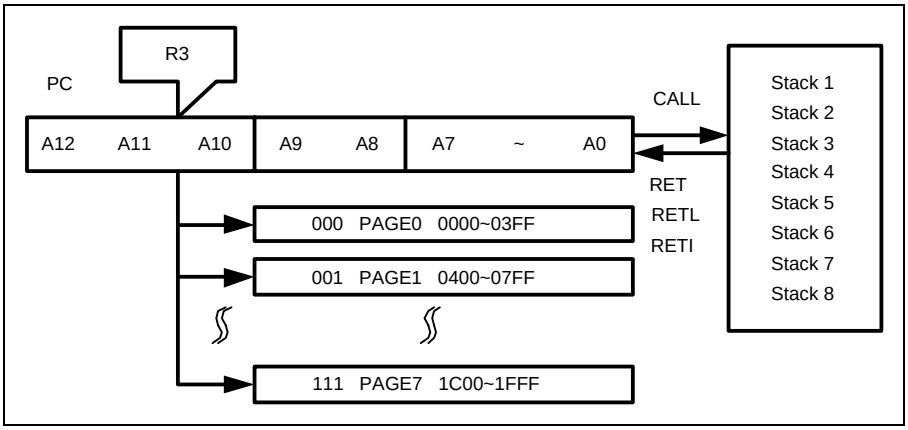
"CALL" instruction loads the low 10 bits of the PC and PC+1, then push onto the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2, A" allows the loading of an address from the A register to the PC, and contents of the ninth and tenth bits do not change.

"ADD R2, A" allows a relative address to be added to the current PC, and contents of the ninth and tenth bits do not change.

The most significant bits (A10~A12) will be loaded with the content of Bits PS0~PS2 in the status register (R3) upon execution of a "JMP", "CALL" instruction.



Address	R Bank 0 Register	R Bank 1 Register
00	R0 (Indirect Addressing Register)	
01	R1 (TCC)	
02	R2 (Program Counter)	
03	R3 (Status Register and RDM Page)	
04	R4 (RAM Select)	
05	R5 (Port 5, MSB of Data RAM and IOC Page	
06	R6 (Port 6)	−
07	R7 (Port 7)	−
08	R8 (Port 8)	−
09	R9 (LCD Control)	R9 (Port 9)
0A	RA (LCD Address)	RA (P6 Switch)
0B	RB (LCD Data Buffer)	−
0C	RC (CNTEN)	−
0D	RD (System Clock Control)	−
0E	RE (IR Control)	−
0F	RF (Interrupt Flag)	−

Address	Control Page 0 Register	Control Page 1 Register
00		
01		
02		
03		
04		
05	IOC5 (Port 5 I/O Control)	IOC5 (Port 9 I/O Control)
06	IOC6 (Port 6 I/O Control)	IOC6 (Wake-up Register)
07	IOC7 (Port 7 I/O Control)	IOC7 (TCC Control)
08	IOC8 (Port 8 I/O Control)	IOC8 (WDT Control)
09	IOC9 (RAM Address)	IOC9 (Counters 1, 2 Control)
0A	IOCA (RAM Data)	IOCA (High/Low Pulse Control)
0B	IOCB (Counter 1 Preset)	IOCB (Port 6 Pull high)
0C	IOCC (Counter 2 Preset)	IOCC (Port 6 Open drain)
0D	IOCD (High Pulse Timer Preset)	IOCD (Port 8 Pull high)
0E	IOCE (Low Pulse Timer Preset)	IOCE (Port 6 Pull low)
0F	IOCF (Interrupt Mask Flag)	−

Address	General Purpose Register
10	General Purpose Register 10
11	General Purpose Register 11
12	General Purpose Register 12
13	General Purpose Register 13
14	General Purpose Register 14
15	General Purpose Register 15
16	General Purpose Register 16
17	General Purpose Register 17
18	General Purpose Register 18
19	General Purpose Register 19
1A	General Purpose Register 1A
1B	General Purpose Register 1B
1C	General Purpose Register 1C
1D	General Purpose Register 1D
1E	General Purpose Register 1E
1F	General Purpose Register 1F

Addr	Bank 0	Bank 1	Bank 2	Bank 3
20	General Purpose Register 20	General Purpose Register 20	General Purpose Register 20	General Purpose Register 20
21	General Purpose Register 21	General Purpose Register 21	General Purpose Register 21	General Purpose Register 21
22	General Purpose Register 22	General Purpose Register 22	General Purpose Register 22	General Purpose Register 22
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
3E	General Purpose Register 3E	General Purpose Register 3E	General Purpose Register 3E	General Purpose Register 3E
3F	General Purpose Register 3F	General Purpose Register 3F	General Purpose Register 3F	General Purpose Register 3F

8.1.4 Bank 0 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS2	PS1	PS0	T	P	Z	DC	C

Bit 0 (C) Carry flag

Bit 1 (DC) Auxiliary carry flag

Bit 2 (Z) Zero flag

Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands or during power up and reset to 0 by WDT timeout.

Event	T	P	Remark
WDT wake-up from sleep mode	0	0	–
WDT time out (not sleep mode)	0	1	–
/RESET wake-up from sleep	1	0	–
Power up	1	1	–
Low pulse on /RESET	×	×	×: don't care

Bit 5 ~ Bit 7 (PS0 ~ PS2) Page select bits

Page Select Bits

PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	Page 0
0	0	1	Page 1
0	1	0	Page 2
0	1	1	Page 3
1	0	0	Page 4
1	0	1	Page 5
1	1	0	Page 6
1	1	1	Page 7

User can use the Page instruction to change page or to maintain user's program page. Otherwise, user can use far jump (FJMP) or far call (FCALL) MACRO instructions to program user's code. The program page is maintained by EMC's compiler. It will change user's program by inserting instructions within the program.

8.1.5 Bank 0 R4 (RAM Select Register)

Bits 0 ~ 5 are used to select up to 64 registers in indirect addressing mode.

Bits 6 ~ 7 determine which bank is activated among the 4 banks.

User can use the Bank instruction to change banks.

8.1.6 Bank 0 R5 (Program Page Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	0	0	RAM_A8	IOCPAGE

Bit 0 (IOCPAGE): change IOC6 ~ IOCF to another page

0 : Page 0
1 : Page 1

Bit 1 (RAM_A8): MSB of Data RAM

Bits 2, 3: reserved, fixed to "0"

Bits 4~7: 4-bit I/O registers of Port 5

8.1.7 R6 (Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R67	R66	R65	R64	R63	R62	R61	R60

Bits 0~7: 8-bit I/O registers of Port 6

8.1.8 R7 (Port 7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R77	R76	R75	R74	R73	R72	R71	R70

Bit 0~7: 8-bit I/O registers of Port 7

8.1.9 R8 (Port 8)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R87	R86	R85	R84	R83	R82	R81	R80

Bit 0~7: 8-bit I/O registers of Port 8

8.1.10 Bank 0 R9 (LCD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCD_BS	DS1	DS0	LCDEN	-	LCDTYPE	LCDF1	LCDF0

Bits 1, 0: LCD clock prescaler ratio control bits

LCDF1	LCDF0	LCD frame frequency (Fs=32.768kHz)		
		1/2 Duty	1/3 Duty	1/4 Duty
0	0	Fs/(256*2)=64.0	Fs/(172*3)=63.5	Fs/(128*4) =64.0
0	1	Fs/(280*2)=58.5	Fs/(188*3)=58.0	Fs/(140*4) =58.5
1	0	Fs/(304*2)=53.9	Fs/(204*3)=53.5	Fs/(152*4) =53.9
1	1	Fs/(232*2)=70.6	Fs/(156*3)=70.0	Fs/(116*4) =70.6

Fs: sub-oscillator frequency

Bit 2: LCD drive waveform type select bit

0: A type waveform

1: B type waveform

Bit 3: Reserved, fixed to "0"

Bit 4: LCD enable bit:

0 : LCD circuit disabled

1 : LCD circuit enabled

When LCD is disabled, all common/segment outputs are set to ground (GND) level

Bits 6, 5 (DS1, 0): LCD duty select

8.1.11 LCD Duty Select

DS1	DS0	LCD Duty
0	0	1/2 duty
0	1	1/3 duty
1	×	1/4 duty

Bit 7 (LCD_BS): bias select

0 : 1/2 bias

1 : 1/3 bias

8.1.12 Bank 1 R9 (Port 9)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	P94	P93	P92	P91	P90

Bits 0~4: 8-bit I/O registers of Port 9

8.1.13 Bank 0 RA (LCD Contrast and Address Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	LCD_A5	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0

Bit 5~Bit 0: LCD RAM address

RA (LCD Address)	RB (LCD Data Buffer)								Segment
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3 (LCD_D3)	Bit 2 (LCD_D2)	Bit 1 (LCD_D1)	Bit 0 (LCD_D0)	
00H	0	0	0	0					**SEG0**
01H	0	0	0	0					**SEG1**
02H	0	0	0	0					**SEG2**
|					|				**|**
1DH	0	0	0	0					**SEG29**
1EH	0	0	0	0					**SEG30**
1FH	0	0	0	0					**SEG31**
20H	0	0	0	0					**SEG32**
21H	0	0	0	0					**SEG33**
22H	0	0	0	0					**SEG34**
23H	0	0	0	0					**SEG35**
24H	0	0	0	0					**SEG36**
25H	0	0	0	0					**SEG37**
26H	0	0	0	0					**SEG38**
27H	0	0	0	0					**SEG39**
Common	**X**	**X**	**X**	**X**	**COM3**	**COM2**	**COM1**	**COM0**	

Bit 7 ~ Bit 6: Reserved, fixed to "0"

8.1.14 Bank 1 RA (Port 6 Switch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P6SH	P6SL

Bit 0 (P6SL): This bit can control the Port 6 low nibble whether SEG output or normal I/O.

0 = low nibble of Port 6 are normal I/O

1 = low nibble of Port 6 are SEG output

Bit 1 (P6SH): This bit can control the Port 6 high nibble whether SEG output or normal I/O.

0 = the high nibble of Port 6 are normal I/O.

1 = the high nibble of Port 6 are SEG output.

Bits 2~3, 4~7: Unused

8.1.15 Bank 0 RB (LCD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	LCD_D 3	LCD_D 2	LCD_D 1	LCD_D 0

Bit 7 ~ Bit 4: Reserved, fixed to “0”

Bits 0~3: LCD RAM data transfer register

8.1.16 Bank 0 RC (CNTEN)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	LPWTEN	HPWTEN	CNT2EN	CNT1EN

Bit 0 (CNT1EN): Counter 1 enable bit

0 : disable

1 : enable

Bit 1(CNT2EN): Counter 2 enable bit

0 : disable

1 : enable

Bit 2(HPWTEN): high pulse width timer enable bit

0 : disable

1 : enable

Bit 3(LPWTEN): low pulse width timer enable bit

0 : disable

1 : enable

Bits 4~7 (Unused)

8.1.17 Bank 0 RD (System Clock Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS

Bit 0: CPU oscillator source select

0 : sub-oscillator (fs)

1 : main oscillator (fosc)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bits 1, 2: LCD booster frequency select bit

BF1	BF0	Booster Frequency
0	0	Fs
0	1	Fs/4
1	0	Fs/8
1	1	Fs/16

Bit 3: Idle mode enable bit. This bit will determine SLEP instruction which mode to go.

IDLE="0"+SLEP instruction → sleep mode

IDLE="1"+SLEP instruction → idle mode

Bit 6~Bit 4: main clock select bit for PLL mode (code option select)

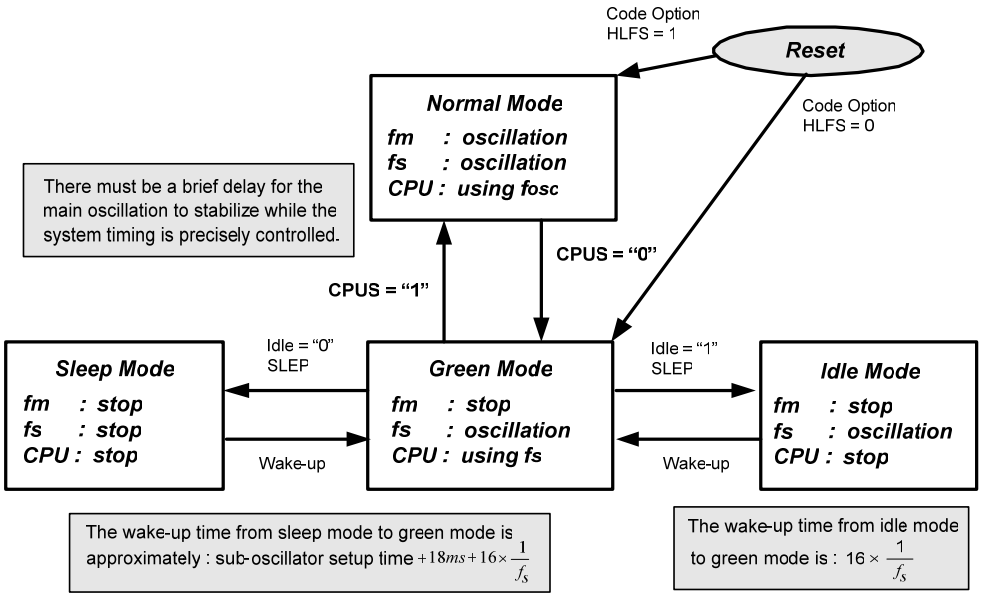
CLK2	CLK1	CLK0	Main Clock	Remark
0	0	0	32.768K×130=4.26 MHz	PLL frequency
0	0	1	32.768K×65=2.13 MHz	PLL frequency
0	1	0	2.13MHz/2	–
0	1	1	2.13MHz/4	–
1	0	0	32.768K×244=8 MHz	PLL frequency
1	0	1		
1	1	0		
1	1	1		

Bit 7: reserved, fixed to "0"

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows:

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
TCC time out IOCF Bit 0=1	×	Wake-up (controlled by CONT Bit 1) + interrupt + next instruction	Interrupt	Interrupt
INT0 pin IOCF Bit 1=1	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
INT1 pin IOCF Bit 2=1	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Counter 1 IOCF Bit 3=1	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Counter 2 IOCF Bit 4=1	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
High-pulse timer IOCF Bit 5=1	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Low-pulse timer IOCF Bit 6=1	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Port 6, Port 8	IOCF Bit 7=0 Wake-up + next instruction IOCF Bit 7=1 Wake-up + interrupt + next instruction	IOCF Bit 7=0 Wake-up + next instruction IOCF Bit 7=1 Wake-up + interrupt + next instruction	×	×
WDT time out	×	RESET	RESET	RESET

8.2 CPU Operation Mode



8.2.1 Bank 0 RE (IR Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRE	HF	LGP	-	IROUTE	TCCE	EINT1	EINT0

Bit 0 (EINT0): Control bit used to define the function of P54 (INT0) pin.

0 : P54, bidirectional I/O pin

1 : INT0, external interrupt pin. In this case, the I/O control bit of P54 (Bit 4 of IOC5) must be set to "1".

Bit 1 (EINT1): Control bit used to define the function of P55 (INT1) pin.

0 : P55, bidirectional I/O pin

1 : INT1, external interrupt pin. In this case, the I/O control bit of P55 (Bit 5 of IOC5) must be set to "1".

Bit 2 (TCCE): Control bit used to define the function of P56 (TCC) pin.

0 : P56, bidirectional I/O pin

1 : TCC, external input pin of TCC. In this case, the I/O control bit of P56 (Bit 6 of IOC5) must be set to "1"

Bit 3 (IROUTE): Control bit used to define the function of P57 (IROUT) pin.

0 : P57, bidirectional I/O pin

1 : IROUT, In this case, the I/O control bit of P57 (Bit 7 of IOC5) must be set to "0".

Bit 4: Reserved, fixed to “0”

Bit 5 (LGP): Long pulse

0 : The high-pulse timer register and low-pulse width timer is valid.

1 : The high-pulse width timer register is ignored. So the IROUT waveform only depends on the low-pulse width timer register.

Bit 6 (HF): High frequency

0 : For PWM application, the IROUT waveform according to high-pulse and low-pulse width timers determine the high pulse and low pulse width time.

1 : For IR application mode, the low time parts of the generated pulse is modulated with a frequency Fcarrier.

Bit 7 (IRE): Infrared Remote Enable bit

0 : Disable IRE. Disable H/W Modulator Function. The IROUT pin is fixed to high level.

1 : Enable IRE. Enable H/W Modulator Function. Pin 57 is defined as IROUT.

8.2.2 Bank 0 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIF	LPWTF	HPWTF	CNT2F	CNT1F	INT1F	INT0F	TCIF

Bit 0 (TCIF): TCC timer overflow interrupt flag. Set when TCC timer overflows.

Bit 1 (INT0F): External INT0 pin interrupt flag.

Bit 2 (INT1F): External INT1 pin interrupt flag.

Bit 3 (CNT1): Internal Counter 1 underflow interrupt flag.

Bit 4 (CNT2): Internal Counter 2 underflow interrupt flag.

Bit 5 (HPWTF): Internal high-pulse width timer underflow interrupt flag.

Bit 6 (LPWTF): Internal low-pulse width timer underflow interrupt flag.

Bit 7 (ICIF): Port 6, Port 8, input status changed interrupt flag. Set when Port 6, Port 8 input changes.

8.3 General Purpose Register

R10~R1F and R20~R3F (Banks 0~3) are general purpose registers.

8.4 Special Purpose Registers

8.4.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

8.4.2 CONT Register (Bank Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	EN16	TCS	-	TCCWAKE	BANKM

Bit 0 (BANKM):

0 : Users always read R Bank 0 register only even if Bits 6~7 values of R4 is changing.

1 : R Bank register will be effected while Bits 6~7 value of R4 is changing.

Bit 1 (TCCWAKE):

0 : MCU will not wake-up from idle mode to green/normal mode while TCC overflows and is interrupted.

1 : MCU will wake-up from idle mode to green/normal mode while TCC overflows and is interrupted.

Bit 3 (TCS): TCC clock source

0 : TCC clock source will be external clock from Port 56 (TCC pin, Set Port 56 as external clock input)

1 : TCC clock source will be internal clock (32kHz)

Bit 4 (EN16): Determine whether Timer 1 or Timer 2 will be combined to one 16-bit timer or two 8-bit timers independently.

0 : Timer 1 and Timer 2 are independent (default)

1 : Timer 1 and Timer 2 are cascaded to one 16-bit timer.

Bits 2, 5~7: Un-used bits

8.4.3 IOC Page 0 IOC5 (Port 5 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS

Bit 0 (P7LS): Switch low nibble I/O of Port 7 or LCD segment output for shared pins SEGxx/P7.x pins

0 : select normal P7.0~P7.3 for low nibble of Port 7

1 : select SEG16~SEG19 output for LCD Segment output

Bit 1(P7HS): switch high nibble I/O of port7 or LCD segment output for share pins SEGxx/P7.x pins

0 : Select normal P7.4~P7.7 for high nibble of Port 7

1 : Select SEG20~SEG23 output for LCD Segment output

Bit 2(P8LS): switch low nibble I/O of port8 or LCD segment output for share pins SEGxx/P8.x pins

0 : Select normal P8.0~P8.3 for low nibble of Port 8

1 : Select SEG24~SEG27 output for LCD Segment output

Bit 3(P8HS): switch low high I/O of port8 or LCD segment output for share pins SEGxx/P8.x pins

0 : Select normal P8.4~P8.7 for high nibble of Port 8

1 : Select SEG28~SEG31 output for LCD Segment output

Bit 4 (IOC54)~Bit 7(IOC57): Port 5 I/O direction control register

0 : sets the relative I/O pins as output

1 : puts the relative I/O pin into high impedance

8.4.4 IOC Page1 IOC5 (Port9 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	IOC94	IOC93	IOC92	IOC91	IOC90

Bit 0 (IOC90)~Bit 7(IOC97): Port 9 I/O direction control register

0 : sets the relative I/O pins as output

1 : puts the relative I/O pins into high impedance

8.4.5 IOC Page 0 IOC6 (Port 6 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60

Bit 0 (IOC60)~Bit 7 (IOC67): Port 6 I/O direction control register

0 : sets the relative I/O pins as output

1 : puts the relative I/O pin into high impedance

8.4.6 IOC Page1 IOC6 (Wake-up Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IROCS	-	-	-	/WUE8H	/WUE8L	/WUE6H	/WUE6L

Bit 7: IROCS: IROUT/Port 5.7 output driver current set

IROUT = **0 :** 14 mA

IROUT = **1 :** 28 mA

Bits 6, 5, 4: Reserve

Bit 3: /WUE8H=0/1: enable/disable P8.4~P8.7 pin change wake-up function

Bit 2: /WUE8L=0/1: enable/disable P8.0~P8.3 pin change wake-up function

Bit 1: /WUE8H=0/1: enable/disable P6.4~P6.7 pin change wake-up function

Bit 0: /WUE8L=0/1: enable/disable P6.0~P6.3 pin change wake-up function

8.4.7 IOC Page 0 IOC7 (Port 7 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

Bit 0 ~ Bit 7 (IOC70 ~ IOC77): Port 7 I/O direction control register

0 : sets the relative I/O pins as output

1 : puts the relative I/O pin into high impedance

8.4.8 IOC Page 1 IOC7 (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0

Bit 0 (TCCP0) ~ Bit 2 (TCCP2) TCC prescaler bits

TCCP2	TCCP1	TCCP0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3: Prescaler Register enable bit

0 : TCC rate 1:1

1 : depends on the table

Bit 4 (TE): TCC signal edge

0 : increment by TCC pin rising edge

1 : increment by TCC pin falling edge

Bit 5 (TS): TCC signal source

0 : Internal instruction cycle clock (clock source is equal to Fosc/2)

1 : Transition on TCC pin, TCC period > internal instruction clock period.

Bit 6 (INT): INT enable flag, this bit is read only

0 : interrupt masked by DISI or hardware interrupt

1 : interrupt enabled by ENI/RETI instructions

Bit 7: INT_EDGE

0 : P54 's (INT0) interrupt source is a rising edge signal.

1 : P54 's (INT0) interrupt source is a falling edge signal.

8.4.9 IOC Page 0 IOC8 (Port 8 I/O control register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80

Bit 0 ~ Bit 7(IOC80 ~ IOC87): Port 8 I/O direction control register

0 : sets the relative I/O pins as output

1 : puts the relative I/O pin into high impedance

8.4.10 IOC Page 1 IOC8 (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	WDTE	WDTP2	WDTP1	WDTP0

Bit 0 (WDTP0) ~ Bit 2 (WDTP2) watchdog timer prescaler bits.

WDTP2	WDTP1	WDTP0	WDT Rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

Bit 3 (WDTE): Watchdog Timer Enable, control bit used to enable the Watchdog timer

0 : disable

1 : enable

Bit 4 ~ Bit 7: reserved, fixed to "0"

8.4.11 IOC Page 0 IOC9 (256 Byte RAM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0

Bits 0~7: 256 byte RAM address

8.4.12 IOC Page1 IOC9 (Counters 1, 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0

Bit 0 ~ Bit 2 (C1P0 ~ C1P2): Counter 1 scale

CNT1P2	CNT1P1	CNT1P0	Counter 1 Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S): Counter 1 clock source select

0 : Fs ; Fs: sub-oscillator clock

1 : Fw ; Fw: Internal instruction cycle clock, (ex. two system clocks, clock source is equal to Fosc/2)

Bit 4 ~ Bit 6 (C2P0 ~ C2P2): Counter 1 scale

CNT2P2	CNT2P1	CNT1P0	Counter 2 Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7(CNT2S): Counter 1 clock source select

0 : Fs ; Fs: sub-oscillator clock

1 : Fw ; Fw: Internal instruction cycle clock, (ex. two system clocks, clock source equal to Fosc/2)

8.4.13 IOC Page 0 IOCA (256 Byte RAM Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0

Bits 0~7: 256 byte RAM data transfer register

8.4.14 IOC Page 1 IOCA (High-pulse Width Timer, Low-pulse Width Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0

Bit 0 ~ Bit 2 (HPWP0 ~ HPWP2): high-pulse width timer scale

HPWTP2	HPWTP1	HPWTP0	High-pulse Width Timer Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (HPWTS): high-pulse width timer clock source select

0 : Fs ; Fs: sub-oscillator clock

1 : Fw ; Fw: Internal instruction cycle clock, (ex. two system clocks, clock source equal to Fosc/2)

Bit 4 ~ Bit 6 (LPWTP0 ~ LPWTP2): low-pulse width timer scale

LPWTP2	LPWTP1	LPWTP0	Low-pulse Width Timer Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7(LPWTS): low-pulse width timer clock source select

0 : Fs ; Fs: sub-oscillator clock

1 : Fw ; Fw: Internal instruction cycle clock, (ex. two clocks system, clock source equal to Fosc/2)

8.4.15 IOC Page 0 IOCB (Counter 1 Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT17	CNT16	CNT15	CNT14	CNT13	CNT12	CNT11	CNT10

Bit 0 ~ Bit 7: all are Counter 1 buffer that user can read and write. Counter 1 is an 8-bit down-counter with 8-bit prescaler that can use IOCB to preset and read the counter. After an interrupt (write=preset), it will auto reload the preset value.

8.4.16 IOC Page 1 IOCB (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60

Bit 0 ~ Bit 7 are Port 6 pull-high control register

0 : disable internal pull-high resistor function

1 : enable internal pull-high resistor function

8.4.17 IOC Page 0 IOCC (Counter 2 Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT27	CNT26	CNT25	CNT24	CNT23	CNT22	CNT21	CNT20

Bit 0 ~ Bit 7: all are Counter 2 buffer that user can read and write. Counter 2 is an 8-bit down-counter with 8-bit prescaler that can use IOCC to preset and read the counter. After an interrupt (write=preset), it will reload the preset value.

When IR output is enabled, setting this control register can obtain carrier frequency output.

If Counter 2 clock source is equal to FT Carrier frequency (Fcarrier) = FT/(preset value+1)

8.4.18 IOC Page 1 IOCC (Port 6 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60

Bit 0 ~ Bit 7 are Port 6 open drain control register

0 : disable open drain function

1 : enable open drain function

8.4.19 IOC Page 0 IOCD (High-pulse Width Timer Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HPWC7	HPWC6	HPWC5	HPWC4	HPWC3	HPWC2	HPWC1	HPWC0

Bit 0 ~ Bit 7: all are high-pulse width timer buffer that user can read and write.

High-pulse width timer preset register is an 8-bit down-counter with 8-bit prescaler that can use IOCD to preset and read the counter. After an interrupt (write=preset), it will reload the preset value.

For PWM or IR application, this control register is set to high pulse width.

If high-pulse width source clock is FT, the high pulse width = (high-pulse width preset value+1)/ FT

8.4.20 IOC Page1 IOCD (Port 8 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80

Bit 0 ~ Bit 7 are Port 8 pull-control register

0 : Disable internal pull-high resistor function

1 : Enable pull-high resistor function

8.4.21 IOC Page 0 IOCE (Low-pulse Width Timer Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPWC7	LPWC6	LPWC5	LPWC4	LPWC3	LPWC2	LPWC1	LPWC0

Bit 0 ~ Bit 7: all are low-pulse width timer buffer that user can read and write.

Low-pulse width timer preset is an 8-bit down-counter with 8-bit prescaler that can use IOCE to preset and read the counter. After an interrupt (write=preset), it will reload the preset value.

For PWM or IR application, this control register is set to low pulse width.

If low-pulse width timer source clock is FT, the low pulse width = (preset value+1)/ FT

8.4.22 IOC Page 1 IOCE (Port 6 Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60

Bit 0 ~ Bit 7 are Port 6 pull-high control register

0 : Disable internal pull-down resistor function

1 : Enable internal pull-down resistor function

8.4.23 IOC Page 0 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE

Bit 0~Bit 7: Interrupt enable bit

0 : Disable interrupt

1 : Enable interrupt

The IOCF0 register is readable and writable.

8.4.24 IOC Page 1 IOCF (Unused)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	-

Bits 0~7: Reserved, fixed to “0”

8.5 TCC/WDT Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The TCCP0~ TCCP2 bits of the IOC7 Page 1 register are used to determine the ratio of the TCC prescaler. Likewise, the WDTP0~ WDTP2 bits of the IOC8 Page 1 register are used to determine the WDT prescaler. The prescaler (TCCP0~ TCCP2) will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the “WDTC” and “SLEP” instructions. Figure 8-1 depicts the circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer/counter. The TCC clock source can be internal clock or external signal input (edge selectable from the TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). As illustrated in Figure 8-1, selection of CLK=Fosc/2 or CLK=Fosc/4 depends on the Code Option bit <CLKS>. CLK=Fosc/2 is selected if the CLKS bit is "0", and CLK=Fosc/4 is selected if the CLKS bit is "1". If TCC signal source is from an external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to WDTE bit of IOC8 Page 1 register. With no prescaler, the WDT time-out period is approximately 18 ms.

NOTE

VDD=5V, Setup time period=16.5ms ± 5%.

VDD=3V, Setup time period=18ms ± 5%.

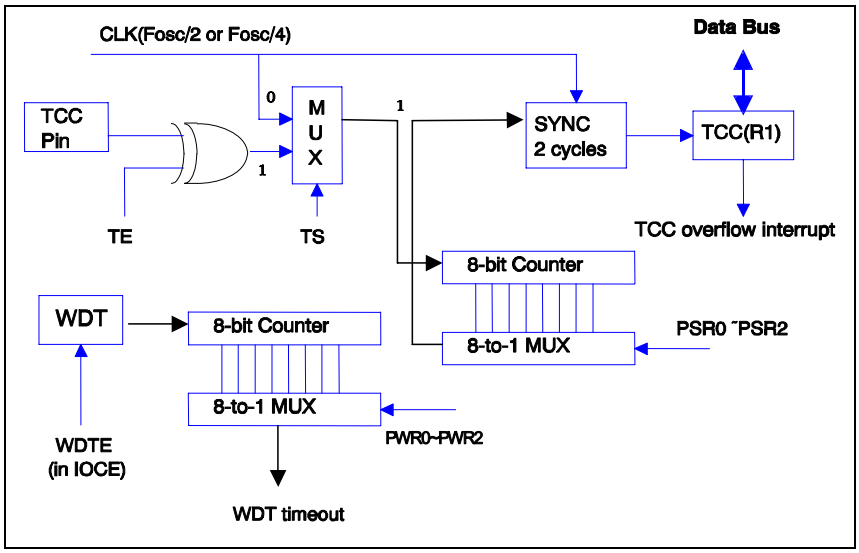
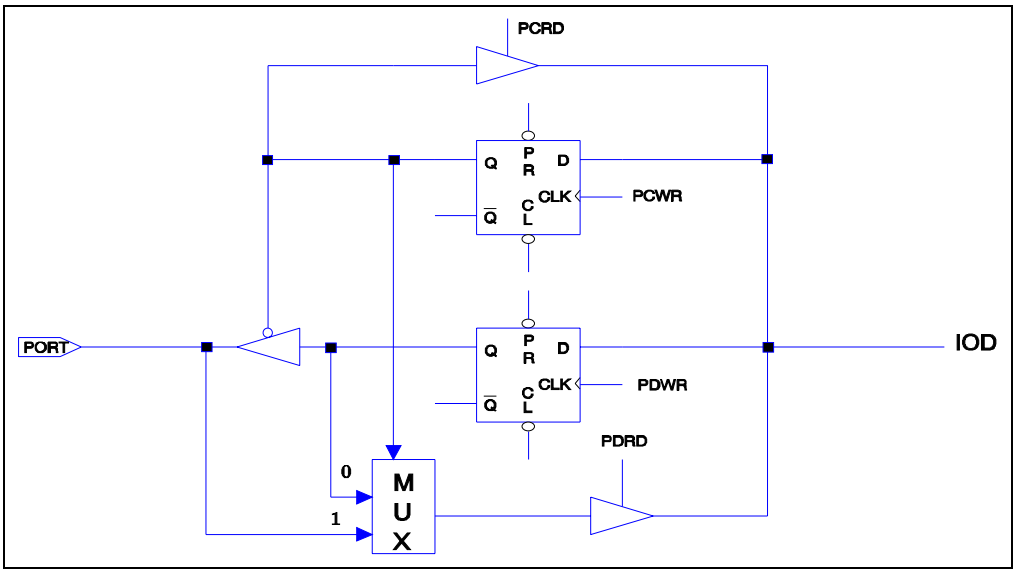


Figure 8-1 TCC and WDT

8.6 I/O Ports

The I/O registers, (Port 5, Port 6, Port 7 and Port 8), are bi-directional tri-state I/O ports. Port 6 and Port 8 are pulled-high internally by software. Port 6 is pulled-down internally by software. Likewise, Port 6 has its open-drain output also through software. Port 5, Port 6 and Port 8 features an input status changed interrupt (or wake-up) function and is pulled-high by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8). The I/O registers and I/O control registers are both readable and writable.



Note: Open-drain is not shown in the figure.

Figure 8-2 Circuit of I/O port and I/O Control Register for Port 5 ~ Port 9

8.7 Reset and Wake-up

The reset can be caused by:

1. Power-on reset
2. WDT timeout (If enabled)
3. /RESET pin connect low
4. Low voltage reset

NOTE

The power-on reset circuit is always enabled, it will reset the CPU at 2.0±0.2V and consumed about 0.5μA.

Once a reset occurs, the following functions are performed

1. The oscillator is running, or will be started.
2. The Program Counter (R2) is set to all "0".
3. All I/O port pins are configured as input mode (high-impedance state).
4. The TCC/Watchdog timer and prescaler are cleared.
5. When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
6. The bits of the IOC7 Page 1 register are set to all "1" except for the Bit 6 (INT flag).

Registers initial values after Power-on reset

Address	Name (Bank / IOC)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Bank 0, R0	R0.7	R0.6	R0.5	R0.4	R0.3	R0.2	R0.1	R0.0
		R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
01	Bank 0, TCC	TCC.7	TCC.6	TCC.5	TCC.4	TCC.3	TCC.2	TCC.1	TCC.0
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
02	Bank 0, PC	PC.7	PC.6	PC.5	PC.4	PC.3	PC.2	PC.1	PC.0
		R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
03	Bank 0, Status	PS2	PS1	PS0	T	P	Z	DC	C
		R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-U	R/W-U	R/W-U
04	Bank 0, R4	RSB1	RSB0	RS5	RS4	RS3	RS2	RS1	RS0
		R/W-0	R/W-0	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
05	Bank 0, Port 5	P57	P56	P55	P54	-	-	RAM_A8	IOCPAGE
		R/W-U	R/W-U	R/W-U	R/W-U	R-0	R-0	R/W-0	R/W-0
06	Bank 0, Port 6	P67	P66	P65	P64	P63	P62	P61	P60
		R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
07	Bank 0, Port 7	P77	P76	P75	P74	P73	P72	P71	P70
		R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
08	Bank 0, Port 8	P87	P86	P85	P84	P83	P82	P81	P80
		R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
09	Bank 0, LCD control	BS	DS1	DS0	LCDEN	-	LCDTYPE	LCDF1	LCDF0
		R/W-0	R/W-0	R/W-1	R/W-0	R-0	R/W-0	R/W-0	R/W-0
09	Bank 1, Port 9	-	-	-	P94	P93	P92	P91	P90
		R-0	R-0	R-0	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
0A	Bank 0, LCD address	-	-	LCD_A5	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0
		R-0	R-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0A	Bank 1, P6 switch, Data RAM address	-	-	-	-	-	-	P6SH	P6SL
		R-0	R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0
0B	Bank 0, LCD data	-	-	-	-	LCD_D3	LCD_D2	LCD_D1	LCD_D0
		R-0	R-0	R-0	R-0	R/W-U	R/W-U	R/W-U	R/W-U
0C	Bank 0, CNTEN	-	-	-	-	LPWTEN	HPWTEN	CNT2EN	CNT1EN
		R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
0D	Bank 0, CLK control	-	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS
		R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0E	Bank 0, IR control	IRE	HF	LGP	-	IROUTE	TCCE	EINT1	EINT0
		R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
0F	Bank 0, Interrupt flag	ICIF	LPWTF	HPWTF	CNT2F	CNT1F	INT1F	INT0F	TCIF
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
05	IOC Page 0, Port 5 control	IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS
		R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
05	IOC Page 1, Port 9 control	-	-	-	IOC94	IOC93	IOC92	IOC91	IOC90
		R-0	R-0	R-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
06	IOC Page 0, Port 6 control	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
06	IOC Page 1, wake up control	IROCS	-	-	-	/WUE8H	/WUE8L	/WUE6H	/WUE6L
		R/W-0	R-0	R-0	R-0	R/W-1	R/W-1	R/W-1	R/W-1

Address	Name (Bank / IOC)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07	IOC Page 0, Port 7 control	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
07	IOC Page 1, TCC control	INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0
		R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
08	IOC Page 0, Port 8 control	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
08	IOC Page 1, WDT control	-	-	-	-	WDTE	WDTP2	WDTP1	WDTP0
		R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
09	IOC Page 0, Data RAM address	RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
09	IOC Page 1, CNT1/2 control	CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0A	IOC Page 0, Data RAM data	RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
		R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
0A	IOC Page 1, L/H pulse control	LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0B	IOC Page 0, CNT1 preset	CNT17	CNT16	CNT15	CNT14	CNT13	CNT12	CNT11	CNT10
		R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
0B	IOC Page 1, Port 6 pull high	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0C	IOC Page 0, CNT2 preset	CNT27	CNT26	CNT25	CNT24	CNT23	CNT22	CNT21	CNT20
		R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
0C	IOC Page 1, Port 6 open-drain	OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0D	IOC Page 0, High pulse width timer	HPWC7	HPWC6	HPWC5	HPWC4	HPWC3	HPWC2	HPWC1	HPWC0
		R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
0D	IOC Page 1, Port 8 pull high	PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0E	IOC Page 0, Low pulse width timer	LPWC7	LPWC6	LPWC5	LPWC4	LPWC3	LPWC2	LPWC1	LPWC0
		R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
0E	IOC Page 1, Port6 pull low	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0F	IOC Page 0, interrupt mask flag	ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0F	IOC Page 1, interrupt mask flag	-	-	-	-	-	-	-	-
		R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
-	CONT register	-	-	-	EN16	TCS	-	TCCWAKE	BANKM
		R-0	R-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

X: not used. **U:** unknown or don't care. **P:** previous value before reset **R:** Read-able W: Write-able

8.8 Oscillator

8.8.1 Oscillator Modes

The EM78R469 can be operated in the three different oscillator modes for main oscillator (R-OSCI, OSCO), such as RC oscillator with external resistor and Internal capacitor mode (IC), crystal oscillator mode and PLL operation mode. User can select one of the three modes by programming FMMD1 and FMMD0 in the Code Option register, the sub-oscillator can be operated in crystal mode and ERIC mode. Table 8-1 show these three modes are defined.

Table 8-1 Oscillator Modes defined by FSMD, FMMD1, FMMD0

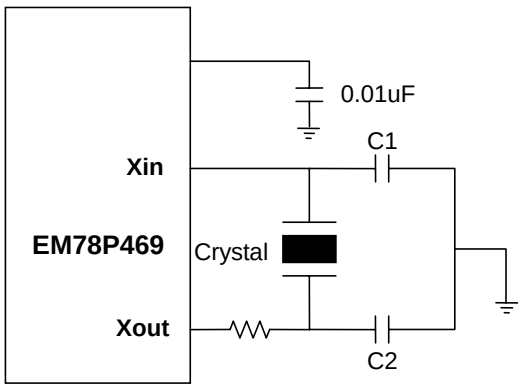
FSMD	FMMD1	FMMD0	Main Clock	Sub-clock
0	0	0	RC type (ERIC)	RC type (ERIC)
0	0	1	Crystal type	RC type (ERIC)
0	1	0	PLL type	RC type (ERIC)
0	1	1	PLL type	RC type (ERIC)
1	0	0	RC type (ERIC)	Crystal type
1	0	1	Crystal type	Crystal type
1	1	0	PLL type	Crystal type
1	1	1	PLL type	Crystal type

Table 8-2 Summary of maximum operating speeds

Conditions	VDD	Fxt Max (MHz)
Two clocks	2.3	4
	3.0	8
	5.0	10

8.8.2 Phase Lock Loop (PLL Mode)

When operating in PLL mode, High frequency is determined by the sub-oscillator. Bank 1 RD register can be chosen to change to high oscillator frequency. The relation between high frequency (Fm) and the sub-oscillator is shown in the below table:

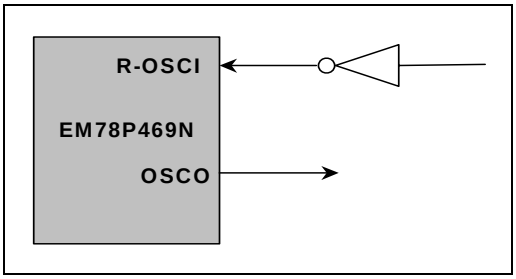


Bits 6~4 (CLK2~0) of RD: main clock selection bits for PLL mode (code option select)

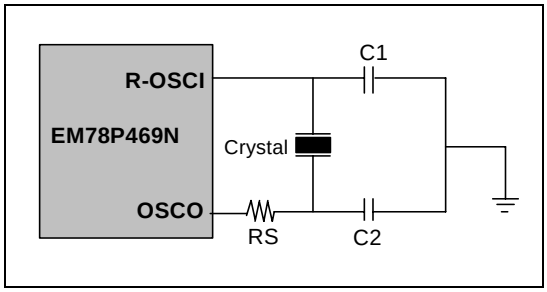
CLK2	CLK1	CLK0	Main Clock	Example Fs=32.768kHz
0	0	0	Fs × 130	4.26 MHz
0	0	1	Fs × 65	2.13 MHz
0	1	0	Fs × 65/2	1.065 MHz
0	1	1	Fs × 65/4	532kHz
1	×	×	Fs × 244	8 MHz

8.8.3 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78R469 can be driven by an external clock signal through the R-OSCI pin as shown below.



In most applications, pin R-OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 8-3 (Circuit for Crystal/Resonator) depicts such circuit. Table 8-3 (Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators) provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. A serial resistor, RS, may be necessary for the AT strip cut crystal or low frequency mode.



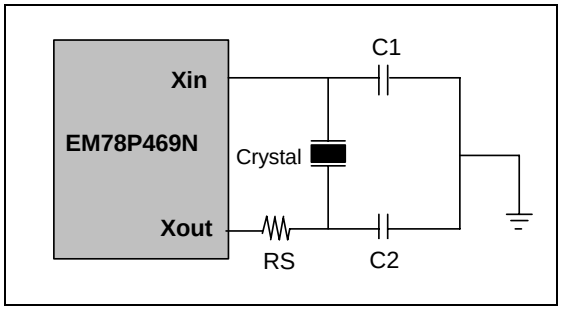


Figure 8-3 Circuit for Crystal/Resonator

Table 8-3 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

Oscillator Source	Oscillator Type	Frequency	C1 (pF)	C2 (pF)
Main oscillator	Ceramic Resonators	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
		10.0 MHz	10~30	10~30
	Crystal Oscillator	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15
		10.0 MHz	15	15
Sub-oscillator	Crystal Oscillator	32.768kHz	25	25

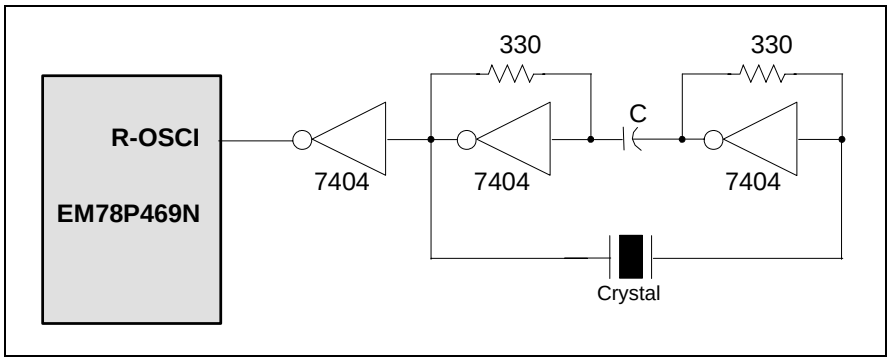


Figure 8-4 Circuit for Crystal/Resonator-Series Mode

8.8.4 RC Oscillator Mode with Internal Capacitor

If both precision and cost are taken into consideration, the EM78R469 also offers a special oscillation mode, which is equipped with an internal capacitor and an external resistor connected to Vcc. The internal capacitor functions as temperature compensator. In order to obtain more accurate frequency, a precise resistor is recommended.

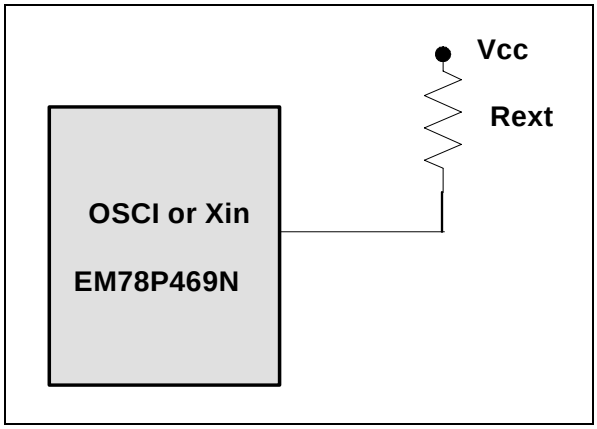


Figure 8-5 Circuit for Internal C Oscillator Mode

Table 8-4 R Oscillator Frequencies

Pin	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
R-OSCI	51K	2.2221 MHz	2.1972 MHz
	100K	1.1345 MHz	1.1203 MHz
	300K	381.36kHz	374.77kHz
Xin	2.2M	32.768kHz	32.768kHz

Note: Measured from QFP packages.

Values are provided for design reference only.

8.9 Power-on Considerations

Any microcontroller is not warranted to start proper operation before the power supply stabilizes in a steady state.

EM78R469 is equipped with Power-on Reset (POR) with detection level range as following table. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises quickly enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

POR table:

Parameters	Sym.	Min.	Typ.	Max.	Unit	Conditions
VH (release level)	VT+	2.0	2.2	2.4	V	
VL (reset level)	VT-	1.8	2.0	2.2	V	

8.9.1 External Power-on Reset Circuit

The circuit shown in Figure 8-6 (External Power-on Reset Circuit) implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time. Because the current leakage from the /RESET pin is about ± 5 μA, it is recommended that R should not be greater than 40K. In this way, the voltage at Pin /RESET is held below 0.2V. The diode (D) acts as a short circuit at power-down. The capacitor, C, is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

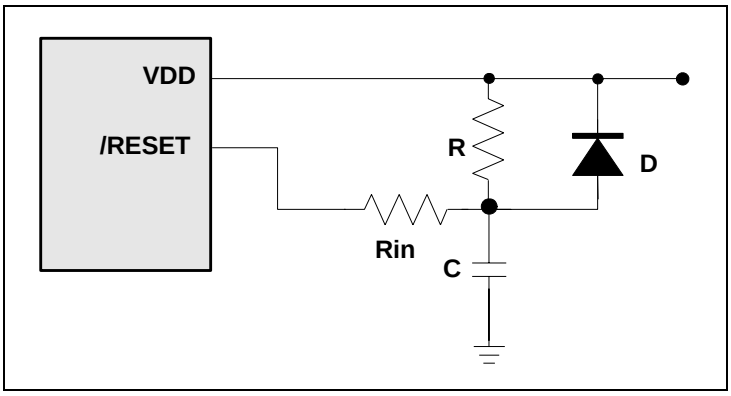


Figure 8-6 External Power on Reset Circuit

8.9.2 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 8-7 (Circuit 1 for the Residue Voltage Protection) and Figure 8-8 (Circuit 2 for the Residue Voltage Protection) show how to build residue-voltage protection circuits.

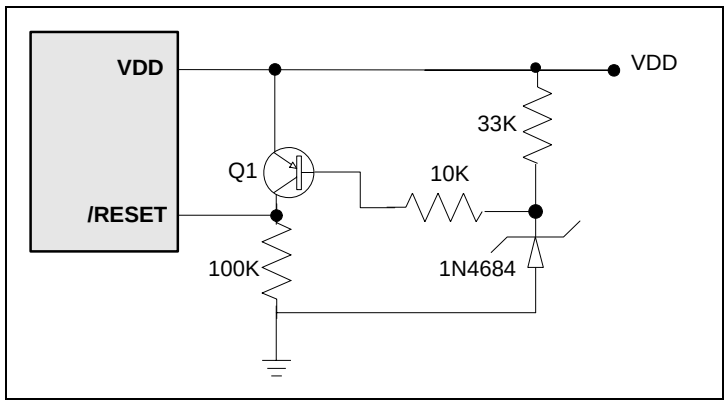


Figure 8-7 Circuit 1 for the Residue Voltage Protection

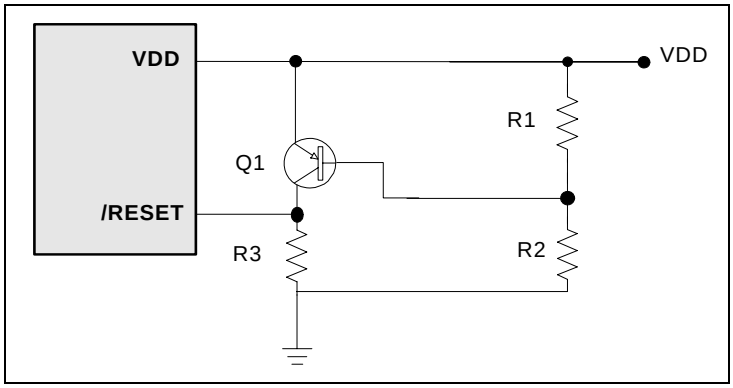


Figure 8-8 Circuit 2 for the Residue Voltage Protection

8.10 Interrupt

The EM78P469 has eight interrupt sources as listed below:

1. TCC overflow interrupt
2. External interrupt P5.3/INT0 pin
3. External interrupt P5.4/INT1 pin
4. Counter 1 underflow interrupt
5. Counter 2 underflow interrupt
6. High-pulse width timer underflow interrupt
7. Low-pulse width timer underflow interrupt
8. Port 6, Port 9 input status change wake-up

This IC has internal interrupts which are falling edge triggered, namely; TCC timer overflow interrupt and four 8-bit down counter/timer underflow interrupt. If these interrupt sources change signal from high to low, Bank 0 RF register will generate a "1" flag to the corresponding register if you enable the Bank 1 RF register.

Bank 0 RF is an interrupt status register which records the interrupt request in flag bit. Bank 1RF is an interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetched from Address 0003H~0021H according to the interrupt source.

In EM78R469, each individual interrupt source has its own interrupt vector as depicted in the Table (Interrupt vector).

Before the interrupt subroutine is executed, the contents of ACC and the R3 register will be saved by the hardware. After the interrupt service routine is finished, ACC and R3 will be pushed back. In an interrupt service routine, other interrupt service routine should not allowed to be executed. If other interrupts occur in an interrupt service routine, the hardware will save this interrupt, and when the interrupt service routine is finished, only then will it be executed in the next interrupt service routine.

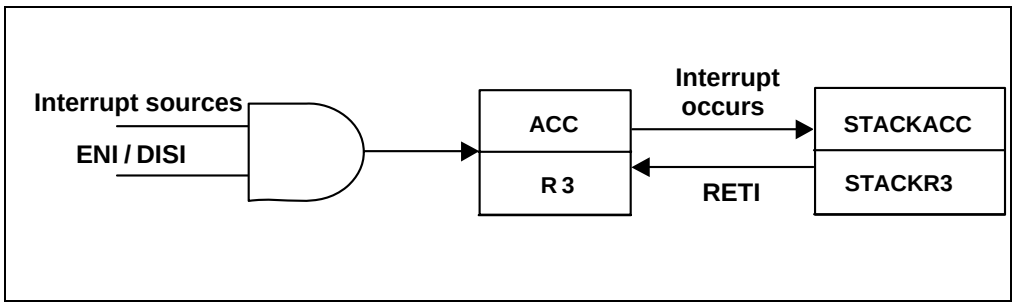


Figure 8-9 Interrupt Back-up Diagram

Interrupt Vector (No priority information)

Interrupt Vector	Interrupt Status
0003H	TCC overflow interrupt
0006H	External interrupt P5.4/INT0 pin
0009H	External interrupt P5.5/INT1 pin
000CH	Counter 1 underflow interrupt
000FH	Counter 2 underflow interrupt
0012H	High-pulse width timer underflow interrupt
0015H	Low-pulse width timer underflow interrupt
0018H	Port 6, Port 8 input status change wake up

8.11 LCD Driver

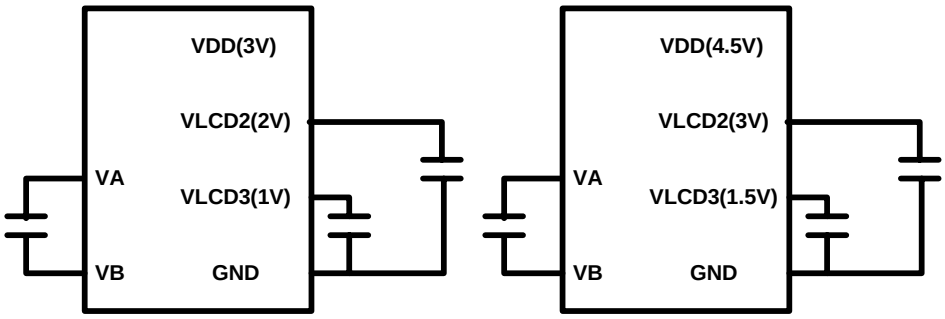
The EM78R469 can drive an LCD of up to 40 segments and 4 commons that can drive a total of 4×40 dots. The LCD block is made up of LCD driver, display RAM, segment output pins, common output pins and LCD operating power supply pins. This circuit can work in normal mode, green mode and idle mode.

The LCD duty, bias, the number of segments, the number of common and frame frequency are determined by the LCD controller register.

The basic structure contains a timing control, which uses the main system clock or subsystem clock to generate the proper timing for different duty and display access. The Bank 0 RC register is a command register for the LCD driver that includes LCD enable/disable, bias (1/2 and 1/3), duty (1/2, 1/3, 1/4) and LCD frame frequency control. The register Bank 1 RD is LCD contrast and LCD RAM address control register. The register Bank 0 RB is an LCD RAM data buffer. The control register is explained as shown below.

The connecting of boosting circuits for LCD voltage is as below:

1/3 bias



1/2 bias

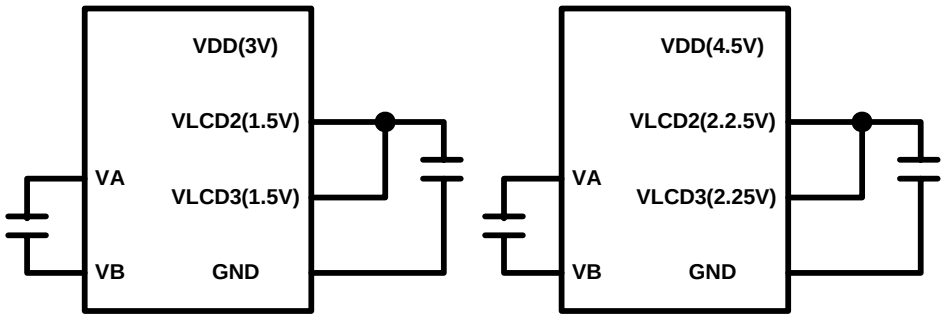
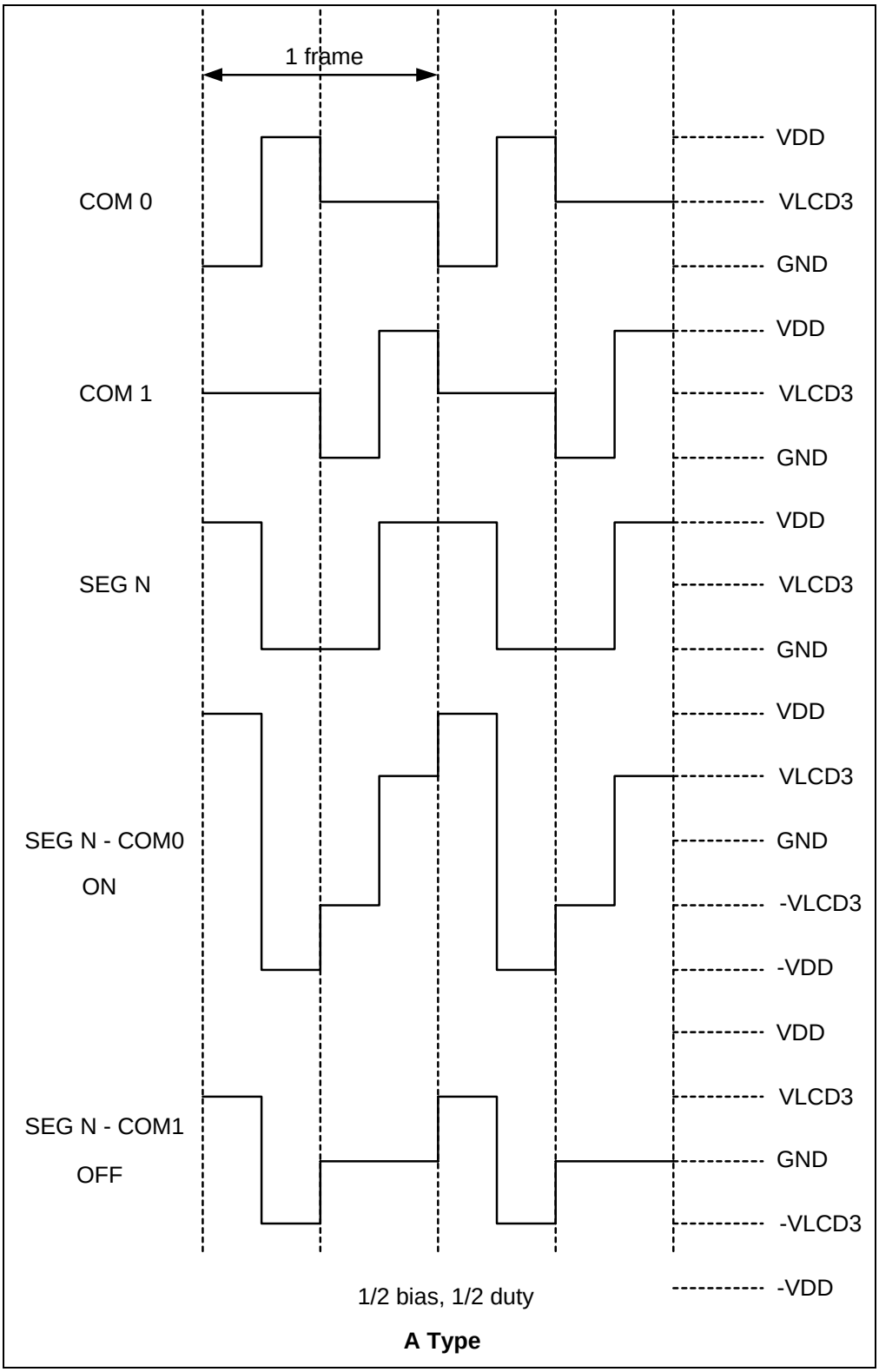


Figure 8-10 Charge Bump Circuit Connection


1 frame
COM 0
COM 1
SEG N
SEG N - COM0
ON
SEG N - COM1
OFF
VDD
VLCD3
GND
-VLCD3
-VDD
1/2 bias, 1/2 duty

A Type

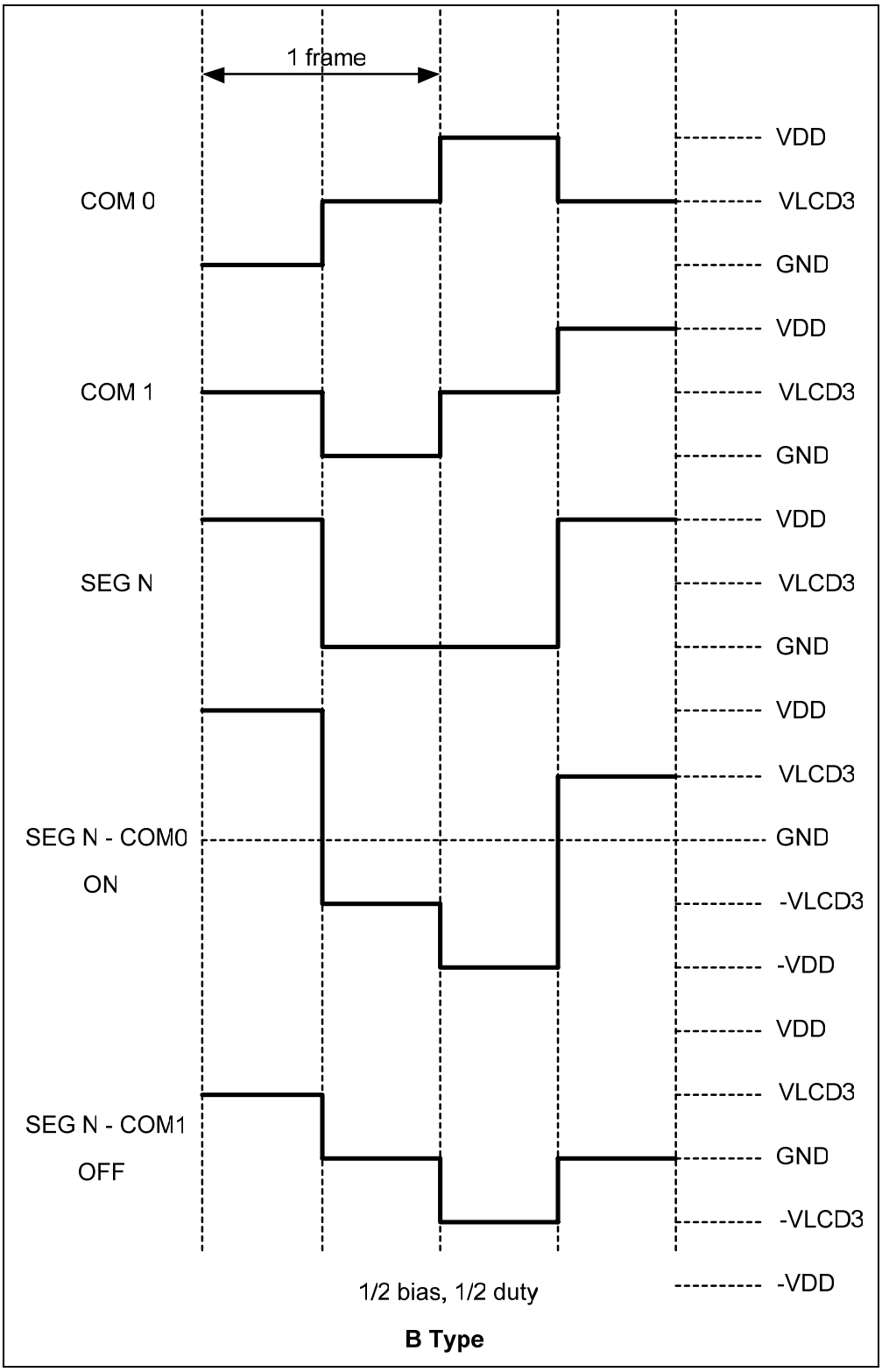
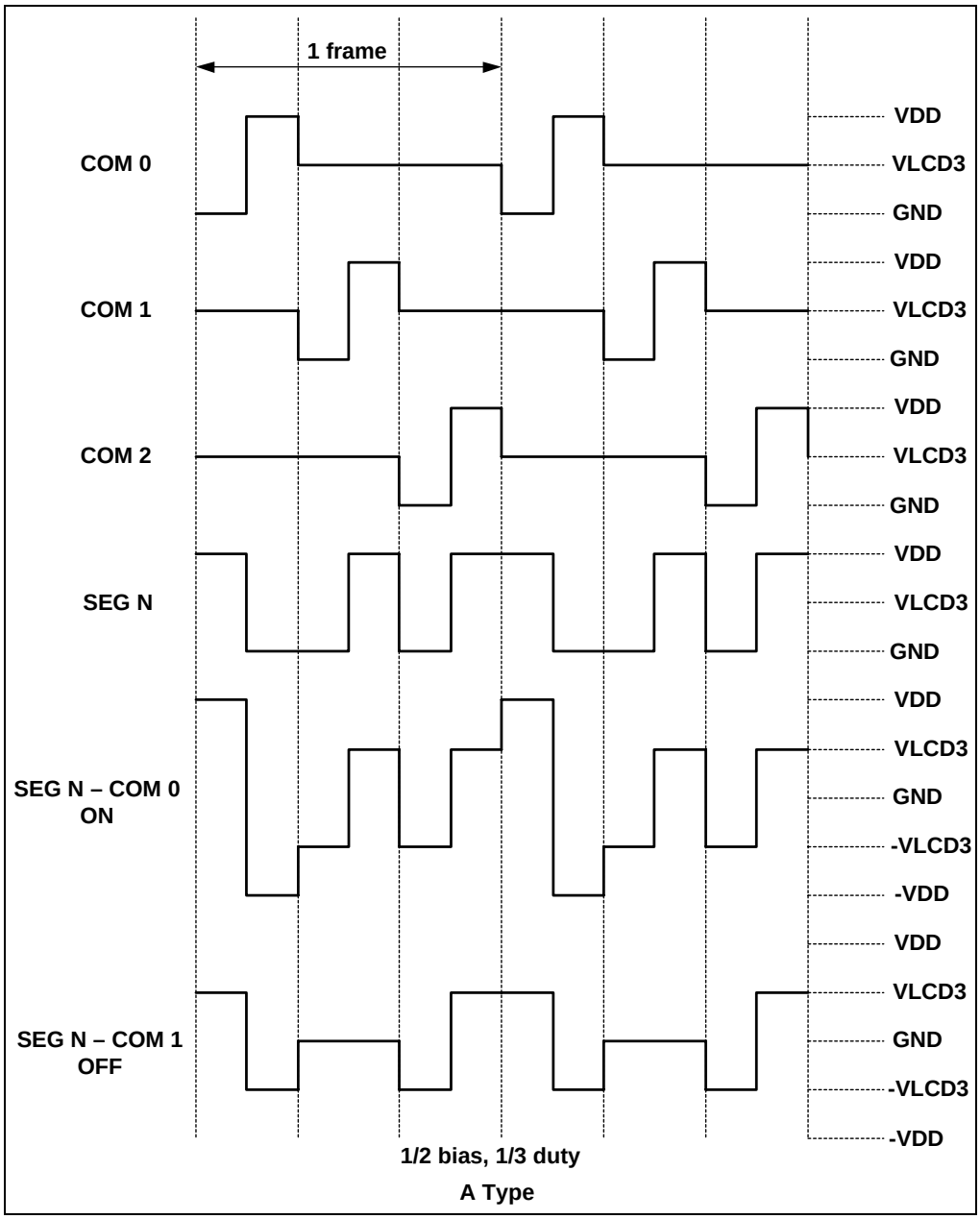


Figure 8-11 LCD Waveform for 1/2 bias, 1/2 Duty


1 frame
COM 0
COM 1
COM 2
SEG N
SEG N – COM 0
ON
SEG N – COM 1
OFF
VDD
VLCD3
GND
-VLCD3
-VDD
1/2 bias, 1/3 duty
A Type

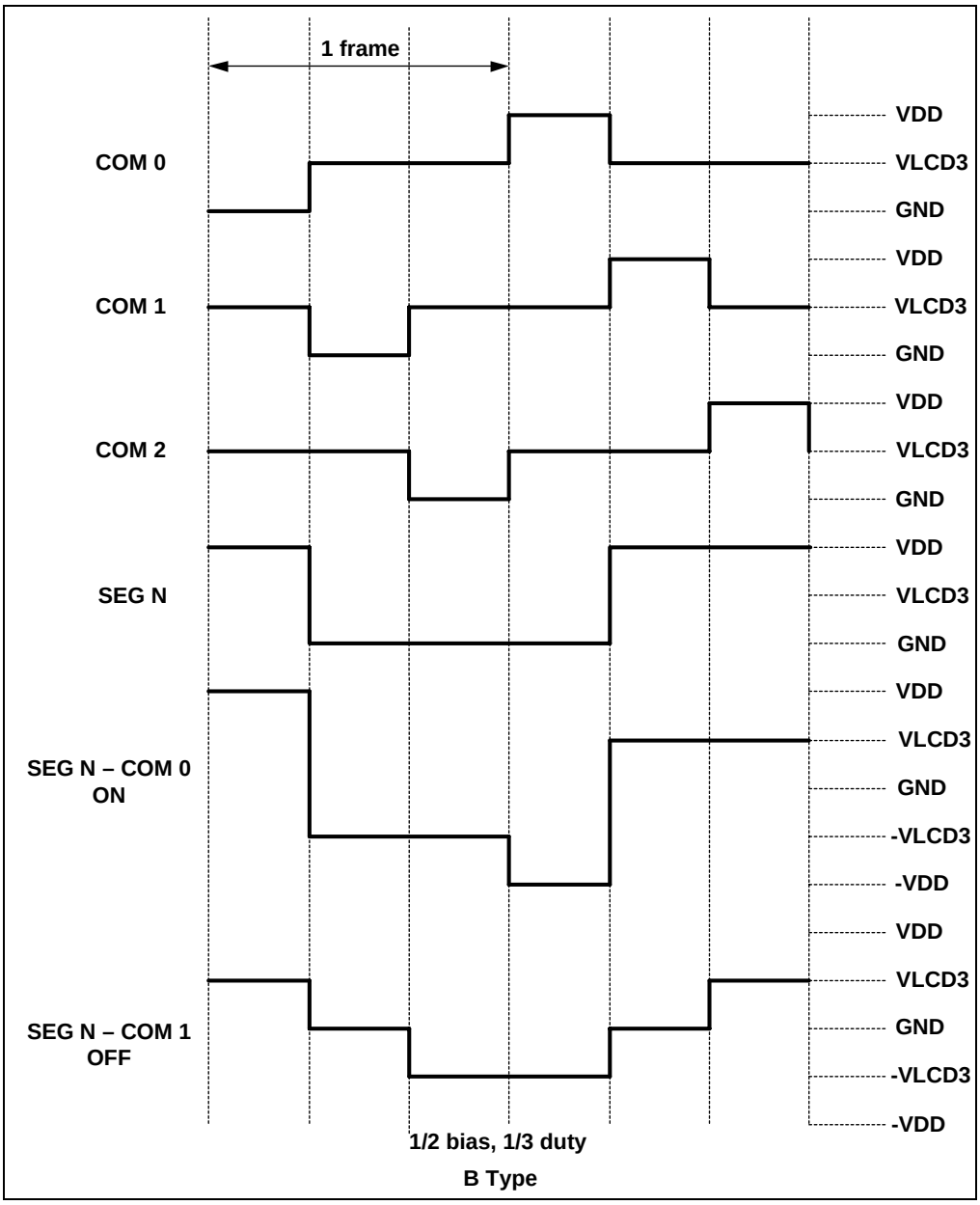


Figure 8-12 LCD Waveform for 1/2 bias, 1/3 Duty

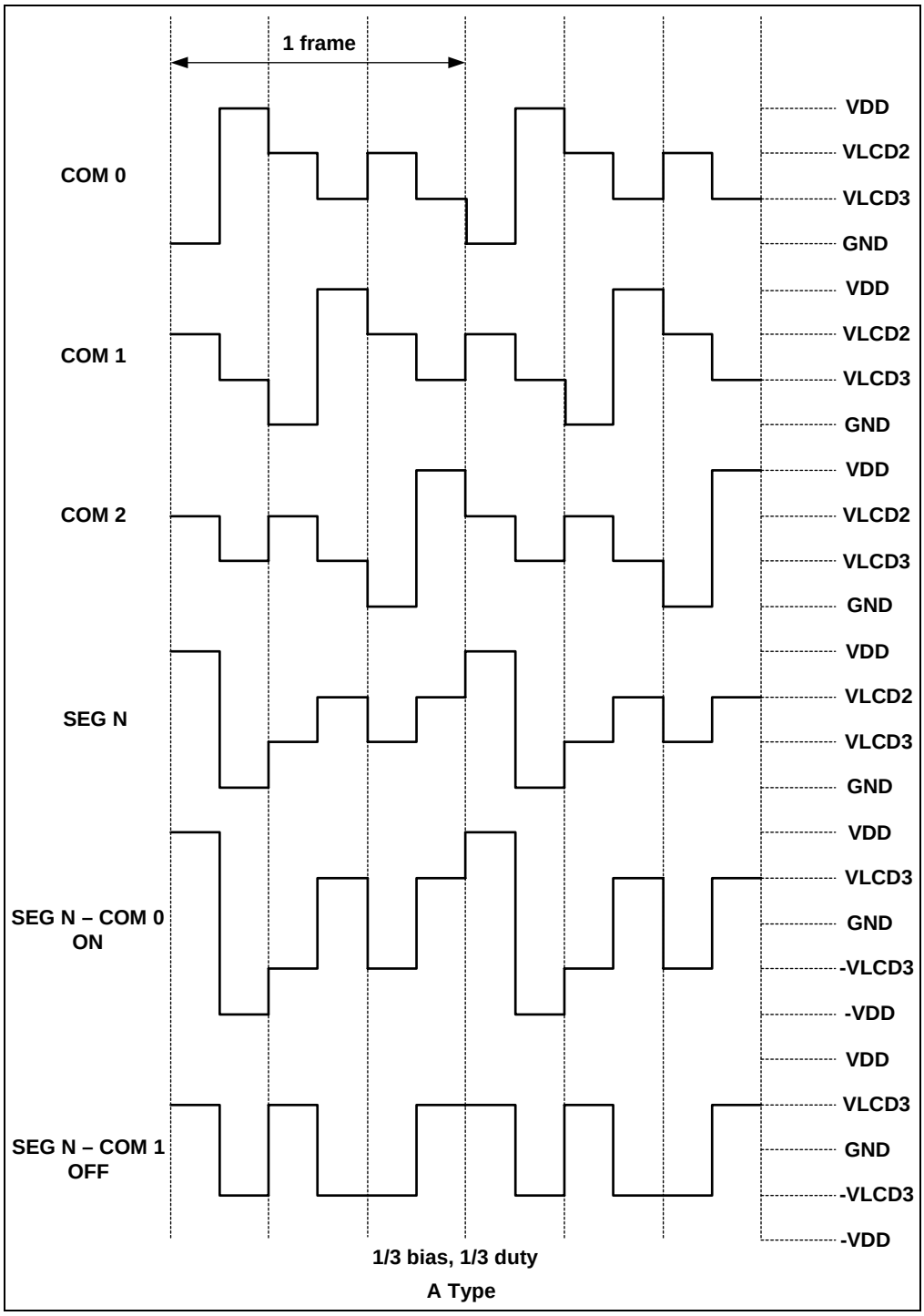


Figure 8-13 LCD Waveform for 1/3 bias, 1/3 Duty

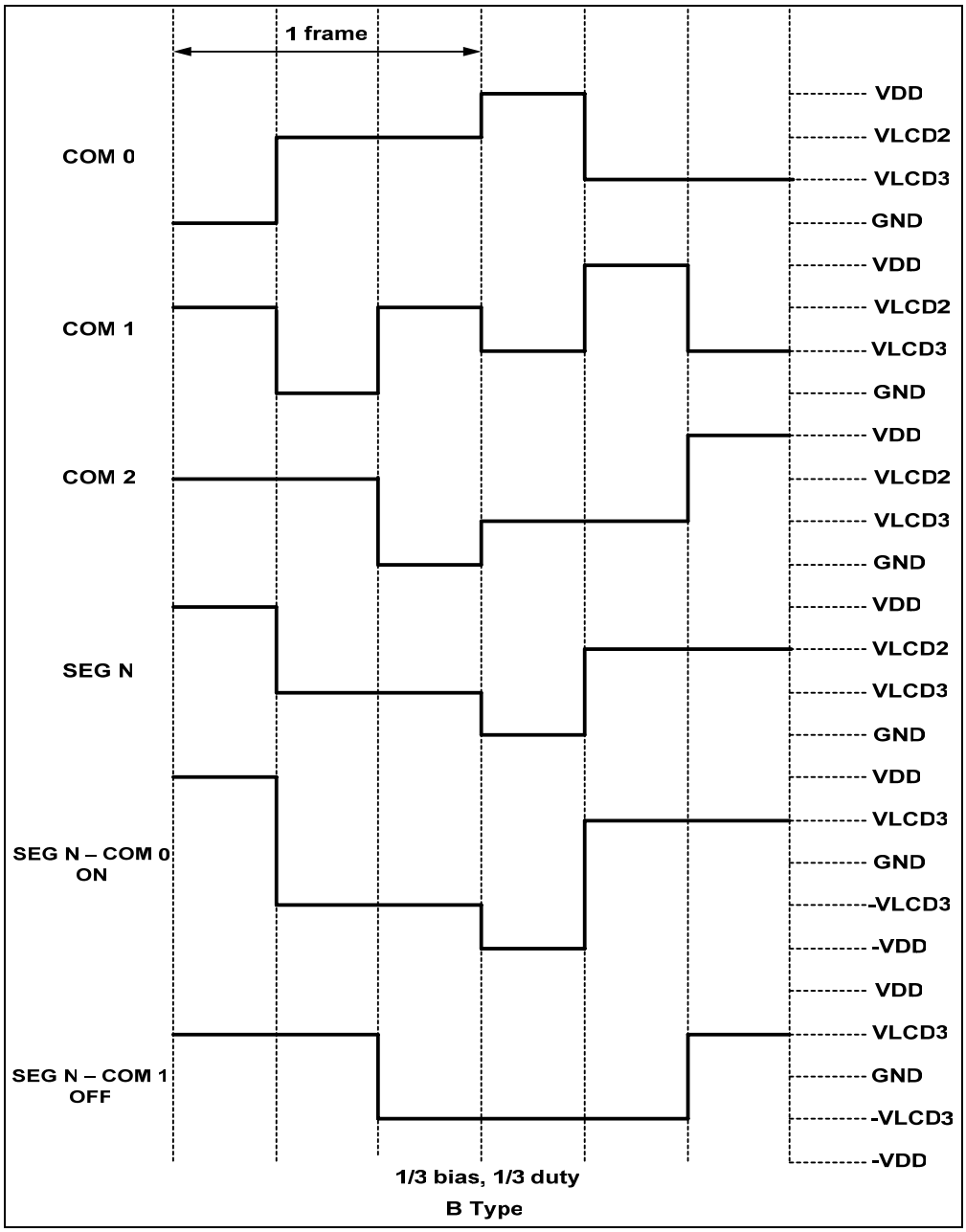


Figure 8-14 LCD Waveform for 1/3 bias, 1/3 Duty

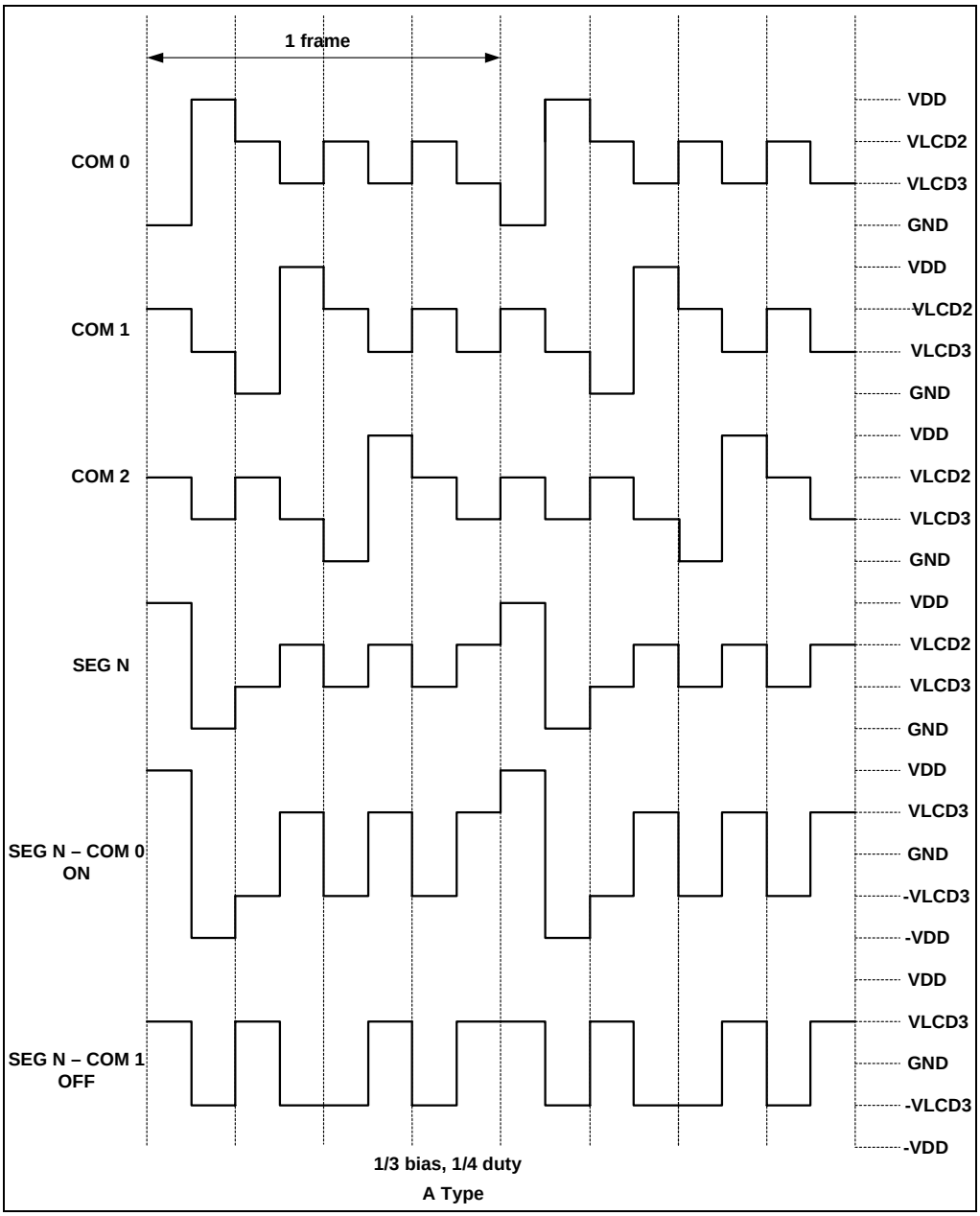


Figure 8-15 LCD Waveform for 1/3 bias, 1/4 Duty

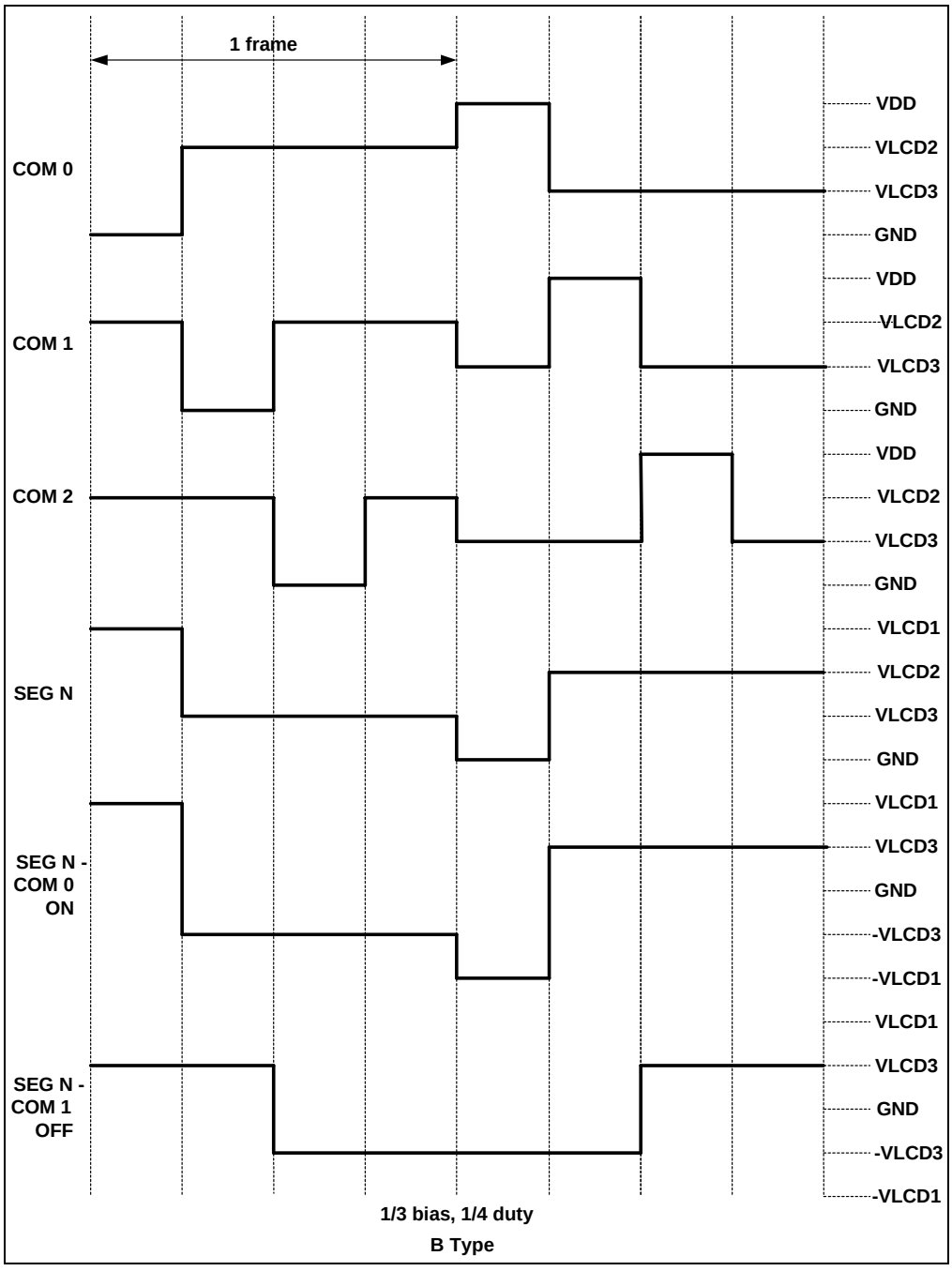


Figure 8-16 LCD Waveform for 1/3 bias, 1/4 Duty

8.12 Infrared Remote Control Application/ PWM Waveform Generate

This LSI can output infrared carrier in user-friendly or in PWM standard waveform. The IR and PWM waveform generated functions include an 8-bit down count timer/counter, high-pulse width timer, low-pulse width timer, and IR control register. The IR system block diagram is shown in Figure 8-17. The IROUT pin waveform is determined by IR control register (RE), IOC90 (Counters 1 and 2 control register), IOCA0 (high-pulse width timer, low-pulse width timer control register), IOCC0 (Counter 2 preset), IOCD0 (high-pulse width timer preset register), and IOCE0 (low-pulse width timer preset register). Details on the Fcarrier, high-pulse time, and low pulse time are explained as follows**:**

If Counter 2 clock source is F_T (this clock source can be set by IOC9), then

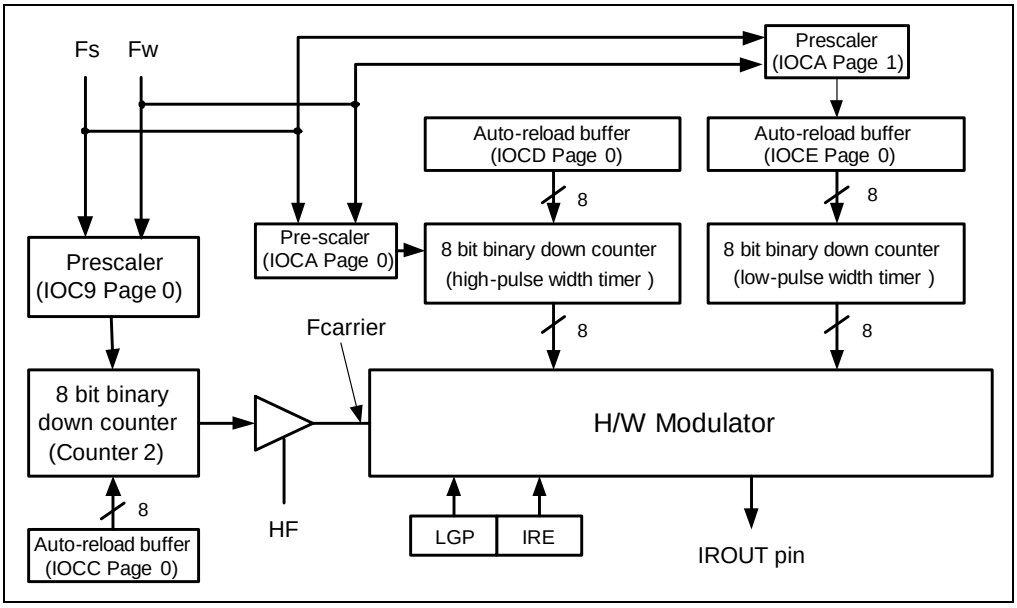
$$F_{carrier} = \frac{F_T}{(1 + decimal \quad of \quad Counter \quad 2 \quad preset \quad value \quad (IOCC \quad 0))}$$

If the high-pulse width timer clock source is FT (this clock source can be set by IOCA), then

$$T_{high \quad pulse \quad time} = \frac{(1 + decimal \quad of \quad high \quad pulse \quad width \quad timer \quad value \quad (IOCD \quad 0))}{F_T}$$

If the low-pulse width timer clock source is FT (this clock source can be set by IOCA);

$$T_{low \quad pulse \quad time} = \frac{(1 + decimal \quad of \quad low \quad pulse \quad width \quad timer \quad value \quad (IOCE \quad 0))}{F_T}$$



Fw: *Internal instruction cycle clock,* **Fs:** *sub-oscillator frequency*

Figure 8-17 IR/PWM System Block Diagram

The IROUT output waveform is explained as follows:

Figure 8-18 LGP=0, HF=1, the IROUT waveform can modulate the Fcarrier waveform when in low-pulse width time.

Figure 8-19 LGP=0, HF=0, the the IROUT waveform cannot modulate the Fcarrier waveform when in low-pulse width time. So the IROUT waveform is determined by high-pulse time and low-pulse time. This mode can produce standard PWM waveform.

Figure 8-20 LGP=0, HF=1, the IROUT waveform can modulate the Fcarrier waveform when in low-pulse width time. When IRE from goes from high to low, the output waveform of IROUT will keep transmitting until high-pulse width timer interrupt occurs.

Figure 8-21 LGP=0, HF=0, the IROUT waveform cannot modulate the Fcarrier waveform when in low-pulse width time. So IROUT waveform is determined by high-pulse time and low-pulse time. This mode can produce standard PWM waveform. When IRE goes from high to low, the output waveform of IROUT will keep transmitting until high-pulse width timer interrupt occurs.

Figure 8-22 LGP=1, when this bit set to high level, the high-pulse width timer is ignored, so IROUT output waveform from low-pulse width timer is established.

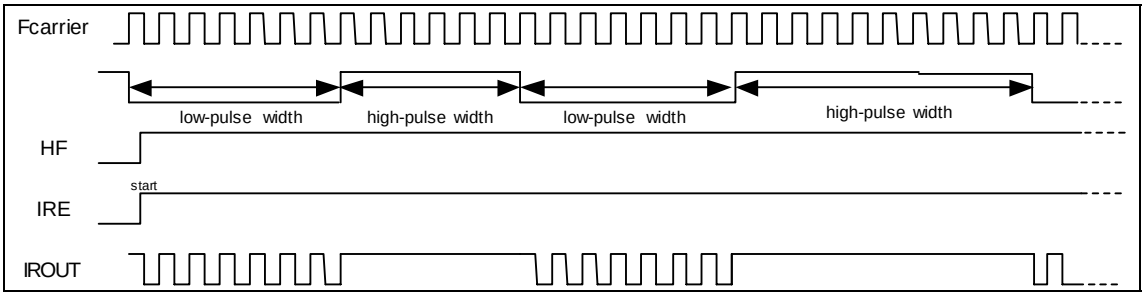


Figure 8-18 LGP=0, IROUT Pin output Waveform

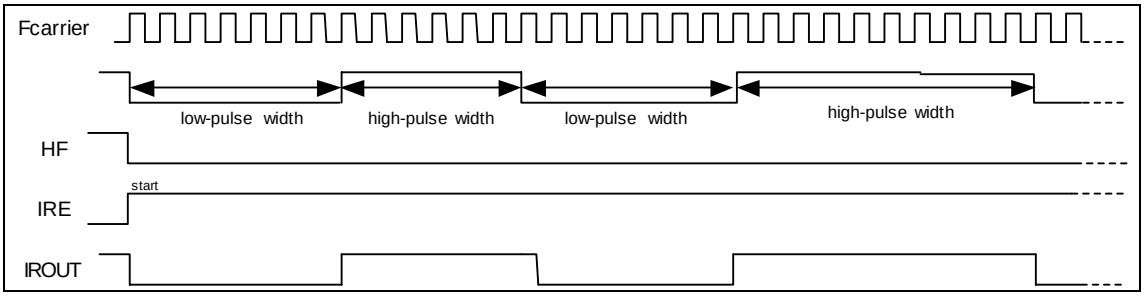


Figure 8-19 LGP=0, IROUT Pin output Waveform

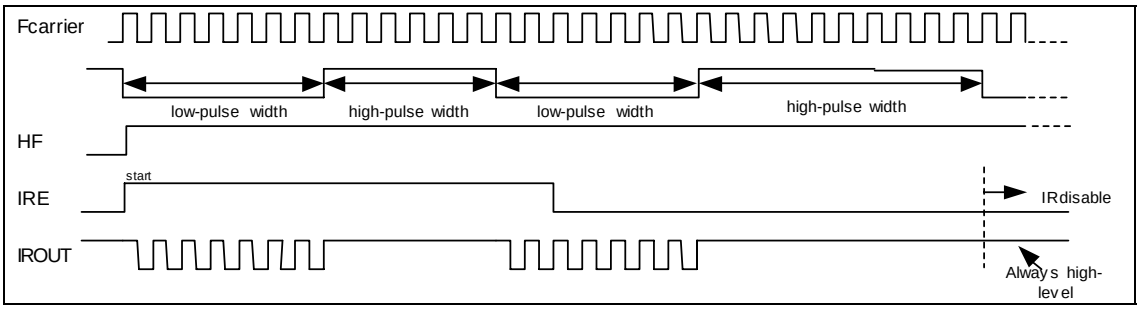


Figure 8-20 LGP=0, IROUT Pin output Waveform

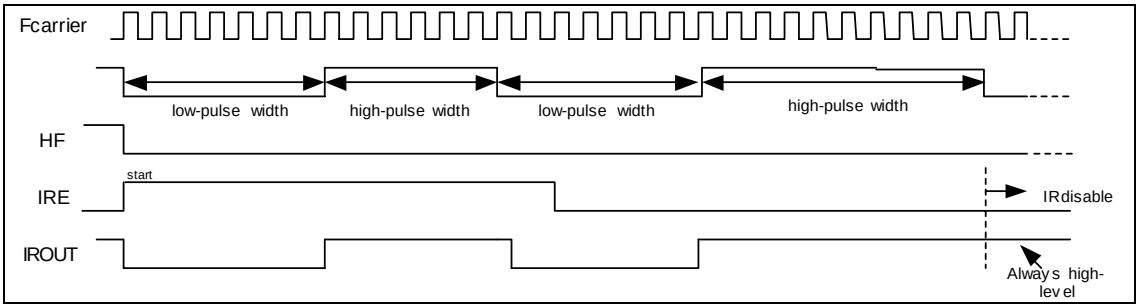


Figure 8-21 LGP=0, IROUT Pin output Waveform

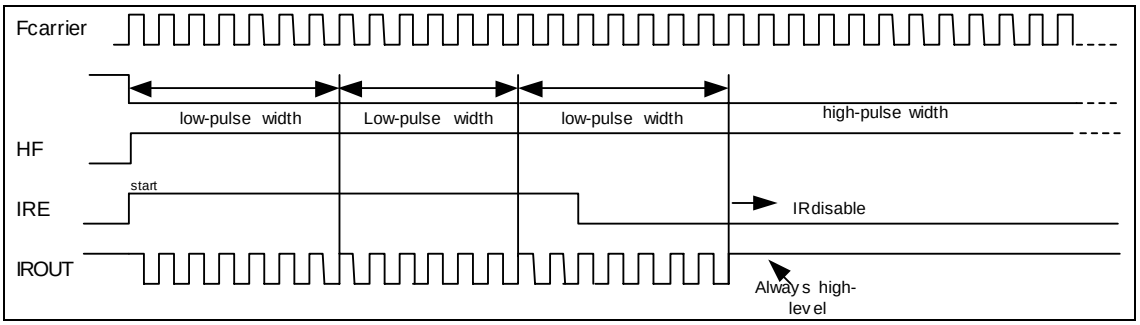


Figure 8-22 LGP=1, IROUT Pin output Waveform

8.13 CNT1 and CNT2 Cascade Architecture

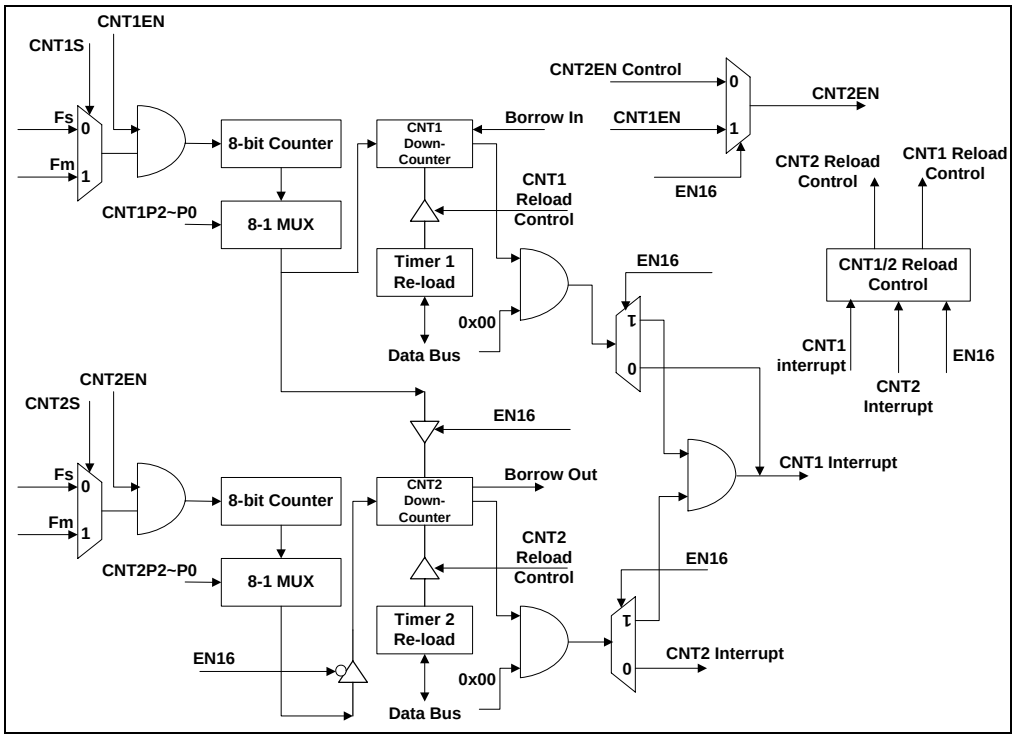


Figure 8-23 CNT1 and CNT2 Cascade Architecture

When EN16=0, CNT1 and CNT2 are independent 8-bit timer and its own independent interrupt service vector. Users can use them at the same time or enable only one of the two.

When EN16=1, CNT1 and CNT2 will be combined into one 16-bit timer, and the clock source will be determined with CNT1S. The prescaler will be determined with CNT1P2~P0. Interrupt service of CNT1 will be used. At the same time, CNT2S, CNT2P2~P0 and interrupt service of CNT2 will be ignored. In 16-bit timer structure, CNT1 will be low-byte and CNT2 will be high-byte. Users can stuff one 16-bit value to them, and interrupt service will occur when counting to 0x0000. The re-load values will be written in to CNT1 and CNT2.

8.13.1 Program Flowchart

■ Enable 16-bit timer:

Step 1: Disable CNT1 and CNT2

Step 2: Set EN16 = 1

Step 3: Write values to registers CNT1 and CNT2

Step 4: Enable CNT1

After those steps, user will have a 16-bit timer.

■ Disable the16-bit timer:

Step 1: Disable CNT1 and CNT2

Step 2: Set EN16 = 0

Step 3: Write values to registers CNT1 and CNT2

After those steps, CNT1 and CNT2 are independent 8-bit timers.

8.14 Code Options

The EM78P469 has one Code Option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Words 0~1
Bit 12~Bit 0

8.14.1 Code Option Register (Word 0)

Word 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	OSCUP	-	CYES	HLFS	ENWDTB	FSMD	FMMD1	FMMD0	HLP	PR2	PR1	PR0

Bit 11 (OSCUP): Select fast or low start-up speed for the oscillator

0 : Oscillator starts with high speed and high power consumption. The time it takes to stabilize, from start to stable time is equal to or smaller than 300 ms.

1 : Oscillator starts with low speed and low power consumption (default). The time it takes to stabilize, from start to stable time is equal to or smaller than 1.2 sec.

Bit 9 (CYES): Cycle select for JMP, CALL instruction

0 : Only one instruction cycle (JMP or CALL) can be executed

1 : Two instruction cycles (JMP or CALL) can be executed (default)

Bit 8 (HLFS): Main or sub-oscillator select

0 : CPU selects the sub-oscillator when reset occurred.

1 : CPU selects the main-oscillator when reset occurred.

Bit 7 (ENWDTB): Watchdog timer enable bit

0 : Enable

1 : Disable

Bit 6 (FSMD): Sub-oscillator type selection

0 : RC type (internal C)

1 : Crystal type (Xin and Xout)

Bits 4, 5 (FMMD0, 1): Main Oscillator type selection

FMMD1	FMMD0	Main Oscillator Type
0	0	RC type (external R, internal C)
0	1	Crystal type (R-OSCI, OSCO)
1	0	PLL type
1	1	PLL type

Bit 3 (HLP): Power consumption selection

0 : Low power consumption mode

1 : High power consumption mode

Bits 2~0 (PR2~PR0): Protect Bit

PR2~PR0 are protect bits, protect type are as follows:

PR2	PR1	PR0	Protect
0	0	0	Enable
0	0	1	Enable
0	1	0	Enable
0	1	1	Enable
1	0	0	Enable
1	0	1	Enable
1	1	0	Enable
1	1	1	Disable

8.14.2 Code Option Register (Word 1)

Word 1												
Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	Customer ID							

Bits 7 ~ 0: Customer ID

8.15 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Change one instruction cycle to consist of 4 oscillator periods.

(B) Executed within two instruction cycles, "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") instructions which were tested to be true. Also execute within two instruction cycles, the instructions that are written to the program counter.

Case (A) is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the 4 oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, not Fosc/2.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None[1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None[2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None[3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 1000 00kk	1E8k	PAGE k	k->R3(7:5)	None
1 1110 1001 00kk	1E9K	BANK k	k->R4(7:6)	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

Note: 1. This instruction is applicable to IOC5~IOF.

2. This instruction is not recommended for R3F operation.

3. This instruction cannot operate under R3F.

9 Absolute Maximum Ratings

Items	Symbol	Condition	Rating		Unit
			Min.	Max.	
Supply voltage	VDD	–	GND-0.3	+5.5	V
Input voltage	V_I	Port 5 ~ Port 8, Port 9	GND-0.3	VDD+0.3	V
Output voltage	V_O	Port 5 ~ Port 8, Port 9	GND-0.3	VDD+0.3	V
Operation temperature	T_{OPR}	–	-20	85	°C
Storage temperature	T_{STG}	–	-65	150	°C
Power consumption	P_D	–	–	500	mW
Operating Frequency	–	–	32.768K	10M	Hz

10 Electrical Characteristic

Ta= -20°C ~85°C, VDD= 5.0V, GND= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768	8M	10M	kHz
Fs	Sub-oscillator	Two cycles with two clocks	–	32.768	–	kHz
ERIC	External R, Internal C for Sub-oscillator	R: 300KΩ, internal capacitance	270	384	500	kHz
	External R, Internal C for Sub-oscillator	R: 2.2MΩ, internal capacitance	22.9	32.768	42.6	kHz
IIL	Input Leakage Current for Input pins	VIN = VDD, GND	-1	0	1	μA
VIH1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8, 9	2.0	–	–	V
VIL1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8, 9	–	–	0.8	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	2.0	–	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	–	0.8	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	2.0	–	–	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	–	–	0.8	V
IOH1	Output High Voltage (Ports 5~8)	VOH = 2.4V, IROCS="0"	-10	–	–	mA
IOL1	Output Low Voltage (Ports 5~8)	VOL = 0.4V, IROCS="0"	–	–	10	mA
IOH1	Output high voltage (P5.7/IROUT pin)	VOH = 2.4V, IROCS="1"	-20	–	–	mA
IOL2	Output Low Voltage (P5.7/IR OUT pin)	VOL = 0.4V, IROCS="1"	–	–	20	mA
IPH	Pull-high current	Pull-high active, input pin at GND	-55	-75	-95	μA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IPL	Pull-low current	Pull-low active, input pin at VDD	55	75	95	μA
ISB	Sleep mode current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	0.5	1.5	μA
ICC1	Idle mode current	/RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, output pin floating, LCD enabled, no load	–	14	18	μA
ICC2	Idle mode current	/RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, output pin floating, TCC enabled	-	5	7	μA
ICC3	Green mode current	/RESET= 'High', CPU ON, Sub-oscillator clock (32.768kHz), Output pin floating, WDT enabled, LCD enabled	–	22	30	μA
ICC4	Normal mode	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating	–	2.2	3	mA
ICC5	Normal mode	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating	–	3.1	4	mA

Ta= -20°C ~85°C, VDD= 3.0V, GND= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768	8M	10M	kHz
Fs	Sub-oscillator	Two cycles with two clocks	–	32.768	–	kHz
ERIC	External R, Internal C for Sub-oscillator	R: 300KΩ, internal capacitance	270	384	500	kHz
	External R, Internal C for Sub-oscillator	R: 2.2MΩ, internal capacitance	22.9	32.768	42.6	kHz
IIL	Input Leakage Current for Input pins	VIN = VDD, GND	-1	0	1	μA
VIH1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	1.8	–	–	V
VIL1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	–	–	0.6	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	1.8	–	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	–	0.6	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	1.8	–	–	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	–	–	0.6	V
IOH1	Output High Voltage (Ports 5~8)	VOH = 2.4V, IROCS="0"	-1.8	–	–	mA
IOL1	Output Low Voltage (Ports 5~8)	VOL = 0.4V, IROCS="0"	–	–	6	mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOH1	Output high voltage (P5.7/IROUT pin)	VOH = 2.4V, IROCS="1"	-3.5	–	–	mA
IOL2	Output Low Voltage (P5.7/IR OUT pin)	VOL = 0.4V, IROCS="1"	–	–	12	mA
IPH	Pull-high current	Pull-high active, input pin at GND	-16	-23	-30	μA
IPL	Pull-low current	Pull-low active, input pin at VDD	16	23	30	μA
ISB	Sleep mode current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	0.1	1	μA
ICC1	Idle mode current	/RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) On, Output pin floating, LCD enabled, no load	–	4	8	μA
ICC2	Idle mode current	/RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) On, Output pin floating, TCC enabled	-	3	5	μA
ICC4	Green mode current	/RESET= 'High', CPU ON, Sub-oscillator clock (32.768kHz), Output pin floating, WDT enabled, LCD enabled	–	10	20	μA
ICC5	Normal mode	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating	–	0.73	1.2	mA

11 AC Electrical Characteristics

Ta=- 20°C ~ 85°C, VDD=5V ± 5%, GND=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

* N= selected prescaler ratio

12 Application Notes

1. If Ports 90~94 will not be used, set them to output.

2. How to use the BANK M function (Bit 0 of the CONT register)

```
When BANKM=0 (default),
;//----- Code example -----//
;//0x09 register of bank0 is LCD control register
;//0x09 register of bank1 is port9 IO register
contr
and a,@0xfe        ;//Set BANKM=0
contw

bank    0
mov     a,@0x55
mov     0x09,a
mov     a,0x09      ;//LCD control setting value will be read out
                       from the LCD control register
                    ;//and store to the accumulator
bank    1
mov     a,0x09      ;//LCD control setting value will be read out
                       from the LCD control register
                    ;//and store to the accumulator
-------------------------------------------------------------
When BANKM=1,
;//----- Code example -----//
contr
or a,@0x01          ;//Set BANKM=1
contw

bank    0
mov     a,@0x55
mov     0x09,a
mov     a,0x09      ;//LCD control setting value will be read out
                       from the LCD control register
                    ;//and store to the accumulator
bank    1
mov     a,0x09      ;//Port 9 IO state will be read out from Port9
                       IO register and
                    ;//store to the accumulator
```

3. TCS and TCCWAKE function (Bit 3 and Bit 1 of the CONT register)

TCS and TCCWAKE bits are defined as both 0 and TCC behavior will be the same with EM78P468. When you setup some values to them, refer to the table as follows:

TS	TCS	TCCWAKE	MCU Mode	TCC Clock Source
0	0	0	Green/normal	Instruction cycle
			Idle	None. The MCU will not be waken up from idle mode. TCC will stop counting when the MCU is in idle mode.
0	0	1	Green/normal	Instruction cycle
			Idle	None. The MCU will not be waken up from idle mode. TCC will stop counting when the MCU is in idle mode.
0	1	0	Green/normal	Instruction cycle
			Idle	None. The MCU will not be waken up from idle mode. TCC will stop counting when the MCU is in idle mode.
0	1	1	Green/normal	Instruction cycle
			Idle	None. The MCU will not be waken up from idle mode. TCC will stop counting when the MCU is in idle mode.
1	0	0	Green/normal	From P56
			Idle	From P56. The MCU will not be waken up from idle mode. TCC will keep counting when the MCU is in idle mode.
1	0	1	Green/normal	From P56
			Idle	From P56. The MCU will be waken up from idle mode by TCC time out. TCC will keep counting when the MCU is in idle mode.
1	1	0	Green/normal	Internal 32kHz
			Idle	Internal 32kHz. The MCU will not be waken up from idle mode. TCC will keep counting when the MCU is in idle mode.
1	1	1	Green/normal	Internal 32kHz
			Idle	Internal 32kHz. The MCU will be waken up from idle mode by TCC time out. TCC will keep counting when the MCU is in idle mode.

Note: There is a priority relation between TS and TCS. If TS is set to 0, the TCC clock will execute the instruction cycle and the set value for the TCS will be ignored. In other words, the TCS setting will be set only when TS is set to 1.

4. Since the ICE469 has more I/Os than the EM78P469, users should take note of the I/O read/write processing, especially in Port 9.

5. When users want to change the MCU operation clock, a delay or NOP instruction should be added to wait for the clock to stabilize. The minimum requirement is 6 NOP instructions time.

6. All bits of unused registers will be read out as 0.

7. There is a difference between the ICE469 and the EM78P469 when the LCD control register (Bank 0, R9) is set.

In ICE469, the LCD function will work continually when users write or re-load value to the LCD control register (Bank 0, R9). In EM78P469, the LCD function will be shut down immediately and wait for about $T\max = \frac{1}{2} \times \frac{1}{32768}$ to re-enable the LCD function again when users write or re-load value to the LCD control register (Bank 0, R9). So, it is suggested to write the LCD setting code in a repeat loop which is executed repeatedly and quickly, for example:

```
;---------- Program In ICE469 ----------
Loop:
Bank 0
MOV A,@0XD3
MOV 0x9,A
JMP Loop              ; LCD function will work fine
                      ; in this repeat loop
```

```
;---------- Program In EM78P469 ----------
Loop:
Bank 0
MOV A,@0XD3
MOV 0x9,A
JMP Loop             ; LCD function will have a bad
                     ; execution result in this
                     ; repeat loop
```

Users should keep this message in mind when programming code and verify the programmed code in both EM78P469 and ICE469.

APPENDIX

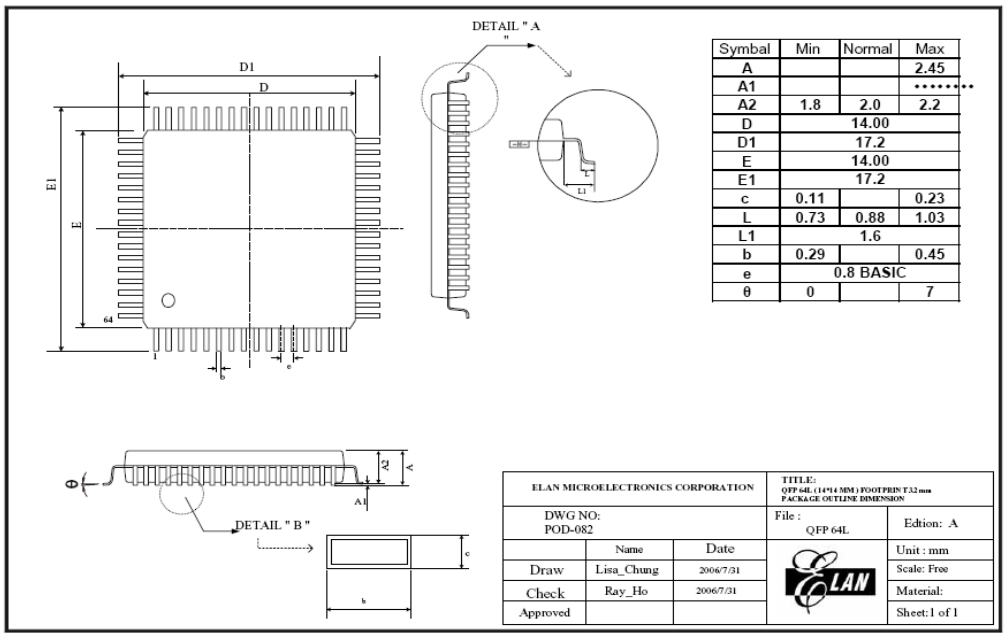
A Comparison Table

The following is a Comparison Table for ICE469, EM78P469 and EM78P468

	ICE469	EM78P469	EM78P468N
Function			
Operating Voltage	2.1V ~ 5.5V	2.3V ~ 5.5V	Commercial: 2.3V~5.5V Industrial: 2.5V~5.5V
Max. Operating Frequency	Oscillator mode: 10 MHz @ 5.0V PLL mode: 8 MHz	Oscillator mode: 10 MHz @ 5.0V PLL mode: 8 MHz	Oscillator mode: 10 MHz @ 5.0V PLL mode: 8 MHz
Operating Temperature	NA	-20°C~85°C	Commercial: 0°C~70°C Industrial:-40°C~+85°C
ROM Size	8K × 13	8K × 13	4K × 13
Bank RAM Size	128 Bytes	128 Bytes	128 Bytes
Data RAM Size	512 Bytes	512 Bytes	128 Bytes
Max. I/O (Including Shared pins)	40	33	28
LCD (Max COM/SEG)	COM/SEG: 4/40 Duty: 1/4, 1/3, 1/2 Bias: 1/3, 1/2 Type: A/B	COM/SEG: 4/40 Duty: 1/4, 1/3, 1/2 Bias: 1/3, 1/2 Type: A/B	COM/SEG: 4/32 Duty: 1/4, 1/3, 1/2 Bias: 1/3, 1/2 Type: A/B
PWM/IROUT	Yes	Yes	Yes
TCC Wake-up for Idle	Yes	Yes	No
16-bit Counter	No	Yes	No
12-bit AD Converter	Yes	No	No
Comparator	Yes	No	No

B Package Information

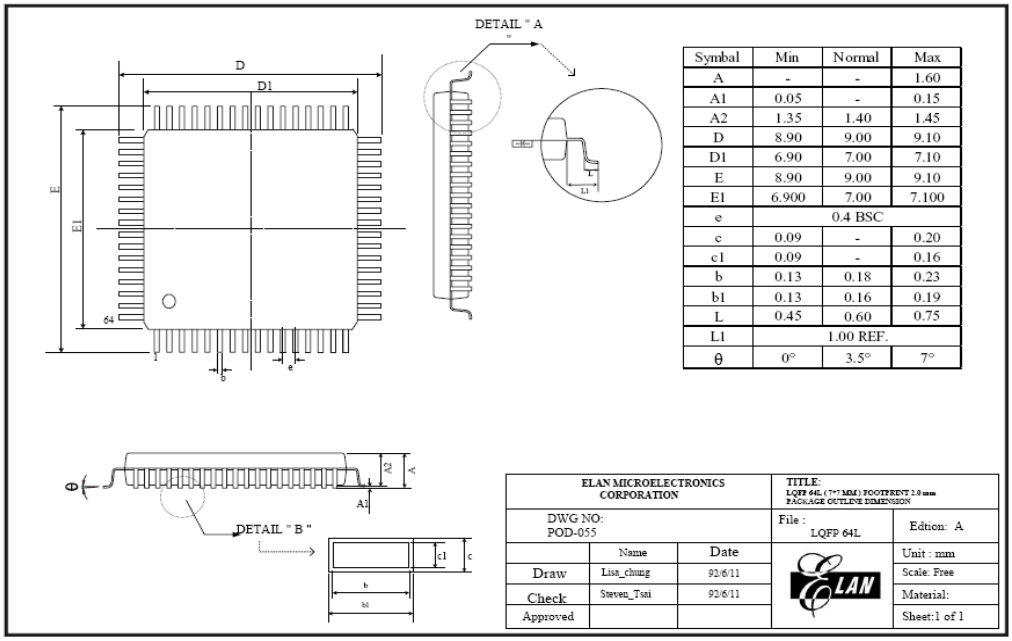
B.1 Package Size for EM78P469AQ64J and EM78P469BQ64J



Symbal	Min	Normal	Max
A			2.45
A1			•••••••••
A2	1.8	2.0	2.2
D		14.00	
D1		17.2	
E		14.00	
E1		17.2	
c	0.11		0.23
L	0.73	0.88	1.03
L1		1.6	
b	0.29		0.45
e		0.8 BASIC	
θ	0		7

ELAN MICROELECTRONICS CORPORATION			TITLE: QFP 64L (14*14 MM) FOOTPRINT 2.72 mm PACKAGE OUTLINE DIMENSION
DWG NO: POD-082			File : QFP 64L
	Name	Date	Edtion: A
Draw	Lisa_Chung	2006/7/31	Unit : mm
Check	Ray_Ho	2006/7/31	Scale: Free
Approved			Material:
			Sheet:1 of 1

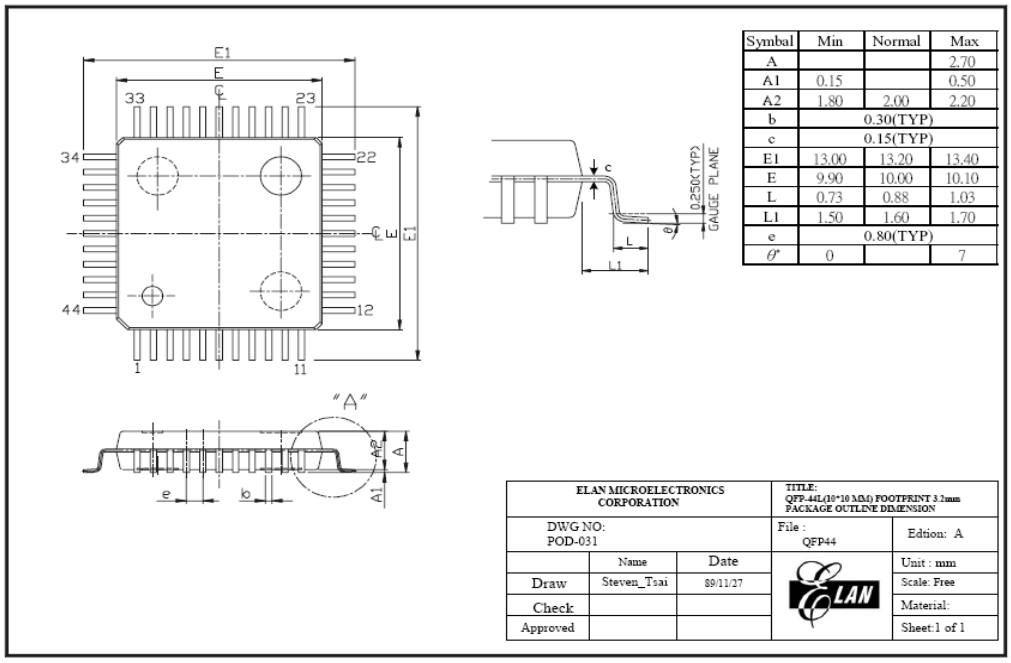
B.2 Package Size for EM78P469AL64J and EM78P469BL64J



Symbal	Min	Normal	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	8.90	9.00	9.10
D1	6.90	7.00	7.10
E	8.90	9.00	9.10
E1	6.900	7.00	7.100
e		0.4 BSC	
c	0.09	-	0.20
c1	0.09	-	0.16
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
L	0.45	0.60	0.75
L1		1.00 REF.	
θ	0°	3.5°	7°

ELAN MICROELECTRONICS CORPORATION			TITLE: LQFP 64L (7*7 MM) FOOTPRINT 2.0 mm PACKAGE OUTLINE DIMENSION
DWG NO: POD-055			File : LQFP 64L
	Name	Date	Edtion: A
Draw	Lisa_chung	92/6/11	Unit : mm
Check	Steven_Tsai	92/6/11	Scale: Free
Approved			Material:
			Sheet:1 of 1

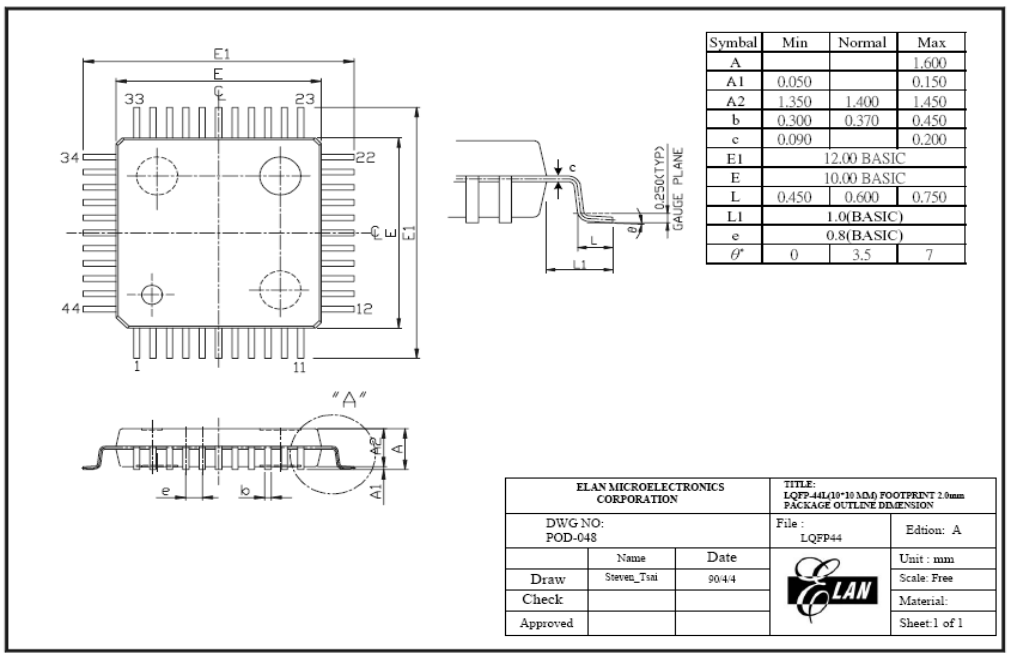
B.3 Package Size for EM78P469Q44J



Symbal	Min	Normal	Max
A			2.70
A1	0.15		0.50
A2	1.80	2.00	2.20
b		0.30(TYP)	
c		0.15(TYP)	
E1	13.00	13.20	13.40
E	9.90	10.00	10.10
L	0.73	0.88	1.03
L1	1.50	1.60	1.70
e		0.80(TYP)	
θ°	0		7

ELAN MICROELECTRONICS CORPORATION			TITLE: QFP-44L(10*10 MM) FOOTPRINT 3.2mm PACKAGE OUTLINE DIMENSION	
DWG NO: POD-031			File : QFP44	Edtion: A
	Name	Date		Unit : mm
Draw	Steven_Tsai	89/11/27		Scale: Free
Check				Material:
Approved				Sheet:1 of 1

B.4 Package Size for EM78P469L44J



Symbal	Min	Normal	Max
A			1.600
A1	0.050		0.150
A2	1.350	1.400	1.450
b	0.300	0.370	0.450
c	0.090		0.200
E1		12.00 BASIC	
E		10.00 BASIC	
L	0.450	0.600	0.750
L1		1.0(BASIC)	
e		0.8(BASIC)	
θ°	0	3.5	7

ELAN MICROELECTRONICS CORPORATION			TITLE: LQFP-44L(10*10 MM) FOOTPRINT 2.0mm PACKAGE OUTLINE DIMENSION	
DWG NO: POD-048			File : LQFP44	Edtion: A
	Name	Date		Unit : mm
Draw	Steven_Tsai	90/4/4		Scale: Free
Check				Material:
Approved				Sheet:1 of 1