EM88F794N

8-BIT Microcontroller

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

April 2018

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Specification Revision History

Version	Revision Description	Date
1.0	Initial Version	2018/04/09

User Application Note

(Before using this IC, take a look at the following description note, it includes important messages.)

1. We strongly recommend placing an external 100nF MLCC between VDD and VSS and as close to the IC as possible.

2. The value in the dead-time register must be less than the value in the duty cycle register, in order to prevent unexpected behaviors on both of the PWM outputs.

3. During ADC conversion, do not perform output instruction to maintain precision for all of the pins. In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion.

4. When TM4 is in capture mode, its behavior is different from TM1/ TM2/ TM3. It has TM4SF and TM4DBSF flags, which can be used to determine if an interrupt is caused by a period or a duty.

1 General Description

EM88F794N is an 8-bit low-cost high performance MCU equipped with DC fan motor driver. EM88F794N is a microprocessor designed and developed with low-power, high-speed CMOS technology. It has an on-chip 4K×16-bits electrical flash memory.

The timer that can perform various PWM operations operates at a maximum resolution of 32 MHz and is provided with several functions, such as PWM (complementary PWM × 3 channels) output function with dead time, 6-phase PWM output function, DC inverter real-time output function, and can perform inverter control.

The MCU is designed as a cost effective processors offering optimized performance and are ideal for DC motor driving applications. EM88F794N constructive features motivate exploration into wide variety of new creative ideas for more innovative products that drive DC motors.

The debug function is built in EM88F794N chip. User can read the program code from OCDS port and monitor the on chip register status, memory and program trace log on computer.

Using OCDS, user can develop their program for several flash types of ELAN IC

2 Features

- CPU configuration
  - 4K×16-bit Flash memory
  - (48+256) bytes general purpose register
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - 8×8 Multiplier
  - Less than 6 mA at 5V/32MHz
  - Typically 1 μA, during sleep mode
  - Power-On Reset 2.1V
  - Three Programmable Brown-out Reset
    BOR: 4.6V, 3.9V, 2.8V
  - Three Programmable Level Voltage Detectors
    LVD: 4.7V, 4.1V, 3.0V
  - Four CPU operation modes (Normal, Green, Idle, Sleep)
- I/O port configuration
  - Three bidirectional I/O ports: P5~P7
  - Three programmable pin change wake-up ports : P5~P7
  - Three programmable pull-down I/O ports: P5~P7
  - Three programmable pull-high I/O ports: P5~P7
  - Three programmable open-drain I/O ports: P5~P7
  - Three programmable high-sink/drive I/O ports: P5~P7
- Operating voltage range:
  - 3.0V~5.5V at -40°C~+125°C (Industrial Grade)
- Operating frequency range (base on two clocks):

Main oscillator:

- IRC mode:

  DC ~ 32 MHz at 4.5V~5.5V

  DC ~ 28 MHz at 4.2V~5.5V

  DC ~ 24 MHz at 4.2V~5.5V

  DC ~ 20 MHz at 3.0V~5.5V

InternalRC Frequency	Drift Rate			
	Temp.	Voltage	Process	Total
32 MHz	±0.8% (0℃~65℃) (4.5V~5.5V)			±1%
	±1.8% (-40℃~85℃) (4.5V~5.5V)		±0.2%	±2%
	±2.8% (-40℃~125℃) (4.5V~5.5V)			±3%
20 MHz 24 MHz 28 MHz	±1.5% (0℃~65℃) (3V~5.5V)			±3%
	±2.5% (-40℃~80℃) (3V~5.5V)		±1.5%	±4%
	±3.5% (-40℃~125℃) (3V~5.5V)			±5%

Sub oscillator:

- IRC mode: 16k/128kHz

- Peripheral configuration
  - Four 16-bit timers (TM1/TM2/TM3/TM4) with seven modes:

    Timer/Counter/Capture/Window/Buzzer/PWM/ PDO (Programmable Divider Output) modes.
  - 6+1 channels Analog-to-Digital Converter with 12-bit resolution:

    One of the channels is 1/2 VDD power detection

    ADC Buffer mode

    Power down (Sleep) mode
  - Two Comparator
    Comparator 2 has hysteresis function
  - One 16-bit PWM
    Three group Pulse Width Modulation(PWM) complementary output with dead time
  - One 16-bit PWM / Capture
  - High EFT/ESD immunity
- 31 available interrupts: (11 external, 20 internal)
  - External interrupt: EINT0,EINT1
  - TM1, TM2, TM3,TM4 overflow interrupt
  - TM5, TM6 period/duty match completion
  - Input-port status changed interrupt
  - ADC completion interrupt
  - LVD interrupt
  - Comparators 1~2 interrupt
  - System hold interrupt
  - PWM brake interrupt
  - Hall edge interrupt
- Single instruction cycle commands
- Programmable free running watchdog timer
  - Watchdog Timer: 16.5ms ± 5% with VDD =5V at 25°C, Temperature range ± 7.5% (-40°C ~+125°C)
  - Two clocks per instruction cycle
  - Package Type:
    - 20-pin TSSOP : 173mil EM88F794NTS20

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Configuration

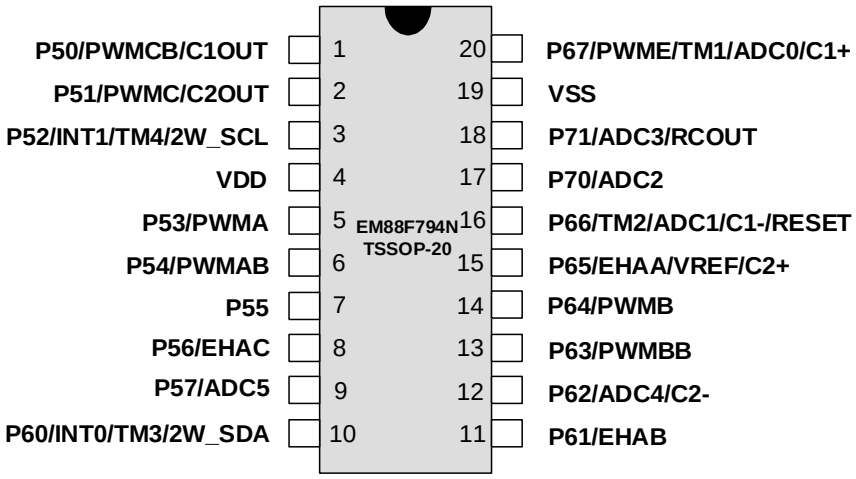


Figure 3-1 EM88F794N TSSOP-20 Pin Assignment

4 Pin Description

Name	Function	Input Type	Output Type	Description
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground
P50/PWMCB/C1OUT	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWMCB	–	CMOS	Complementary PWM output of Channel C
	C1OUT	–	CMOS	Comparator 1 output
P51/PWMC/C2OUT	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWMC	–	CMOS	PWM output of channel C
	C2OUT	–	CMOS	Comparator 2 output
P52/INT1/TM4/2W_SCL	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	INT1	ST	–	External Interrupt 1
	TM4	ST	CMOS	16-bit Timer/Counter 4
	2W_SCL	ST	CMOS	On-chip debug system clock pin
P53/PWMA	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWMA		CMOS	PWM output of Channel A
P54/PWMAB	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wakeup
	PWMAB		CMOS	Complementary PWM output of Channel A
P55	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P56/EHAC	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	EHAC	ST	–	Hall sensor input
P57/ADC5	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC5	AN	–	ADC Input 5

Name	Function	Input Type	Output Type	Description
P60/INT0/TM3/2W_SDA	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	INT0	ST	–	External Interrupt 0
	TM3	ST	CMOS	16-bit Timer/Counter 3
	2W_SDA	ST	CMOS	On-chip debug system data pin
P61/EHAB	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	EHAB	ST	–	Hall sensor input
P62/ADC4/C2-	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC4	AN	–	ADC input 4
	C2-	AN	–	Inverting end of Comparator 2
P63/PWMBB	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWMBB	–	CMOS	Complementary PWM output of Channel B
P64/PWMB	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWMB	–	CMOS	PWM output of Channel B
P65/EHAA/VREF/C2+	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	EHAA	ST	–	Hall sensor input
	VREF	AN	–	Voltage reference for ADC
	C2+	AN	–	Non-inverting end of Comparator 2
P66/TM2/ADC1/C1-/RESET	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TM2	ST	CMOS	16-bit Timer/Counter 2
	ADC1	AN	–	ADC Input 1
	C1-	AN	–	Inverting end of Comparator 1
	RESET	ST	–	

Name	Function	Input Type	Output Type	Description
P67/PWME/TM1/ ADC0/C1+	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWME	–	CMOS	PWM output of Channel E
	TM1		–	16-bit Timer/Counter 1
	ADC0	AN	–	ADC input 0
	C1+	AN	–	Non inverting end of Comparator 1
P70/ADC2	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC2	AN	–	ADC Input 2
P71/ADC3/RCOUT	P71	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC3	AN	–	ADC Input 3
	RCOUT	–	CMOS	Clock output of resonator oscillator

5 Functional Block Diagram

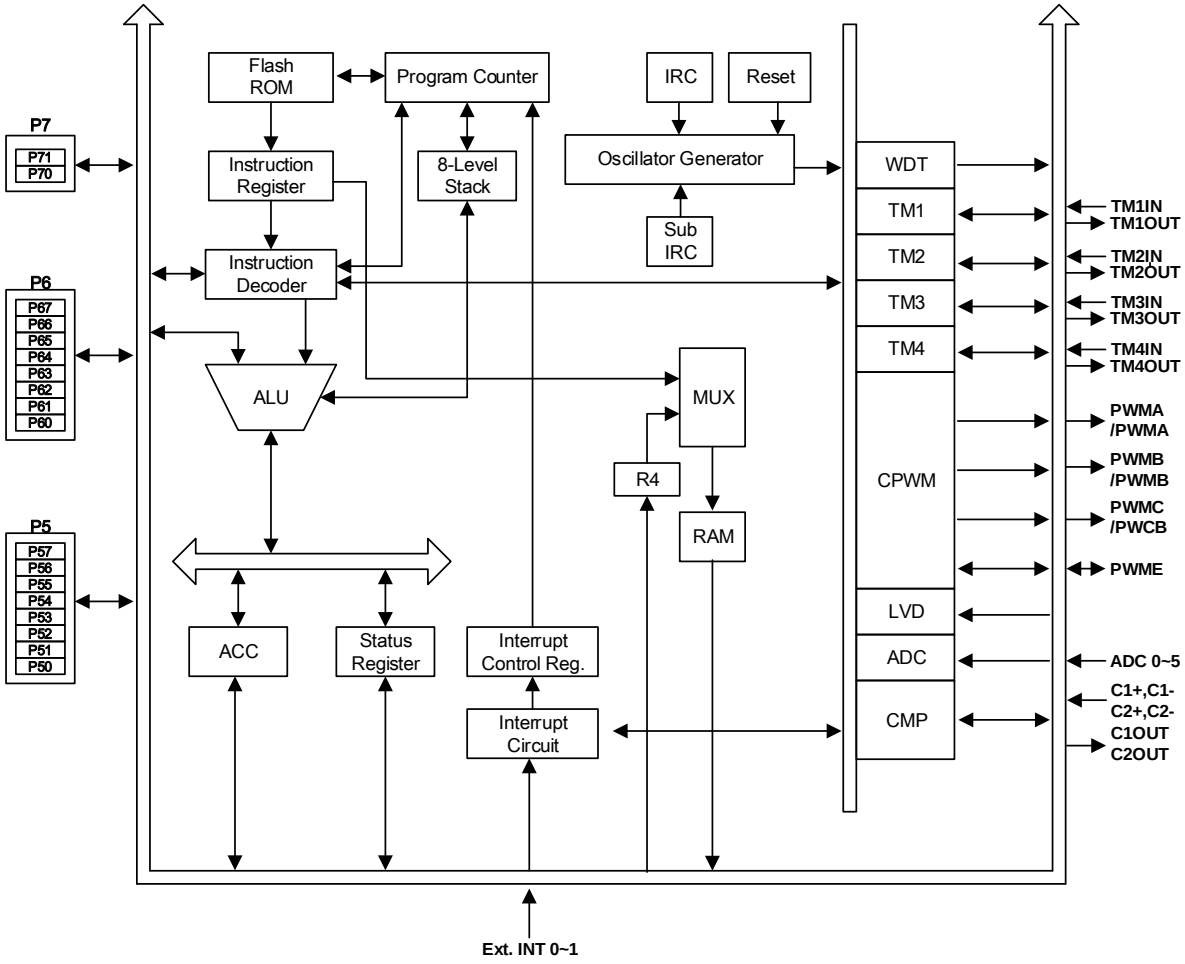


Figure 5-1 Function Block Diagram

6 Function Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Selection Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SBS1	SBS0	-	-	-	GBS0
0	0	R/W	R/W	0	0	0	R/W

Bits 7~6: Not used, set to "0" all the time.

Bits 5~4 (SBS1~SBS0): special register bank select bit. It is used to select Bank 0/1/2 of special register **R5~R4F**.

SBS1	SBS0	Special Register Bank
0	0	0
0	1	1
1	0	2
1	1	x

Bits 3~2: Not used, set to "0" all the time.

Bits 2~0 (GBS1~GBS0): general register bank select bit. It is used to select Bank 0/1 of general register R80~RFF.

GBS0	RAM Bank
0	0
1	1

6.1.3 R2: PCL (Program Counter Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PC7~PC0): The low byte of program counter.

- Depending on the device type, R2 and hardware stack are 15-bit wide. The structure is depicted in Figure 6-1.

- Generate 4K×16 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "0"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, the present PC value will add 1 and is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 12 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 4K (2^{12}).
- "LCALL" instruction loads the lower 12 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC won't be changed.
- Any instruction except "ADD R2,A" that is written to R2 (e.g. "MOV R2, A", "BC R2, 6","INC R2", etc.) will cause the ninth and above bits (PC8~PC11) of the PC to remian unchanged.
- All instructions are single instruction cycle (Fsys/2) except "LCALL", "LJMP" and the instructions corresponding to the operation on R2. Those instructions require two instructions cycles.

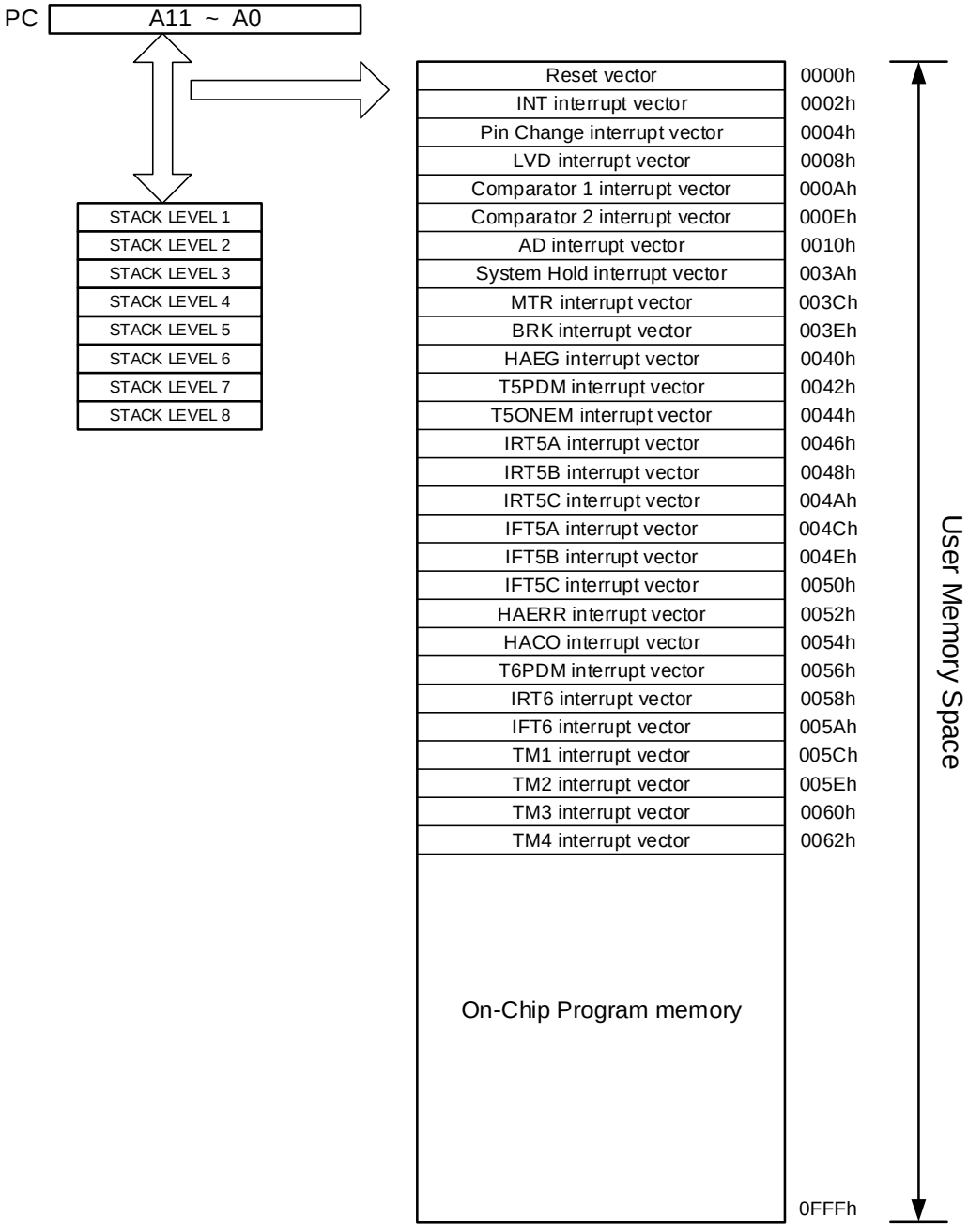


Figure 6-1 Program Counter Organization

Address	Bank 0	Bank 1	Bank 2	Bank 3
0X00	IAR (Indirect Addressing Register)			
0X01	BSR (Bank Selection Control Register)			
0X02	PCL (Program Counter Low)			
0X03	SR (Status Register)			
0X04	RSR (RAM Selection Reg.)			
0X05	Port 5	Reserved	TM1CR1	EIOPWMPE0
0X06	Port 6	Reserved	TM1CR2	EOPWMPE0
0X07	Port 7	Reserved	TM1DBH	EIOPHAPE
0X08	Reserved	P5PHCR	TM1DBL	Reserved
0X09	Reserved	P6PHCR	TM1DAH	T5CRH
0X0A	Reserved	P7PHCR	TM1DAL	T5CRL
0x0B	IOCR5	P5PLCR	TM2CR1	T6CRH
0X0C	IOCR6	P6PLCR	TM2CR2	T6CRL
0X0D	IOCR7	P7PLCR	TM2DBH	PWMCR1H
0X0E	OMCR	P5HDSCR	TM2DBL	PWMCR1L
0X0F	EIESCR	P6HDSCR	TM2DAH	PWMCR2H
0X10	WUCR1	P7HDSCR	TM2DAL	PWMCR2L
0X11	Reserved	P5ODCR	TM3CR1	T5OPMS
0X12	WUCR3	P6ODCR	TM3CR2	T6OPMS
0X13	Reserved	P7ODCR	TM3DBH	ASPWM
0X14	SFR1	Reserved	TM3DBL	LVPWM
0X15	Reserved	Reserved	TM3DAH	SLPWM
0X16	Reserved	Reserved	TM3DAL	COPH
0X17	SFR4	Reserved	TM4CR1	COPL
0X18	Reserved	Reserved	TM4CR2	MCOPH
0X19	SFR6	Reserved	TM4DBH	MCOPL
0X1A	Reserved	Reserved	TM4DBL	T5DECR
0X1B	IMR1	Reserved	TM4DAH	T5DEB
0X1C	Reserved	Reserved	TM4DAL	HACRH
0X1D	Reserved	Reserved	EI01NCR	HACRL
0X1E	IMR4	Reserved	CMP1CR	BRKCR1H
0X1F	Reserved	Reserved	CMP2CR	BRKCR1L
0X20	IMR6	Reserved	Reserved	BRKCR2H
0X21	WDTCR	Reserved	Reserved	BRKCR2L
0X22	Reserved	Reserved	CMPESCR	TRADCR

Address	Bank 0	Bank 1	Bank 2	Bank 3
0X23	Reserved	Reserved	CMP12NCR	TSF1H
0X24	Reserved	Reserved	Reserved	TSF1L
0X25	Reserved	Reserved	CMPTCR1	SETM1H
0X26	Reserved	Reserved	CMPTCR2	SETM1L
0X27	Reserved	Reserved	TCMP1H	RSTM1H
0X28	Reserved	Reserved	TCMP1L	RSTM1L
0X29	Reserved	Reserved	Reserved	Reserved
0X2A	Reserved	Reserved	Reserved	Reserved
0x2B	Reserved	Reserved	THCMP2H	T5VALH
0X2C	Reserved	Reserved	TLCMP2H	T5VALL
0X2D	Reserved	Reserved	THCMP2L	T5PDH
0X2E	Reserved	Reserved	TLCMP2L	T5PDL
0X2F	Reserved	Reserved	Reserved	T5ACDH
0X30	Reserved	Reserved	Reserved	T5ACDL
0X31	Reserved	Reserved	Reserved	T5BCDH
0X32	Reserved	Reserved	Reserved	T5BCDL
0X33	Reserved	Reserved	Reserved	T5CCDH
0X34	Reserved	Reserved	Reserved	T5CCDL
0X35	Reserved	Reserved	Reserved	T5ACDMH
0X36	Reserved	Reserved	Reserved	T5ACDML
0X37	Reserved	Reserved	Reserved	T5BCDMH
0X38	Reserved	Reserved	Reserved	T5BCDML
0X39	Reserved	Reserved	Reserved	T5CCDMH
0X3A	Reserved	Reserved	Reserved	T5CCDML
0x3B	Reserved	Reserved	Reserved	TRAD1VH
0X3C	Reserved	Reserved	Reserved	TRAD1VL
0X3D	Reserved	Reserved	Reserved	TRAD2VH
0X3E	ADCR1	Reserved	Reserved	TRAD2VL
0X3F	Reserved	Reserved	Reserved	T6VALH
0X40	ADISR	Reserved	Reserved	T6VALL
0X41	ADER1	Reserved	Reserved	T6PDH
0X42	Reserved	Reserved	Reserved	T6PDL
0X43	ADDL	Reserved	Reserved	T6CDH
0X44	ADDH	FLKR	Reserved	T6CDL
0X45	ADCVL	TBPTL	Reserved	T6CDMH

Address	Bank 0	Bank 1	Bank 2	Bank 3
0X46	ADCVH	TBPTH	Reserved	T6CDML
0X47	ADCONBUF	STKMON	LOCKPR	Reserved
0X48	Reserved	PCH	LOCKCR	Reserved
0X49	Reserved	LVDCR	Reserved	Reserved
0X4A	Reserved	Reserved	Reserved	Reserved
0x4B	Reserved	Reserved	Reserved	Reserved
0X4C	Reserved	Reserved	Reserved	SFR9
0X4D	Reserved	TBWCR	Reserved	SFR10
0X4E	Reserved	TBWAL	Reserved	IMR9
0X4F	Reserved	TBWAH	Reserved	IMR10
0X50	**General Purpose Register**			
0X51 . . . 0x7E				
0X7F				
0X80	Bank 0	Bank 1		
0X81 . . . 0XFE				
0XFF				

Figure 6-2 Data Memory Configuration

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	N	OV	T	P	Z	DC	C
F	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/RETI instructions

Bit 6 (N): Negative flag

The negative flag stores the state of the most significant bit of the output result

0: The result of the operation is not negative

1: The result of the operation is negative

Bit 5 (OV): Overflow flag.

OV is set when a two-complement overflow occurs as a result of an operation

0: No overflow occurred

1: Overflow occurred

Bit 4 (T): Time-out bit

Set to “1” with "SLEP" and "WDTC" commands, or during power-up and reset to 0 by WDT time-out.

Bit 3 (P): Power down bit

Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

C is set when a carry occurs and cleared when a borrow occurs during an arithmetic operation. The setting and clearing of a carry flag bit depends on the operation that is performed

For ADD, ADC, INC, and INCA instructions

0: No carry occurs

1: Carry occurs

For SUB, SUBB, DEC, DECA, and NEG instructions

0: Borrow occurs

1: No borrow occurs

For RLC, RRC, RLCA, and RRCA instructions

The Carry flag is used as a link between the least significant bit (LSB) and the most significant bit (MSB).

6.1.5 R4: RSR (RAM Select Register)

Bits 7~0 (RSR7~RSR0): used to select registers (Address: 00~FF) in the indirect address mode. Figure 6-2 shows the configuration of the data memory in detailed.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.1.6 Bank 0 R5 ~ R7: (Port 5 ~ Port 7)

R5, R6 and R7 are I/O data registers.

6.1.7 Bank 0 R8 ~ RA: (Reserved)

6.1.8 Bank 0 RB: IOCR5 (I/O Port 5 Control Register)

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance (default)

6.1.9 Bank 0 RC: IOCR6 (I/O Port 6 Control Register)

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance (default)

6.1.10 Bank 0 RD: IOCR7 (I/O Port 7 Control Register)

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance (default)

6.1.11 Bank 0 RE: OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	CLK2	CLK1	CLK0	-	RCM1	RCM0
R/W	R/W	R/W	R/W	R/W	0	R/W	R/W

Bit 7 (CPUS): CPU Oscillator Source Select.

0: Fs: sub-oscillator

1: Fm: main-oscillator (default)

When CPUS = 0, the CPU oscillator selects a sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit will decide the mode of SLEP instruction.

0: "IDLE=0"+SLEP instruction → sleep mode

1: "IDLE=1"+SLEP instruction → idle mode (default)

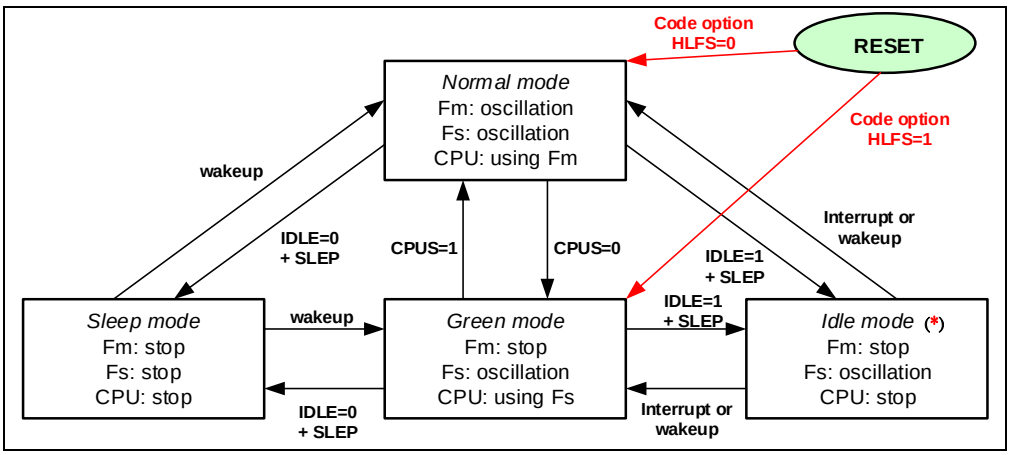


Figure 6-3 CPU Operation Mode

Note

(*) Switching Operation Mode from Idle → Normal, Idle → Green

If the clock source of the timer is Fs, the timer/counter will continue to count in Idle mode. When the matching condition of the timer/counter occurs during Idle mode, the interrupt flag of the Timer/Counter will be active. The MCU will jump to the interrupt vector when the corresponding interrupt is enabled.

Oscillation Characteristics

HLFS=0 (Normal)

Fmain	Fsub	Power-on LVR	Pin-Reset / WDT	
			N / G / I	S
RC 20M, 24M 28M, 32M	RC	16ms + WSTO + (8 or 16)*1/Fsub	WSTO + (8 or 16)*1/Fsub	WSTO + (8 or 16)*1/Fsub

HLFS=1 (Green)

Fmain	Fsub	Power-on LVR	Pin-Reset / WDT	
			N / G / I	S
RC 20M,24M, 28M, 32M	RC	16ms + WSTO + 8*1/Fsub	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub

Fmain	Fsub	G → N	I → N	S → N
RC 20M, 24M 28M, 32M	RC	WSTO + (8 or 16)*1/Fsub	WSTO + (8 or 16)*1/Fsub	WSTO + (8 or 16)*1/Fsub

Fmain	Fsub	I → G	S → G
RC	RC	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub

N: Normal mode *WSTO: Waiting Time from Start-to-Oscillation*
G: Green mode *I: Idle mode* *S: Sleep mode*

Bits 5~3: Instruction period option bits

CLK2	CLK1	CLK0	Scale of Main Clock
0	0	0	/2 (Default)
0	0	1	/4
0	1	0	/8
0	1	1	/16
1	0	0	/32
1	0	1	/64

Bits 2~0 (RCM2~RCM0): Internal RC mode select bits

RCM1	RCM0	Frequency (MHz)
0	0	20 (Default)
0	1	24
1	0	28
1	1	32

6.1.12 Bank 0 RF: EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EIES1	EIES0	-	-
0	0	0	0	R/W	R/W	0	0

Bits 7~4: Not used, set to "0" all the time

Bit 3 (EIES1): external interrupt edge select bit

0: falling edge interrupt

1: rising edge interrupt

Bit 2 (EIES0): external interrupt edge select bit

0: falling edge interrupt

1: rising edge interrupt

Bits 1~0: Not used, set to "0" all the time

6.1.13 Bank 0 R10: WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2WK	CMP1WK	LVDWK	ADWK	INT1WK	INT0WK	-	-
R/W	R/W	R/W	R/W	R/W	R/W	0	0

Bit 7 (CMP2WK): Comparator 2 Wake-up Enable Bit

0: Disable Comparator 2 wake-up

1: Enable Comparator 2 wake-up

Bit 6 (CMP1WK): Comparator 1 Wake-up Enable Bit

0: Disable Comparator 1 wake-up

1: Enable Comparator 1 wake-up

Bit 5 (LVDWK): Low Voltage Detect Wake-up Enable Bit

0: Disable Low Voltage Detect wake-up

1: Enable Low Voltage Detect wake-up

Bit 4 (ADWK): A/D Converter Wake-up Function Enable Bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

NOTE

When AD Complete status is used to enter the interrupt vector or to wake up the IC from sleep/idle with AD conversion running, the ADWK bit must be set to "Enable".

Bit 3 (INT1WK): External Interrupt (INT1 pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

Bit 2 (INT0WK): External Interrupt (INT0 pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

NOTE

When the External Interrupt status changed is used to enter the interrupt vector or to wake-up the IC from sleep/idle, the INTxWK bits must be set to "Enable".

Bits 1~0: Not used, set to "0" all the time

6.1.14 Bank 0 R11: (Reserved)

6.1.15 Bank 0 R12: WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ICWKP7	ICWKP6	ICWKP5	-	-	-	-
0	R/W	R/W	R/W	0	0	0	0

Bit 7: Not used, set to "0" all the time

Bits 6~4 (ICWKP7~ICWKP5): pin change wake-up enable for Port 7, 6, or 5.

0: disable wake-up function

1: enable wake-up function

Bits 3~0: Not used, set to "0" all the time

NOTE

When the MCU wakes up from sleep or idle mode, the PxICSF must be equal to 1. If PxICSF is equal to 0, it means the pin status doesn't change or the pin change PxICIE is disabled, hence the MCU cannot be awakened.

6.1.16 Bank 0 R13: (Reserved)

6.1.17 Bank 0 R14: SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2SF	CMP1SF	LVDSF	ADSF	EXSF1	EXSF0	-	-
F	F	F	F	F	F	0	0

Each corresponding status flag is set to "1" when an interrupt condition is triggered.

Bit 7 (CMP2SF): Comparator 2 status flag, reset by software.

Bit 6 (CMP1SF): Comparator 1 status flag, reset by software.

Bit 5 (LVDSF): Low Voltage Detector status flag.

LVDEN	BORS1, BORS0	LVD Voltage Interrupt Level	LVDSF
1	00	3.0V	1*
1	01	4.1V	1*
1	10	4.7V	1*
0	xx	NA	0

* If VDD has crossover at the LVD voltage interrupt level as VDD varies, LVDSF =1.

Bit 4 (ADSF): Status flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bit 3 (EXSF1): External Interrupt 1 Status flag.

Bit 2 (EXSF0): External Interrupt 0 Status flag.

Bits 1~0: Not used, set to “0” all the time

NOTE

If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.

6.1.18 Bank 0 R15~R16: (Reserved)

6.1.19 Bank 0 R17: SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	P7ICSF	P6ICSF	P5ICSF	-	-	-	-
0	F	F	F	0	0	0	0

Bit 7: Not used, set to "0" all the time

Bit 6 (P7ICSF): Port 7 input status change status flag. Set when Port 7 input changes, reset by software.

Bit 5 (P6ICSF): Port 6 input status change status flag. Set when Port 6 input changes, reset by software.

Bit 4 (P5ICSF): Port 5 input status change status flag. Set when Port 5 input changes, reset by software.

Bits 3~0: Not used, set to "0" all the time

NOTE

If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.

6.1.20 Bank 0 R18: (Reserved)

6.1.21 Bank 0 R19: SFR6 (Status Flag Register 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHSF	-	-	-	-	-	-	-
F	0	0	0	0	0	0	0

Bit 7 (SHSF): System hold status flag, Set when a system hold occurs, reset by software.

Bits 6~0: Not used, set to "0" all the time

6.1.22 Bank 0 R1A: (Reserved)

6.1.23 Bank 0 R1B: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	CMP1IE	LVDIE	ADIE	EXIE1	EXIE0	-	-
R/W	R/W	R/W	R/W	R/W	R/W	0	0

Bit 7 (CMP2IE): CMP2SF interrupt enable bit.

0: Disable CMP2SF interrupt

1: Enable CMP2SF interrupt.

Bit 6 (CMP1IE): CMP1SF interrupt enable bit.

0: Disable CMP1SF interrupt

1: Enable CMP1SF interrupt.

Bit 5 (LVDIE): LVDSF interrupt enable bit.

0: Disable LVDSF interrupt

1: Enable LVDSF interrupt

Bit 4 (ADIE): ADSF interrupt enable bit.

0: Disable ADSF interrupt

1: Enable ADSF interrupt.

Bit 3 (EXIE1): EXSF1 interrupt enable and **INT1 function enable bit.**

0: P52/INT1/TM4/2W_SCL is P52/TM4/2W_SCL pin,
EXSF1 always equals to 0.

1: Enable EXSF1 Interrupt and P52/INT1/TM4/2W_SCL is INT pin

Bit 2 (EXIE0): EXSF0 interrupt enable and **INT0 function enable bit.**

0: P60/INT0/TM3/2W_SDA is P60/TM3/2W_SDA pin,
EXSF0 always equals 0.

1: Enable EXSF0 Interrupt and P60/INT0/TM3/2W_SDA is INT pin

Bits 1~0: Not used, set to "0" all the time

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.24 Bank 0 R1C~R1D: (Reserved)

6.1.25 Bank 0 R1E: IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	P7ICIE	P6ICIE	P5ICIE	-	-	-	-
0	R/W	R/W	R/W	0	0	0	0

Bit 7: Not used, set to "0" all the time.

Bit 6 (P7ICIE): P7ICSF interrupt enable bit.

0: Disable P7ICSF interrupt

1: Enable P7ICSF interrupt

Bit 5 (P6ICIE): P6ICSF interrupt enable bit.

0: Disable P6ICSF interrupt

1: Enable P6ICSF interrupt

Bit 4 (P5ICIE): P5ICSF interrupt enable bit.

0: Disable P5ICSF interrupt

1: Enable P5ICSF interrupt

Bits 3~0: Not used, set to "0" all the time.

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter would jump into corresponding interrupt vector when the corresponding status flag is set.

6.1.26 Bank 0 R1F: (Reserved)

6.1.27 Bank 0 R20: IMR6 (Interrupt Mask Register 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHIE	-	-	-	-	-	-	-
R/W	0	0	0	0	0	0	0

Bit 7 (SHIE): SHSF Interrupt Enable Bit.

0: Disable SHSF interrupt

1: Enable SHSF interrupt

Bits 6~0: Not used, set to "0" all the time.

6.1.28 Bank 0 R21: WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
R/W	0	0	0	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer Enable Bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bits 6~4: Not used, set to "0" all the time.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1

1: Prescaler enable bit. WDT rate is set at Bit 2~0.

Bits 2~0 (WPSR2~WPSR0): WDT Prescaler Bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.29 Bank 0 R22~3D: (Reserved)

6.1.30 Bank 0 R3E: ADCR1 (ADC Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (CKR2~0): Clock Rate Select of ADC

System Mode	CKR2~0	Clock Rate	Max. System Operation Frequency in 3.0~3.8V	Max. System Operation Frequency in 3.8~4.5V	Max. System Operation Frequency in 4.5~5.5V
Normal Mode	000	$F_{HIRC}/16$	20 MHz	-	32 MHz
	001	$F_{HIRC}/8$	20 MHz	28 MHz	32 MHz
	010	$F_{HIRC}/4$	-	-	20 MHz
	011	$F_{HIRC}/2$	-	-	-
	100	$F_{HIRC}/64$	20 MHz	28 MHz	32 MHz
	101	$F_{HIRC}/32$	20 MHz	28 MHz	32 MHz
	110	$F_{HIRC}/6$	-	20 MHz	32 MHz
	111	F_{Sub}	Fs	Fs	Fs
Green Mode	xxx	F_{Sub}	Fs	Fs	Fs

NOTE

For the system operation frequency, users must refer to Table 13 in Section 6.13.

Bit 4 (ADRUN): ADC Starts to Run

In single mode:

0: Reset upon the completion of the conversion by hardware, this bit cannot be reset by software.

1: A/D conversion starts. This bit can be set by software

In Continuous Mode:

0: ADC is stopped.

1: ADC is running unless this bit is reset by software

Bit 3 (ADP): ADC Power

0: ADC is in power down mode.

1: ADC is operating normally.

Bit 2 (ADOM): ADC Operation Mode Select

0: ADC operates in single mode.

1: ADC operates in continuous mode.

Bits 1~0 (SHS1~0): Sample and Hold Timing Select

SHS[1:0]	Sample and Hold Timing
00	2 x T_{AD}
01	4 x T_{AD}
10	8 x T_{AD}
11	12 x T_{AD}

NOTE

When the comparator trim mode is enabled, the ADCR1[ADP] will be cleared.

6.1.31 Bank 0 R3F: ADCR2 (ADC Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	VPIS2	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
0	R/W	R/W	R/W	R/W	R/W	R/W	0

Bit 7: Not used, set to "0" all the time.

Bit 5 (ADIM): ADC Interrupt Mode

0: Normal mode. Interrupt occurred after AD conversion is completed.

1: Compare mode. Interrupt occurred when comparison result conforms the setting of ADCMS bits.

Bit 4 (ADCMS): ADC Comparison Mode Select.

In compare mode:

0: Interrupt occurs when AD conversion data is greater than the data in ADCD register.

It means when ADD > ADCD, interrupt occurs.

1: Interrupt occurs when AD conversion data is less than the data in ADCD register.

It means when ADD < ADCD, interrupt occurs.

In Normal Mode:

No effect

Bits 6, 3 ~ 2 (VPIS2~0): Internal Positive Reference Voltage Select.

VPIS[2]	VPIS[1:0]	Reference Voltage
0	00	AVDD
0	01	4.096 V
0	10	3.072 V
0	11	2.048 V
1	11	2.560 V

Bit 1 (VREFP): Positive Reference Voltage Select

0: Internal positive reference voltage. The actual voltage is set by VPIS[1:0] bits

1: From VREF pin.

Bit 0: Not used, set to "0" all the time.

NOTE

When using internal voltage reference, users need to wait at least 50 µs the first time to enable and stabilize the internal voltage reference circuit. After that, users only need to wait 6 µs (the least) when switching voltage references.

6.1.32 Bank 0 R40: ADISR (Analog to Digital Converter Input Channel Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STPMK	-	-	-	ADIS3	ADIS2	ADIS1	ADIS0
R/W	0	0	0	R/W	R/W	R/W	R/W

Bit 7 (STPMK): Stop Mask for ADC buffer mode.

0: Stop

1: Turn

Bits 6~4: Not used, set to "0" all the time.

Bits 3~0 (ADIS4~0): ADC input channel select bits

ADIS[3:0]	Selected Channel
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5
0110	NA
0111	NA
1xxx	1/2 VDD PowerDet.

NOTE

For internal signal source, users only need to set ADIS3=1 for these AD input channels are instantly active. Internal Vref stable time is 4 μs.

6.1.33 Bank 0 R41: ADER1 (Analog to Digital Converter Input Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used, set to "0" all the time.

Bit 5 (ADE5): AD converter enable bit of P57 pin.

0: Disable ADC5, P57/ADC5 act as I/O pin

1: Enable ADC5, act as analog input pin

Bit 4 (ADE4): AD converter enable bit of P62 pin.

0: Disable ADC4, P62/ADC4 /C2- acts as I/O or C2- pin

1: Enable ADC4, act as analog input pin

Bit 3 (ADE3): AD converter enable bit of P71 pin.

0: Disable ADC3, P71/ADC3/RCOUT acts as I/O or RCOUT pin

1: Enable ADC3, act as analog input pin

Bit 2 (ADE2): AD converter enable bit of P70 pin.

0: Disable ADC2, P70/ADC2 acts as I/O pin

1: Enable ADC2, act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P66 pin.

0: Disable ADC1, P66/TM2/ADC1/C1-/RESET acts as I/O or TM2 or C1- or RESET pin

1: Enable ADC1, act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P67 pin.

0: Disable ADC0, P67/PWME/TM1/ADC0/C1+ acts as I/O or PWME or TM1 or C1+ pin

1: Enable ADC0, act as analog input pin

6.1.34 Bank 0 R42: (Reserved)

6.1.35 Bank 0 R43: ADDL (Low Byte of Analog to Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
R	R	R	R	R	R	R	R

Bits 7~0 (ADD7~0): Low Byte of AD Data Buffer

6.1.36 Bank 0 R44: ADDH (High Byte of Analog to Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
R	R	R	R	R	R	R	R

Bits 7~0 (ADD15~8): High Byte of AD Data Buffer.

The format of AD data is dependent on code option ADFM.

ADFM			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	0	ADDH					ADD11	ADD10	ADD9	ADD8
		ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	1	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		ADDL					ADD3	ADD2	ADD1	ADD0

6.1.37 Bank 0 R45: ADCVL (Low Byte of Analog to Digital Converter Comparison)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (ADCD7~0): Low Byte Data for AD Comparison.

6.1.38 Bank 0 R46: ADCVH (High Byte of Analog to Digital Converter Comparison)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCD15	ADCD14	ADCD13	ADCD12	ADCD11	ADCD10	ADCD9	ADCD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (ADCD15~8): High Byte Data for AD Comparison

NOTE

Users should use ADCVL and ADCVH data formats as the same as ADDH and ADDL registers. Otherwise, faulty results will be obtained after AD comparison.

6.1.39 Bank 0 R47: ADCONBUF (ADC Control Register for Buffer Mode)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADBFEN	ADBFOVR	ADBFINT	-	-	ADBFPTR2	ADBFPTR1	ADBFPTR0
R/W	R/W	R/W	0	0	R/W	R/W	R/W

Bit 7 (ADBFEN): ADC Buffer Mode Enable

0: Disable ADC buffer mode

1: Enable ADC buffer mode

Bit 6 (ADBFOVR): Indicator of Buffer Overrun

ADBFOVR is set when ADBFEN=1 and internal buffer is overwrite

0: No internal buffer overwrite occurred

1: Internal buffer overwrite occurred

H/W Set, S/W Reset

Bit 5 (ADBFINT): Indicator of Conversion interrupt

0: ADC Conversion is completed normally

1: ADC Conversion is interrupted by user

H/W Set, S/W Reset

Bits 4~3: Not used, set to 0 all the time.

Bits 2~0 (ADBFPTR2~0): Pointer of ADC Buffer

6.1.40 Bank 0 R48 ~ R4F: (Reserved)

6.1.41 Bank 1 R5 ~ R7: (Reserved)

6.1.42 Bank 1 R8: P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PH57): Control bit used to enable pull-high of the P57 pin

0: Enable internal pull-high

1: Disable internal pull-high (default)

Bit 6 (PH56): Control bit used to enable pull-high of the P56 pin

Bit 5 (PH55): Control bit used to enable pull-high of the P55 pin

Bit 4 (PH54): Control bit used to enable pull-high of the P54 pin

Bit 3 (PH53): Control bit used to enable pull-high of the P53 pin

Bit 2 (PH52): Control bit used to enable pull-high of the P52 pin

Bit 1 (PH51): Control bit used to enable pull-high of the P51 pin

Bit 0 (PH50): Control bit used to enable pull-high of the P50 pin

6.1.43 Bank 1 R9: P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PH67): Control bit used to enable pull-high of the P67 pin

0: Enable internal pull-high

1: Disable internal pull-high (default)

Bit 6 (PH66): Control bit used to enable pull-high of the P66 pin

Bit 5 (PH65): Control bit used to enable pull-high of the P65 pin

Bit 4 (PH64): Control bit used to enable pull-high of the P64 pin

Bit 3 (PH63): Control bit used to enable pull-high of the P63 pin

Bit 2 (PH62): Control bit used to enable pull-high of the P62 pin

Bit 1 (PH61): Control bit used to enable pull-high of the P61 pin

Bit 0 (PH60): Control bit used to enable pull-high of the P60 pin

6.1.44 Bank 1 RA: P7PHCR (Port 7 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	P7LPH
0	0	0	0	0	0	0	R/W

Bits 7~2: Not used, set to "0" all the time.

Bit 0 (P7LPH): Control bit used to enable the pull-high of Port 7 low nibble pin

0: Enable internal pull-high

1: Disable internal pull-high (default)

6.1.45 Bank 1 RB: P5PLCR (Port 5 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PL57): Control bit used to enable pull-low of the P57 pin

0: Enable internal pull-low

1: Disable internal pull-low (default)

Bit 6 (PL56): Control bit used to enable pull-low of the P56 pin

Bit 5 (PL55): Control bit used to enable pull-low of the P55 pin

Bit 4 (PL54): Control bit used to enable pull-low of the P54 pin

Bit 3 (PL53): Control bit used to enable pull-low of the P53 pin

Bit 2 (PL52): Control bit used to enable pull-low of the P52 pin

Bit 1 (PL51): Control bit used to enable pull-low of the P51 pin

Bit 0 (PL50): Control bit used to enable pull-low of the P50 pin

6.1.46 Bank 1 RC: P6PLCR (Port 6 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PL67): Control bit used to enable pull-low of the P67

0: Enable internal pull-low

1: Disable internal pull-low (default)

Bit 6 (PL66): Control bit used to enable pull-low of the P66 pin

Bit 5 (PL65): Control bit used to enable pull-low of the P65 pin

Bit 4 (PL64): Control bit used to enable pull-low of the P64 pin

Bit 3 (PL63): Control bit used to enable pull-low of the P63 pin

Bit 2 (PL62): Control bit used to enable pull-low of the P62 pin

Bit 1 (PL61): Control bit used to enable pull-low of the P61 pin

Bit 0 (PL60): Control bit used to enable pull-low of the P60 pin

6.1.47 Bank 1 RD: P789APLCR (Ports 7~A Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	P7LPL
0	0	0	0	0	0	0	R/W

Bits 7~1: Not used, set to "0" all the time.

Bit 0 (P7LPL): Control bit used to enable pull-low of the Port 7 low nibble pin

0: Enable internal pull-low

1: Disable internal pull-low (default)

6.1.48 Bank 1 RE: P5HDSCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H57	H56	H55	H54	H53	H52	H51	H50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H57~H50): P57~P50 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink (default)

6.1.49 Bank 1 RF: P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H67	H66	H65	H64	H63	H62	H61	H60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H67~H60): P67~P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink (default)

6.1.50 Bank 1 R10: P789AHDSCR (Ports 7~A High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	P7LHDS
0	0	0	0	0	0	0	R/W

Bits 7~1: Not used, set to "0" all the time.

Bit 0 (P7LHDS): Control bit used to enable high drive/sink of Port 7 low nibble pin

1: Disable high drive/sink (default)

0: Enable high drive/sink

6.1.51 Bank 1 R11: P5ODCR (Port 5 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD57~OD50): Open-Drain control bits

0: Disable open-drain function (default)

1: Enable open-drain function

6.1.52 Bank 1 R12: P6ODCR (Port 6 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD67~OD60): Open-Drain control bits

0: Disable open-drain function (default)

1: Enable open-drain function

6.1.53 Bank 1 R13: P789AODCR (Ports 7~A Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	P7LOD
0	0	0	0	0	0	0	R/W

Bits 7~1: Not used, set to "0" all the time.

Bit 0 (P7LOD): Control bit used to enable open-drain of Port A low nibble pin

0: Disable open-drain function (default)

1: Enable open-drain function

6.1.54 Bank 1 R14 ~ R43: (Reserved)

6.1.55 Bank 1 R44: FLKR (Flash Key Register for Table Write Use)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FLK7	FLK5	FLK5	FLK4	FLK3	FLK2	FLK1	FLK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This FLKR register is used by table write IAP mode operation. The IAP enable signal is generated when a specific value is written into this register, e.g., **0xB4**. The register is designed to make sure that IAP operation occurs for flash update.

6.1.56 Bank 1 R45: TBPTL (Table Point Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB7~TB0): Table Point Address Bits 7~0.

6.1.57 Bank 1 R46: TBPTH (Table Point High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	RDS	-	-	TB11	TB10	TB9	TB8
R/W	R/W	0	0	R/W	R/W	R/W	R/W

Bit 7 (HLB): Take Hi Byte or Low Byte content of Flash ROM addressed by TPBTH and TPBTL.

RDS	HLB	Read to Register Data Value Description
0	0	Read Low Byte
0	1	Read Hi Byte

Bit 6 (RDS): ROM data select bit.

0: ROM data (Must be 0 all the time)

Bits 5~4: Not used, set to "0" all the time.

Bits 3 ~0 (TB11~TB8): Table Point Address Bits 11~8.

6.1.58 Bank 1 R47: STKMON (Stack Point)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOV	-	-	-	-	STL2	STL1	STL0
R	0	0	0	0	R	R	R

Bit 7 (STOV): Stack pointer overflow indication bit. Read-only.

Bits 6~3: Not used, set to "0" all the time.

Bits 2~0 (STL2~ STL 0): Stack pointer number. Read-only.

6.1.59 Bank 1 R48: PCH (Program Counter High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PC11	PC10	PC9	PC8
0	0	0	0	R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time.

Bits 3~0 (PC11~PC8): The low byte of program counter.

6.1.60 Bank 1 R49: LVDCR (Low Voltage Detector Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDEN	-	-	-	LVDB	-	-	-
R/W	0	0	0	R	0	0	0

Bit 7 (LVDEN): Low Voltage Detector Enable Bit

0: Disable low voltage detector

1: Enable low voltage detector

LVDEN	BORS1, BORS0	LVD Voltage Interrupt Level	LVDB
1	10	VDD < 4.7V	0
		VDD > 4.8V	1
1	01	VDD < 4.1V	0
		VDD > 4.2V	1
1	00	VDD < 3.0V	0
		VDD > 3.1V	1
0	XX	NA	1

Bit 3 (LVDB): Low Voltage Detector State Bit. This is a read-only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by Code Option BORS1~BORS0), this bit will be cleared.

0: The low voltage is detected.

1: The low voltage is not detected or LVD function is disabled.

Bits 6~4, 2~0: Not used, set to "0" all the time.

6.1.61 Bank 1 R4D: TBWCR (Table Write Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	IAPEN
0	0	0	0	0	0	0	R/W

Bits 7~1: Not used bits, fixed to “0” all the time.

Bit 0 (IAPEN): IAP enable bit

0: IAP mode Disable

1: IAP mode Enable

6.1.62 Bank 1 R4E: TBWAL (Table Write Start Address Low Byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBWA7	TBWA6	TBWA5	TBWA4	TBWA3	TBWA2	TBWA1	TBWA0
R/W	R/W	R/W	R	R	R	R	R

Bits 7~0 (TBWA7~TBWA0): Table Write Star Address Bits 7~0, TBWA4~TBWA0 are always fixed to “0”.

6.1.63 Bank 1 R4F: TBWAH (Table Write Start Address High Byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	TBWA11	TBWA10	TBWA9	TBWA8
0	0	0	0	R/W	R/W	R/W	R/W

Bits 7~4: Fixed to “0” all the time (Read only)

Bits 3~0 (TBWA11~TBWA8): Table Write Address Bits 11~8.

6.1.64 Bank 2 R5: TM1CR1 (Timer 1 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1S	TM1RC	TM1SS1	-	TM1FF	TM1MOS	TM1IS1	TM1IS0
R/W	R/W	R/W	0	R/W	R/W	R/W	R/W

Bit 7 (TM1S): Timer/Counter 1 Start Control Bit

0: Stop and clear counter (default)

1: Start

Bit 6 (TM1RC): Timer 1 Read Control Bit

0: When this bit is set to 0, no data can be read from TM1DB (default)

1: When this bit is set to 1, data read from TM1DB is a number of counting

Bit 5 (TM1SS1): Timer 1 Read Control Bit

0: Internal clock as count source (Fc)- Fs/Fm (default)

1: External TM1 pin as count source (Fc). It is used only in timer/counter mode

Bit 4: Not used bits, fixed to "0" all the time

Bit 3 (TM1FF): Inversion for Timer/counter as PWM or PDO mode

0: Duty is Logic 1 (default)

1: Duty is Logic 0

Bit 2 (TM1MOS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One–shot mode

Bits 1~0 (TM1IS1~TM1IS0): Timer 1 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode

TM1IS1	TM1IS0	Timer 1 Interrupt Type Select
0	0	TM1DA (period) matching
0	1	TM1DB(duty) matching
1	x	TM1DA and TM1DB matching

6.1.65 Bank 2 R6: TM1CR2 (Timer 1 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1M2	TM1M1	TM1M0	TM1SS0	TM1CK3	TM1CK2	TM1CK1	TM1CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (TM1M2~TM1M0): Timer 1 operation mode select

TM1M2	TM1M1	TM1M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of clock source must be 50/50)

Bit 4 (TM1SS0): Timer 1 clock source select bit

0: The Fs is used as count source (Fc) (default)

1: The Fm is used as count source (Fc)

Bits 3~0 (TM1CK3~TM1CK0): Timer 1 clock source prescaler select

TM1CK3	TM1CK2	TM1CK1	TM1CK0	Clock Source	Resolution 32 MHz	Max time 32 MHz	Resolution 16 kHz	Max time 16 kHz
				Normal	F_C=32M	F_C=32M	F_C=16K	F_C=16K
0	0	0	0	F_C	31.25ns	2048µs	62.5µs	4.096s
0	0	0	1	$F_C/2$	62.5ns	4096µs	125µs	8.192s
0	0	1	0	$F_C/2^2$	125ns	8192µs	250µs	16.384s
0	0	1	1	$F_C/2^3$	250ns	16384µs	500µs	32.768s
0	1	0	0	$F_C/2^4$	500ns	32768µs	1ms	65.536s
0	1	0	1	$F_C/2^5$	1µs	65536µs	2ms	131.072s
0	1	1	0	$F_C/2^6$	2µs	131072µs	4ms	262.144s
0	1	1	1	$F_C/2^7$	4µs	262144µs	8ms	524.288s
1	0	0	0	$F_C/2^8$	8µs	524.288ms	16ms	1048.58s
1	0	0	1	$F_C/2^9$	16µs	1.048s	32ms	2097.15s
1	0	1	0	$F_C/2^{10}$	32µs	2.097s	64ms	4194.3s
1	0	1	1	$F_C/2^{11}$	64µs	4.194s	128ms	8388.6s
1	1	0	0	$F_C/2^{12}$	128µs	8.389s	256ms	16777s
1	1	0	1	$F_C/2^{13}$	256µs	16.777s	512ms	33554s
1	1	1	0	$F_C/2^{14}$	512µs	33.554s	1.024s	67108s
1	1	1	1	$F_C/2^{15}$	1.024ms	67.109s	2.048s	134217s

6.1.66 Bank 2 R7: TM1DBH (High Byte of Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DB15	TM1DB14	TM1DB13	TM1DB12	TM1DB11	TM1DB10	TM1DB9	TM1DB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7~0 (TM1DB15~TM1DB8): Data buffer B of 16-bit timer 1

6.1.67 Bank 2 R8: TM1DBL (Low byte of Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DB7	TM1DB6	TM1DB5	TM1DB4	TM1DB3	TM1DB2	TM1DB1	TM1DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM1DB7~TM1DB0): Data buffer B of 16-bit Timer 1

6.1.68 Bank 2 R9: TM1DAH (High bytes of Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DA15	TM1DA14	TM1DA13	TM1DA12	TM1DA11	TM1DA10	TM1DA9	TM1DA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM1DA15~TM1DA8): Data buffer A of 16-bit Timer 1

6.1.69 Bank 2 RA: TM1DAL (Low bytes of Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DA7	TM1DA6	TM1DA5	TM1DA4	TM1DA3	TM1DA2	TM1DA1	TM1DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM1DA7~TM1DA0): Data buffer A of 16-bit Timer 1

NOTE

1. *When TMx is used in PWM mode, the duty value stored at register TMxDB must be less than or equal to the period value stored at register TMxDA, i.e. duty ≦ period. The PWM waveform is then generated. If duty is greater than the period, the PWM output waveform remains at a **high** voltage level.*
2. *The period value set by users is extra plus 1 in inner circuit.*

   For example:

   If the period value is set as 0x4F, the circuit actually processes 0x50 period length.

   If the period value is set as 0xFF, the circuit actually processes 0x100 period length.
3. *When TMx is used in PWM mode, the TMxDAH, TMxDAL, TMxDBH and TMxDBL can be written at any time, but the data of TMxDA and TMxDB are latched only when writing to TMxDAL. Therefore, the new duty and new period of PWM will be updated at the last period–match.*

6.1.70 Bank 2 RB: TM2CR1 (Timer 2 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2S	TM2RC	TM2SS1	-	TM2FF	TM2MOS	TM2IS1	TM2IS0
R/W	R/W	R/W	0	R/W	R/W	R/W	R/W

Bit 7 (TM2S): Timer 2 Start Control Bit

0: Stop and clear counter (default)

1: Start

Bit 6 (TM2RC): Timer 2 Read Control Bit

0: When this bit is set to 0, no data can be read from TM1DB (default)

1: When this bit is set to 1, data read from TM1DB is a number of counting

Bit 5 (TM2SS1): Timer 2 Read Control Bit

0: Internal clock as count source (Fc)- Fs/Fm (default)

1: External TM2 pin as count source (Fc). It is used only for timer/counter mode

Bit 4: Not used bits, fixed to “0” all the time

Bit 3 (TM2FF): Inversion for Timer/counter as PWM or PDO mode

0: Duty is logic 1 (default)

1: Duty is logic 0

Bit 2 (TM2MOS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One–shot mode

Bits 1~0 (TM2IS1~TM2IS0): Timer 2 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode

TM2IS1	TM2IS0	Timer 2 Interrupt Type Select
0	0	TM2DA(period) matching
0	1	TM2DB(duty) matching
1	x	TM2DA and TM2DB matching

6.1.71 Bank 2 RC: TM2CR2 (Timer 2 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2M2	TM2M1	TM2M0	TM2SS0	TM2CK3	TM2CK2	TM2CK1	TM2CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (TM2M2~TM2M0): Timer 2 operation mode select

TM2M2	TM2M1	TM2M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of clock source must be 50/50)

Bit 4 (TM2SS0): Timer 2 clock source select bit

0: The Fs is used as count source (Fc) (default)

1: The Fm is used as count source (Fc)

Bits 3~0 (TM2CK3~TM2CK0): Timer 2 clock source prescaler select

TM2CK3	TM2CK2	TM2CK1	TM2CK0	Clock Source	Resolution 32 MHz	Max time 32 MHz	Resolution 16kHz	Max time 16kHz
				Normal	F_C=32M	F_C=32M	F_C=16K	F_C=16K
0	0	0	0	F_C	31.25ns	2048µs	62.5µs	4.096s
0	0	0	1	$F_C/2$	62.5ns	4096µs	125µs	8.192s
0	0	1	0	$F_C/2^2$	125ns	8192µs	250µs	16.384s
0	0	1	1	$F_C/2^3$	250ns	16384µs	500µs	32.768s
0	1	0	0	$F_C/2^4$	500ns	32768µs	1ms	65.536s
0	1	0	1	$F_C/2^5$	1µs	65536µs	2ms	131.072s
0	1	1	0	$F_C/2^6$	2µs	131072µs	4ms	262.144s
0	1	1	1	$F_C/2^7$	4µs	262144µs	8ms	524.288s
1	0	0	0	$F_C/2^8$	8µs	524.288ms	16ms	1048.58s
1	0	0	1	$F_C/2^9$	16µs	1.048s	32ms	2097.15s

TM2CK3	TM2CK2	TM2CK1	TM2CK0	Clock Source	Resolution 32 MHz	Max time 32 MHz	Resolution 16kHz	Max time 16kHz
				Normal	F_C=32M	F_C=32M	F_C=16K	F_C=16K
1	0	1	0	$F_C/2^{10}$	32us	2.097s	64ms	4194.3s
1	0	1	1	$F_C/2^{11}$	64us	4.194s	128ms	8388.6s
1	1	0	0	$F_C/2^{12}$	128us	8.389s	256ms	16777s
1	1	0	1	$F_C/2^{13}$	256us	16.777s	512ms	33554s
1	1	1	0	$F_C/2^{14}$	512us	33.554s	1.024s	67108s
1	1	1	1	$F_C/2^{15}$	1.024ms	67.109s	2.048s	134217s

6.1.72 Bank 2 RD: TM2DBH (High Byte of Timer 2 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2DB15	TM2DB14	TM2DB13	TM2DB12	TM2DB11	TM2DB10	TM2DB9	TM2DB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM2DB15~TM2DB8): Data Buffer B of Timer 2

6.1.73 Bank 2 RE: TM2DBL (Low Byte of Timer 2 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2DB7	TM2DB6	TM2DB5	TM2DB4	TM2DB3	TM2DB2	TM2DB1	TM2DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM2DB7~TM2DB0): Data Buffer B of Timer 2

6.1.74 Bank 2 RF: TM2DAH (High Bytes of Time 2 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2DA15	TM2DA14	TM2DA13	TM2DA12	TM2DA11	TM2DA10	TM2DA9	TM2DA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM2DA15~TM2DA8): Data Buffer A of Timer 2

6.1.75 Bank 2 R10: TM2DAL (Low Bytes of Timer 2 Data Buffer A) (Last Update)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2DA7	TM2DA6	TM2DA5	TM2DA4	TM2DA3	TM2DA2	TM2DA1	TM2DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM1DA7~TM1DA0): Data Buffer A of 16 bit Timer 2

6.1.76 Bank 2 R11: TM3CR1 (Timer 3 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3S	TM3RC	TM3SS1	-	TM3FF	TM3MOS	TM3IS1	TM3IS0
R/W	R/W	R/W	0	R/W	R/W	R/W	R/W

Bit 7 (TM3S): Timer 3 Start Control Bit

0: Stop and clear counter (default)

1: Start

Bit 6 (TM3RC): Timer 3 Read Control Bit

0: When this bit is set to 0, no data can be read from TM3DB (default)

1: When this bit is set to 1, data read from TM3DB is a number of counting

Bit 5 (TM3SS1): Timer 3 Read Control Bit

0: Internal clock as count source (Fc) - Fs/Fm (default)

1: External TM3 pin as count source (Fc). It is used only for timer/counter mode

Bit 4: Not used bits, fixed to “0” all the time

Bit 3 (TM3FF): Inversion for Timer/counter as PWM or PDO mode

0: Duty is Logic 1 (default)

1: Duty is Logic 0

Bit 2 (TM3MOS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One–shot mode

Bits 1~0 (TM3IS1~TM3IS0): Timer 3 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode

TM3IS1	TM3IS0	Timer 3 Interrupt Type Select
0	0	TM3DA(period) matching
0	1	TM3DB(duty) matching
1	x	TM3DA and TM3DB matching

6.1.77 Bank 2 R12: TM3CR2 (Timer 3 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3M2	TM3M1	TM3M0	TM3SS0	TM3CK3	TM3CK2	TM3CK1	TM3CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (TM3M2~TM3M0): Timer 3 operation mode select

TM3M2	TM3M1	TM3M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of clock source must be 50/50)

Bit 4 (TM3SS0): Timer 3 clock source select bit

0: The Fs is used as count source (Fc) (default)

1: The Fm is used as count source (Fc)

Bits 3~0 (TM3CK3~TM3CK0): Timer 3 clock source prescaler select

TM3CK3	TM3CK2	TM3CK1	TM3CK0	Clock Source	Resolution 32 MHz	Max. Time 32 MHz	Resolution 16 kHz	Max. Time 16 kHz
				Normal	F_C=32M	F_C=32M	F_C=16K	F_C=16K
0	0	0	0	F_C	31.25ns	2048µs	62.5µs	4.096s
0	0	0	1	$F_C/2$	62.5ns	4096µs	125µs	8.192s
0	0	1	0	$F_C/2^2$	125ns	8192µs	250µs	16.384s
0	0	1	1	$F_C/2^3$	250ns	16384µs	500µs	32.768s
0	1	0	0	$F_C/2^4$	500ns	32768µs	1ms	65.536s
0	1	0	1	$F_C/2^5$	1µs	65536µs	2ms	131.072s
0	1	1	0	$F_C/2^6$	2µs	131072µs	4ms	262.144s
0	1	1	1	$F_C/2^7$	4µs	262144µs	8ms	524.288s
1	0	0	0	$F_C/2^8$	8µs	524.288ms	16ms	1048.58s
1	0	0	1	$F_C/2^9$	16µs	1.048s	32ms	2097.15s

TM3CK3	TM3CK2	TM3CK1	TM3CK0	Clock Source	Resolution 32 MHz	Max. Time 32 MHz	Resolution 16kHz	Max. Time 16 kHz
				Normal	F_C=32M	F_C=32M	F_C=16K	F_C=16K
1	0	1	0	$F_C/2^{10}$	32μs	2.097s	64ms	4194.3s
1	0	1	1	$F_C/2^{11}$	64μs	4.194s	128ms	8388.6s
1	1	0	0	$F_C/2^{12}$	128μs	8.389s	256ms	16777s
1	1	0	1	$F_C/2^{13}$	256μs	16.777s	512ms	33554s
1	1	1	0	$F_C/2^{14}$	512μs	33.554s	1.024s	67108s
1	1	1	1	$F_C/2^{15}$	1.024ms	67.109s	2.048s	134217s

6.1.78 Bank 2 R13: TM3DBH (High Byte of Timer 3 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3DB15	TM3DB14	TM3DB13	TM3DB12	TM3DB11	TM3DB10	TM3DB9	TM3DB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM3DB15~TM3DB8): Data Buffer B of Timer 3

6.1.79 Bank 2 R14: TM3DBL (Low Byte of Timer 3 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3DB7	TM3DB6	TM3DB5	TM3DB4	TM3DB3	TM3DB2	TM3DB1	TM3DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM3DB7~TM3DB0): Data Buffer B of Timer 3

6.1.80 Bank 2 R15: TM3DAH (High Byte of Timer 3 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3DA15	TM3DA14	TM3DA13	TM3DA12	TM3DA11	TM3DA10	TM3DA9	TM3DA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM3DA15~TM3DA8): Data Buffer A of Timer 3

6.1.81 Bank 2 R16: TM3DAL (Low Byte of Timer 3 Data Buffer A) (Last Update)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3DA7	TM3DA6	TM3DA5	TM3DA4	TM3DA3	TM3DA2	TM3DA1	TM3DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM3DA7~TM3DA0): Data Buffer A of Timer 3

6.1.82 Bank 2 R17: TM4CR1 (Timer 4 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4S	TM4RC	TM4SS1	-	TM4FF	TM4MOS	TM4IS1	TM4IS0
R/W	R/W	R/W	0	R/W	R/W	R/W	R/W

Bit 7 (TM4S): Timer 4 Start Control Bit

0: Stop and clear counter (default)

1: Start

Bit 6 (TM4RC): Timer 4 Read Control Bit

0: When this bit is set to 0, no data can be read from TM4DB (default)

1: When this bit is set to 1, data read from TM4DB is a number of counting

Bit 5 (TM4SS1): Timer 4 Read Control Bit

0: Internal clock as count source (Fc) - Fs/Fm (default)

1: External TM4 pin as count source (Fc). It is used only for timer/counter mode

Bit 4: Not used bits, fixed to “0” all the time

Bit 3 (TM3FF): Inversion for Timer/counter as PWM or PDO mode

0: Duty is logic 1 (default)

1: Duty is logic 0

Bit 2 (TM4MOS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One–shot mode

Bits 1~0 (TM4IS1~TM4IS0): Timer 4 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode

TM4IS1	TM4IS0	Timer 4 Interrupt Type Select
0	0	TM4DA (period) matching
0	1	TM4DB (duty) matching
1	x	TM4DA and TM3DB matching

6.1.83 Bank 2 R18: TM4CR2 (Timer 4 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4M2	TM4M1	TM4M0	TM4SS0	TM4CK3	TM4CK2	TM4CK1	TM4CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (TM4M2~TM4M0): Timer 4 operation mode select

TM4M2	TM4M1	TM4M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of clock source must be 50/50)

Bit 4 (TM4SS0): Timer 4 clock source select bit

0: The Fs is used as count source (Fc) (default)

1: The Fm is used as count source (Fc)

Bits 3~0 (TM4CK3~TM4CK0): Timer 4 clock source prescaler select.

TM4CK3	TM4CK2	TM4CK1	TM4CK0	Clock Source	Resolution 32 MHz	Max. Time 32 MHz	Resolution 16 kHz	Max. Time 16 kHz
				Normal	F_C=32M	F_C=32M	F_C=16K	F_C=16K
0	0	0	0	F_C	31.25ns	2048µs	62.5µs	4.096s
0	0	0	1	$F_C/2$	62.5ns	4096µs	125µs	8.192s
0	0	1	0	$F_C/2^2$	125ns	8192µs	250µs	16.384s
0	0	1	1	$F_C/2^3$	250ns	16384µs	500µs	32.768s
0	1	0	0	$F_C/2^4$	500ns	32768µs	1ms	65.536s
0	1	0	1	$F_C/2^5$	1µs	65536µs	2ms	131.072s
0	1	1	0	$F_C/2^6$	2µs	131072µs	4ms	262.144s
0	1	1	1	$F_C/2^7$	4µs	262144µs	8ms	524.288s
1	0	0	0	$F_C/2^8$	8µs	524.288ms	16ms	1048.58s
1	0	0	1	$F_C/2^9$	16µs	1.048s	32ms	2097.15s
1	0	1	0	$F_C/2^{10}$	32µs	2.097s	64ms	4194.3s
1	0	1	1	$F_C/2^{11}$	64µs	4.194s	128ms	8388.6s
1	1	0	0	$F_C/2^{12}$	128µs	8.389s	256ms	16777s
1	1	0	1	$F_C/2^{13}$	256µs	16.777s	512ms	33554s
1	1	1	0	$F_C/2^{14}$	512µs	33.554s	1.024s	67108s
1	1	1	1	$F_C/2^{15}$	1.024ms	67.109s	2.048s	134217s

6.1.84 Bank 2 R19: TM4DBH (High Byte of Timer 4 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4DB15	TM4DB14	TM4DB13	TM4DB12	TM4DB11	TM4DB10	TM4DB9	TM4DB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM4DB15~TM4DB8): Data Buffer B of timer 4

6.1.85 Bank 2 R1A: TM4DBL (Low Byte of Timer 4 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4DB7	TM4DB6	TM4DB5	TM4DB4	TM4DB3	TM4DB2	TM4DB1	TM4DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM4DB7~TM4DB0): Data Buffer B of Timer 4

6.1.86 Bank 2 R1B: TM4DAH (High Byte of Timer 4 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4DA15	TM4DA14	TM4DA13	TM4DA12	TM4DA11	TM4DA10	TM4DA9	TM4DA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM4DA15~TM4DA8): Data Buffer B of Timer 4

6.1.87 Bank 2 R1C: TM4DAL (Low Byte of Timer 4 Data Buffer A) (Last Update)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4DA7	TM4DA6	TM4DA5	TM4DA4	TM4DA3	TM4DA2	TM4DA1	TM4DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM4DA7~TM4DA0): Data Buffer A of Timer 4

6.1.88 Bank 2 R1D: EI01NCR (External Interrupt 0, 1 Noise Rejection Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EI1NRE	-	EI1NR1	EI1NR0	EI0NRE	-	EI0NR1	EI0NR0
R/W	0	R/W	R/W	R/W	0	R/W	R/W

Bit 7 (EI1NRE): Noise rejection enable of External Interrupt 1

Bit 6: Not used. Set to 0 all the time

Bits 5~4 (EI1NR1~ EI1NR0): Delay time select for noise rejection of External Interrupt 1

EI1NR1	EI1NR0	Function Description
0	0	8 x (1 / F_{HIRC})
0	1	16 x (1 / F_{HIRC})
1	0	32 x (1 / F_{HIRC})
1	1	64 x (1 / F_{HIRC})

Bit 3 (EI1NRE): Noise rejection enable of External Interrupt 0

Bit 2: Not used. set to 0 all the time

Bits 1~0 (EI0NR1~ EI0NR0): Delay time select for noise rejection of External Interrupt 0

EI0NR1	EI0NR0	Function Description
0	0	8 x (1 / F_{HIRC})
0	1	16 x (1 / F_{HIRC})
1	0	32 x (1 / F_{HIRC})
1	1	64 x (1 / F_{HIRC})

6.1.89 Bank 2 R1E: CMP1CR (Comparator 1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C1PRS1	C1PRS0	C1NRS1	C1NRS0	-	CMP1EN	CMP1OE	CP1OUT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6 (C1PRS1~C1PRS0): Reference source select for noninverting terminal of Comparator 1

C1PRS1	C1PRS0	Function Description
0	0	C1+ is connected to pad(default)
0	1	C1+ is connected to Internal reference (1.25V)
1	0	NA
1	1	NA

Bits 5~4 (C1NRS1~C1NRS0): Reference source select for inverting terminal of Comparator 1

C1NRS1	C1NRS0	Function Description
0	0	C1- is connected to pad(default)
0	1	C1- is connected to Internal reference (1.25V)
1	0	NA
1	1	NA

Bit 3: Not used, set to 0 all the time.

Bit 2 (CMP1EN): Power of Compare 1

0: Disable (default)

1: Enable

Bit 1 (CMP1OE): Compare 1 output control

0: Disable (default)

1: Enable, compare 1 output connect to C1OUT

Bit 0 (CP1OUT): The result of the comparator 1 out

6.1.90 Bank 2 R1F: CMP2CR (Comparator 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2PRS1	C2PRS0	C2NRS1	C2NRS0	HYSEN2	CMP2EN	CMP2OE	CP2OUT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6 (C2PRS1~C2PRS0): Reference source select for noninverting terminal of Comparator 2

C2PRS1	C2PRS0	Function Description
0	0	C2+ is connected to pad (default)
0	1	C2+ is connected to Internal reference (1.25V)
1	0	NA
1	1	NA

Bits 5~4 (C2NRS1~C2NRS0): Reference source select for inverting terminal of Comparator 2

C2NRS1	C2NRS0	Function Description
0	0	C2- is connected to pad (default)
0	1	C2- is connected to Internal reference (1.25V)
1	0	NA
1	1	NA

Bit 3 (HYSEN2): Input Hysteresis Enable.

0: Disable (default)

1: Enable

Bit 2 (CMP2EN): Power of Comparator 2

0: Disable (default)

1: Enable

Bit 1 (CMP2OE): Comparator 2 output control

0: Disable (default)

1: Enable, Comparator 2 output connects to C2OUT

Bit 0 (CP2OUT): The result of the Comparator 2 output

6.1.91 Bank 2 R20~R21: (Reserved)

6.1.92 Bank 2 R22: CMPESCR (Interrupt Triggering Type of Comparator Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	CMP2ES	CMP1ES
0	0	0	0	0	0	R/W	R/W

Bits 7~2: Not used. Set to 0 all the time

Bit 1 (CMP2ES): Interrupt trigger type of comparator 2 edge select bit

0: Falling edge interrupt

1: Rising edge interrupt (default)

Bit 0 (CMP1ES): Interrupt trigger type of comparator 1 edge select bit

0: Falling edge interrupt

1: Rising edge interrupt (default)

6.1.93 Bank 2 R23: CMP12NCR (Comparator 1, 2 Noise Rejection Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CO2NRE	-	CO2NR1	CO2NR0	CO1NRE	-	CO1NR1	CO1NR0
R/W	0	R/W	R/W	R/W	0	R/W	R/W

Bit 7 (CO2NRE): Noise rejection enable of compare 2 output

0: Disable noise rejection (default)

1: Enable noise rejection

Note that in Green, Idle and Sleep mode, the noise rejection circuit is always disabled.

Bit 6: Not used, set to 0 all the time

Bits 5~4 (CO2NR1~ CO2NR0): Delay time select for noise rejection of Comparator 2 output

CO2NR1	CO2NR0	Function Description
0	0	8 x (1 / F_{HIRC})
0	1	16 x (1 / F_{HIRC})
1	0	32 x (1 / F_{HIRC})
1	1	64 x (1 / F_{HIRC})

Bit 3 (CO1NRE): Noise Rejection Enable of Compare 1 output

0: Disable noise rejection (default)

1: Enable noise rejection

Note that in Green, Idle and Sleep mode, the noise rejection circuit is always disabled.

Bit 2: Not used, set to 0 all the time

Bits 1~0 (CO1NR1~ CO1NR0): Delay Time Select for Noise Rejection of Comparator 1 Output

CO1NR1	CO1NR0	Function Description
0	0	8 x (1 / F_{HIRC})
0	1	16 x (1 / F_{HIRC})
1	0	32 x (1 / F_{HIRC})
1	1	64 x (1 / F_{HIRC})

6.1.94 Bank 2 R24: (Reserved)

6.1.95 Bank 2 R25: CMPTCR1 (Comparator Trim Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPTEN	TVRS2	TVRS1	TVRS0	-	-	TRIMDU2	TRIMDU1
R/W	R/W	R/W	R/W	0	0	R/W	R/W

Bit 7 (CMPTEN): Comparator trim mode enable

0: Normal Mode (default)

1: Trim Mode

When CMPTEN is set, ADC peripheral will be disabled.

Bits 6~4 (TVRS2~ TVRS0): Trim Voltage Reference Select of Comparator 2

TRIMIS2	TVRS2	TVRS1	TVRS0	Hysteresis Offset (mV) *B.G.=4V	Note
0	0	0	0	10	Trim Low Side
0	0	0	1	20	
0	0	1	0	30	
0	0	1	1	39	
0	1	0	0	49	
0	1	0	1	59	
0	1	1	0	69	
0	1	1	1	79	
1	0	0	0	10	Trim High Side
1	0	0	1	20	
1	0	1	0	30	
1	0	1	1	40	
1	1	0	0	50	
1	1	0	1	60	
1	1	1	0	70	
1	1	1	1	80	

The reference source from bandgap, voltage of bandgap is controlled by VPIS[2:0]

Bits 3~2: Not used, set to 0 all the time

Bit 1 (TRIMDU2): Trim resolution of Comparator 2

0: High resolution (default)

1: Low resolution

Bit 0 (TRIMDU1): Trim resolution of Comparator 1

0: High resolution (default)

1: Low resolution

6.1.96 Bank 2 R26: CMPTCR2 (Comparator Trim Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	TRIMOS	-	-	TRIMIS2	TRIMIS1
0	0	0	R/W	0	0	R/W	R/W

Bits 7~5: Not used, set to 0 all the time

Bit 4 (TRIMOS): Trim mode output select of comparator 2

0: Low Channel (default)

1: High Channel

Bits 3~2: Not used. Set to 0 all the time

Bit 1(TRIMIS2): Trim Mode Input Select of Comparator 2

0: Low Side (default)

1: High Side

Bit 0 (TRIMIS1): Trim Mode Input Select of Comparator 1

0: Low Side (default)

1: High Side

In trim mode, low side is trimmed first, then high side.

6.1.97 Bank 2 R27: TCMP1H (Trim Comparator 1 High Side)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCMP1HS	-	-	TCMP1H4	TCMP1H3	TCMP1H2	TCMP1H1	TCMP1H0
R/W	0	0	R/W	R/W	R/W	R/W	R/W

Bit 7 (TCMP1HS): The trimmed sign bit of high-side Comparator 1

Bits 6~5: Not used, set to 0 all the time

Bits 4~0 (TCMP1H4~TCMP1H0): The trimmed bits of high-side Comparator 1

6.1.98 Bank 2 R28: TCMP1L (Trim Comparator 1 Low Side)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCMP1LS	-	-	TCMP1L4	TCMP1L3	TCMP1L2	TCMP1L1	TCMP1L0
R/W	0	0	R/W	R/W	R/W	R/W	R/W

Bit 7 (TCMP1LS): The trimmed sign bit of low-side Comparator 1

Bits 6~5: Not used. Set to 0 all the time

Bits 4~0 (TCMP1L4~TCMP1L0): The trimmed bits of low-side Comparator 1

6.1.99 Bank 2 R29~R2A: (Reserved)

6.1.100 Bank 2 R2B: THCMP2H (Trim High Side of Comparator 2 High Channel)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
THCMP2HS	-	THCMP2H5	THCMP2H4	THCMP2H3	THCMP2H2	THCMP2H1	THCMP2H0
R/W	0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (THCMP2HS): The trimmed sign bit of high-side Comparator 2 high channel

Bit 6: Not used. Set to 0 all the time

Bits 5~0 (THCMP2H5~THCMP2H0): The trimmed bits of high-side Comparator 2 high channel

6.1.101 Bank 2 R2C: TLCMP2H (Trim Low Side of Comparator 2 High Channel)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TLCMP2HS	-	TLCMP2H5	TLCMP2H4	TLCMP2H3	TLCMP2H2	TLCMP2H1	TLCMP2H0
R/W	0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (TLCMP2HS): The trimmed sign bit of low-side Comparator 2 high channel

Bit 6: Not used. Set to 0 all the time

Bits 5~0 (TLCMP2H5~TLCMP2H0): The trimmed bits of low-side Comparator 2 high channel

6.1.102 Bank 2 R2D: THCMP2L (Trim High Side of Comparator 2 Low Channel)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
THCMP2LS	-	THCMP2L5	THCMP2L4	THCMP2L3	THCMP2L2	THCMP2L1	THCMP2L0
R/W	0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (THCMP2LS): The trimmed sign bit of high-side Comparator 2 low channel

Bit 6: Not used. Set to 0 all the time

Bits 5~0 (THCMP2L5~THCMP2L0): The trimmed bits of high-side Comparator 2 low channel

6.1.103 Bank 2 R2E: TLCMP2L (Trim Low Side of Comparator 2 Low Channel)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TLCMP2LS	-	TLCMP2L5	TLCMP2L4	TLCMP2L3	TLCMP2L2	TLCMP2L1	TLCMP2L0
R/W	0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (TLCMP2LS): The trimmed sign bit of low-side Comparator 2 low channel

Bit 6: Not used, set to 0 all the time

Bits 5~0 (TLCMP2L5~TLCMP2L0): The trimmed bits of low-side Comparator 2 low channel

6.1.104 Bank 2 R2F~R3F: (Reserved)

6.1.105 Bank 2 R40 MULMOD (Mode Control for Multiplier)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	PROD16	MACEN	MACM	SMCAND	SMIER
0	0	0	R	R/W	R/W	R/W	R/W

Bits 7~5: Not used. Set to 0 all the time

Bit 4 (PROD16): Bit 16 of Multiplier Product

Bit 3 (MACEN): Accumulator Enable, this bit can enable multiplication and accumulation functions

0: Disable accumulation function for multiplier

1: Enable accumulation function for multiplier

Bit 2 (MACM): Accumulator Mode Select

0: Multiplication and Addition, accumulator = product + accumulator

1: Multiplication and Subtraction, accumulator = accumulator – product

Bit 1 (SMCAND): Signed or unsigned select bit of the Multiplicand (Constant or Register)

0: Multiplicand is unsigned

1: Multiplicand is signed

Bit 0 (SMIER): Signed or unsigned select bit of the Multiplier (ACC)

0: Multiplier is unsigned

1: Multiplier is signed

6.1.106 Bank 2 R41 PRODH (High Byte of Multiplier Product)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PROD15	PROD14	PROD13	PROD12	PROD11	PROD10	PROD9	PROD8
0	0	0	R	R/W	R/W	R/W	R/W

Bits 7~0 (PROD15~PROD8): Bits 15~8 of multiplier product

6.1.107 Bank 2 R42 PRODL (Low Byte of Multiplier Product)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PROD7	PROD6	PROD5	PROD4	PROD3	PROD2	PROD1	PROD0
0	0	0	R	R/W	R/W	R/W	R/W

Bits 7~0 (PROD7~PROD0): Bits 7~0 of multiplier product

6.1.108 Bank 2 R43 SFR7 (Status Flag Register 7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4DBSF	-	-	-	TM4SF	TM3SF	TM2SF	TM1SF
R/W	0	0	0	R/W	R/W	R/W	R/W

Each corresponding status flag is set to "1" when an interrupt condition is triggered.

Bits 7 (TM4DBSF): 16-bit capture 4 status flag, cleared by software

Bits 6~4: Not used, set to 0 all the time

Bit 3 (TM4SF): 16-bit timer/counter 4 status flag, cleared by software

Bit 2 (TM3SF): 16-bit timer/counter 3 status flag, cleared by software

Bit 1 (TM2SF): 16-bit timer/counter 2 status flag, cleared by software

Bit 0 (TM1SF): 16-bit timer/counter 1 status flag, cleared by software

6.1.109 Bank 2 R44: (Reserved)

6.1.110 Bank 2 R45 IMR7 (Interrupt Mask Register 7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	TM4IE	TM3IE	TM2IE	TM1IE
0	0	0	0	R/W	R/W	R/W	R/W

Bits 7~4: Not used. Set to 0 all the time

Bit 3 (TM4IE): TM4SF interrupt enable bit.

0: Disable TM4SF interrupt

1: Disable TM4SF interrupt

Bit 2 (TM3IE): TM3SF interrupt enable bit.

0: Disable TM3SF interrupt

1: Disable TM3SF interrupt

Bit 1 (TM2IE): TM2SF interrupt enable bit.

0: Disable TM2SF interrupt

1: Disable TM2SF interrupt

Bit 0 (TM1IE): TM1SF interrupt enable bit.

0: Disable TM1SF interrupt

1: Disable TM1SF interrupt

6.1.111 Bank 2 R46: (Reserved)

6.1.112 Bank 2 R47 LOCKPR (Lock Page Number Register))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOCKPR7	LOCKPR6	LOCKPR5	LOCKPR4	LOCKPR3	LOCKPR2	LOCKPR1	LOCKPR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (LOCKPR7~ LOCKPR0): Lock Page Number

6.1.113 Bank 2 R48 LOCKCR (Lock Control Register))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOCKEN	-	-	-	-	-	-	-
R/W	0	0	0	0	0	0	0

Bit 7 (LOCKEN): Enhanced Protect Control Bit

0: Enable

1: Disable (default)

Bits 6~0: Not used. Set to 0 all the time

6.1.114 Bank 2 R49~R4F: (Reserved)

6.1.115 Bank 3 R5 EIOPWMPE0 (External IO Pins Functional Select for PWM Port Enable 0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PWMCBEN	PWMCEN	PWMBBEN	PWMBEN	PWMABEN	PWMAEN
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used. Set to 0 all the time

Bit 5 (PWMCBEN): PWMCB enable bit.

0: PWMCB is off (default)

1: PWMCB is on

Bit 4 (PWMCEN): PWMCB enable bit.

0: PWMC is off (default)

1: PWMC is on

Bit 3 (PWMBBEN): PWMBB enable bit.

0: PWMBB is off (default)

1: PWMBB is on

Bit 2 (PWMBEN): PWMB enable bit.

0: PWMB is off (default)

1: PWMB is on

Bit 1 (PWMABEN): PWMAB enable bit.

0: PWMAB is off (default)

1: PWMAB is on

Bit 0 (PWMAEN): PWMA enable bit.

0: PWMA is off (default)

1: PWMA is on

6.1.116 Bank 3 R6 EOPWMPE0 (External I/O Pins Functional Select for PWM Port Enable 0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PWMEEN	PWMEOE	-	-	-	-
0	0	R/W	R/W	0	0	0	0

Bits 7~6: Not used. Set to 0 all the time

Bit 5 (PWMEEN): PWME pin enable bit.

0: PWME is off (default)

1: PWME is on, and its related pin is automatically set by PWMEOE.

Bit 4 (PWMEOE): PWME output enable bit.

0: PWM mode Disable, Capture or Compare mode Enable, PWME is set to Input

1: PWM mode Enable, PWME is set to output

Bits 3~0: Not used. Set to 0 all the time

6.1.117 Bank 3 R7 EIOPHAPE (External IO Pins Functional Select for EHAx Port Enable)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	HACEN1	HACEN0	HABEN1	HABEN0	HAAEN1	HAAEN0
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used. Set to 0 all the time

Bits 5~4 (HACEN1~ HACEN0): HAC pin enable bit.

HACEN1	HACEN0	Mode
0	0	EHAC is off (Default), and its related pin carries out I/O pin function.
0	1	EHAC is on ,EHAC set to input.
1	0	EHAC is off , and its related pin carries out I/O pin function.
1	1	EHAC is off , and its related pin carries out I/O pin function.

Bits 3~2 (HABEN1~ HABEN0): HAB pin enable bit.

HABEN1	HABEN0	Mode
0	0	EHAB is off (Default), and its related pin carries out I/O pin function.
0	1	EHAB is on ,EHAB set to input.
1	0	EHAB is off , and its related pin carries out I/O pin function.
1	1	EHAB is off , and its related pin carries out I/O pin function.

Bits 1~0 (HAAEN1~ HAAEN0): HAA pin enable bit.

HAAEN1	HAAEN0	Mode
0	0	EHAA is off (Default), and its related pin carries out I/O pin function.
0	1	EHAA is on, EHAA set to input.
1	0	CP2OUT trigger HAA, EHAA is off and its related pin carries out I/O pin function.
1	1	EHAA is off, and its related pin carries out I/O pin function.

6.1.118 Bank 3 R8: (Reserved)

6.1.119 Bank 3 R9 T5CRH (High Byte of Timer 5 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5SP	T5CLR	T5CKS1	T5CKS0	T5PRE3	T5PRE2	T5PRE1	T5PRE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (T5SP): The single pulse Timer 5 control bit

0: Disable (default)

1: Single pulse mode is enable

After single pulse mode is finished, the T5RF is reset. Therefore, the PWMxSF (x =A ~ C) is reset.

Bit 6 (T5CLR): Timer 5 Clear

0: No action on Timer 5 (default)

1: The Timer 5 counter register is clear to zero immediately.

After finish clearing, T5CLR will be automatically reset to zero. T5CLR has no influence on T5RF.

Bits 5~4 (T5CKS1~ T5CKS0): This signal is used to select the clock source (t5_tmr_clk) for Timer 5

T5CKS1	T5CKS0	Function Description
0	0	F_{HIRC} (default)
0	1	Fm
1	0	NA
1	1	NA

Bits 3~0 (T5PRE3~ T5PRE0): Pre-scaler select

T5PRE3	T5PRE2	T5PRE1	T5PRE0	Function Description
0	0	0	0	t5_tmr_clk / 1
0	0	0	1	t5_tmr_clk / 2
0	0	1	0	t5_tmr_clk / 4
0	0	1	1	t5_tmr_clk / 8
0	1	0	0	t5_tmr_clk / 16
0	1	0	1	t5_tmr_clk / 32
0	1	1	0	t5_tmr_clk / 64
0	1	1	1	t5_tmr_clk / 128
1	0	0	0	t5_tmr_clk / 256
1	0	0	1	t5_tmr_clk / 512
1	0	1	0	t5_tmr_clk / 1024
1	0	1	1	t5_tmr_clk / 2048
1	1	x	x	Reserved

6.1.120 Bank 3 RA T5CRL (Low Byte of Timer 5 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5MS	T5CDIR	DECLR	FT6PRESEL	-	-	-	TMR5P
R/W	R	R/W	R/W	0	0	0	R/W

Bit 7 (T5MS): Timer 5 operation mode select bit

0: Normal PWM Output mode. Timer 5 operates in up-count mode. (default)

1: Phase Correct PWM Output mode. Timer 5 operates in up-down-count mode.

Bit 6 (T5CDIR): Direction of counting for Timer 5

0: Count up

1: Count down

Bit 5 (DECLR): Dead Timer for PWMA, PWMB, and PWMC clear

0: No action on dead timer

1: The dead timer register is cleared to zero.

After finishing clearing, DECLR will be automatically reset to zero

Bit 4 (FT6PRESEL): Clock source select for timer 6

0: Depend on T6CKS

1: Depend on T5CKS

Bits 3~1: Not use set to 0 all the time

Bit 0 (TMR5P): Timer 5 module is powered-down by gating clock with this bit which should be used as an active-high power down control

0: Power down Timer 5 module clock

1: Enable Timer 5 module clock

6.1.121 Bank 3 RB T6CRH (High Byte of Timer 6 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6SP	T6CLR	T6CKS1	T6CKS0	T6PRE3	T6PRE2	T6PRE1	T6PRE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (T6SP): The single pulse Timer 6 control bit

0: Disable (default)

1: Single pulse mode is enable

After single pulse mode is finished, the T6RF is reset. Therefore, the PWME is reset.

Bit 6 (T6CLR): Timer 6 Clear

0: No action on Timer 6 (default)

1: The Timer 6 counter register is cleared to zero immediately. After finishing clearing, T6CLR will be automatically reset to zero. T6CLR has no influence on T6RF.

Bits 5~4 (T6CKS1~ T6CKS0): This signal is used to select the clock source (t6_tmr_clk) for Timer 6

T6CKS1	T6CKS0	Function Description
0	0	F_{HIRC} (default)
0	1	Fm
1	0	NA
1	1	NA

Bits 3~0 (T6PRE3~ T6PRE0): Pre-scaler select

T6PRE3	T6PRE2	T6PRE1	T6PRE0	Function Description
0	0	0	0	t6_tmr_clk / 1
0	0	0	1	t6_tmr_clk / 2
0	0	1	0	t6_tmr_clk / 4
0	0	1	1	t6_tmr_clk / 8
0	1	0	0	t6_tmr_clk / 16
0	1	0	1	t6_tmr_clk / 32
0	1	1	0	t6_tmr_clk / 64
0	1	1	1	t6_tmr_clk / 128
1	0	0	0	t6_tmr_clk / 256
1	0	0	1	t6_tmr_clk / 512
1	0	1	0	t6_tmr_clk / 1024
1	0	1	1	t6_tmr_clk / 2048
1	1	x	x	Reserved

6.1.122 Bank 3 RC T6CRL (Low Byte of Timer 6 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6TMS3	T6TMS2	T6TMS1	T6TMS0	T6TDIR1	T6TDIR0	RPHT6	TMR6P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~4 (T6TMS3~ T6TMS0): Timer 6 trigger mode select

T6TMS3	T6TMS2	T6TMS1	T6TMS0	Set T6RF
0	x	x	X	NA
1	0	0	0	Both edge of HAA, HAB, HAC
1	0	0	1	A period match of Timer 5
1	0	1	0	A zero match of Timer 5 (Phase Correct PWM mode). Don't care about T6TDIR bit.
1	0	1	1	A Timer 5 duty compare event on PWMA, PWMB or PWMC.*
1	1	0	0	A Timer 5 duty compare event on PWMA.*
1	1	0	1	A Timer 5 duty compare event on PWMB.*
1	1	1	0	A Timer 5 duty compare event on PWMC.*

*: It is independent on T6DIR for normal PWM mode.
And it is dependent on T6DIR for Phase Correct PWM mode.

Bits 3~2 (T6TDIR1~ T6TDIR0): Timer 6 Trigger mode with the Timer 5 duty compare event for phase correct mode

T6TDIR1	T6TDIR0	Timer 6 Trigger Direction
0	0	Independent of the count direction of Timer 5
0	1	When Timer 5 is counting down
1	0	When Timer 5 is counting up
1	1	Independent of the count direction of Timer 5

Bit 1 (RPHT6): PWME active state and passive state are switched each other

0: Switching disable (default)

1: Switching enable

Bit 0 (TMR6P): Timer 6 module is powered-down by gating clock with this bit which should be used as an active-high power down control

0: Power down Timer 6 module clock (default)

1: Enable Timer 6 module clock

6.1.123 Bank 3 RD PWMCR1H (High Byte of PWM Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	T6EPWMCB	T6EPWMC	T6EPWMBB	T6EPWMB	T6EPWMAB	T6EPWMA
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used. Set to 0 all the time

Bit 5 (T6EPWMCB): PWMCB is modulated by timer 6

0: Disable (default)

1: Enable

Bit 4 (T6EPWMC): PWMC is modulated by Timer 6

0: Disable (default)

1: Enable

Bit 3 (T6EPWMBB): PWMBB is modulated by Timer 6

0: Disable (default)

1: Enable

Bit 2 (T6EPWMB): PWMB is modulated by Timer 6

0: Disable (default)

1: Enable

Bit 1 (T6EPWMAB): PWMAB is modulated by timer 6

0: Disable (default)

1: Enable

Bit 0 (T6EPWMA): PWMA is modulated by timer 6

0: Disable (default)

1: Enable

6.1.124 Bank 3 RE PWMCR1L (Low Byte of PWM Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	T5EPWMCB	T5EPWMC	T5EPWMBB	T5EPWMB	T5EPWMAB	T5EPWMA
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used. Set to 0 all the time

Bit 5 (T5EPWMCB): PWMCB is modulated by Timer 5

0: Disable (default)

1: Enable

Bit 4 (T5EPWMC): PWMC is modulated by Timer 5

0: Disable (default)

1: Enable

Bit 3 (T5EPWMBB): PWMBB is modulated by Timer 5

0: Disable (default)

1: Enable

Bit 2 (T5EPWMB): PWMB is modulated by Timer 5

0: Disable (default)

1: Enable

Bit 1 (T5EPWMAB): PWMAB is modulated by Timer 5

0: Disable (default)

1: Enable

Bit 0 (T5EPWMA): PWMA is modulated by Timer 5

0: Disable (default)

1: Enable

6.1.125 Bank 3 RF PWMCR2H (High Byte of PWM Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPE	T6EPWME	CPMTE	-	-	TSYN2	TSYN1	TSYN0
R/W	R/W	R/W	0	0	R/W	R/W	R/W

Bit 7 (CPE): Composite PWM mode enable

0: Composite PWM mode disables (default)

1: The waveform of corresponding PWM output is modulated by bit CPWMxx (xx = A ~ C, AB ~ CB)

Bit 6 (T6EPWME): PWME is modulated by Timer 6

0: Disable (default)

1: Enable

Bit 5 (CPMTE): Mapping Transfer mode select for Composite PWM Mode.

0: Mapping transfer trigger decided by TSMS and TSYN.

1: Mapping transfer trigger decided by TSYN.

Bits 4~3: Not used. Set to 0 all the time

Bits 2~0 (TSYN2~TSYN0): Synchronization source for mapping transfer, once the mapping transfer happens, the MTSF bit is reset

TSYN2	TSYN1	TSYN0	Function Description
0	0	0	NA
0	0	1	Timer 5 (while counting up) triggers the mapping transfer
0	1	0	Timer 6 zero match triggers the mapping transfer
0	1	1	Direct; Once MTSF=1, the mapping transfer happens
1	0	0	Timer 5 one match (while counting down)
1	0	1	Timer 5 period match detected (while counting up)
1	1	0	Timer 6 period match detected (while counting up)
1	1	1	NA

6.1.126 Bank 3 R10 PWMCR2L (Low Byte of PWM Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MTSF	TSMS2	TSMS1	TSMS0	-	-	-	-
R	R/W	R/W	R/W	0	0	0	0

Bit 7 (MTSF): Mapping Trigger Source Flag

Bits 6~4 (TSMS2~TSMS0): Synchronization source for mapping transfer, once the mapping transfer happens, the MTSF bit is reset

TSMS2	TSMS1	TSMS0	Function Description
0	0	0	No trigger request will be generated
0	0	1	Timer 5 one match (while counting down)
0	1	0	Timer 5 period match detected (while counting up)
0	1	1	Timer 5 PWMA compare(duty) match detected(up counter)
1	0	0	Timer 5 PWMA compare (Duty) match detected(down counter)
1	0	1	Timer 6 compare (Duty) match detected
1	1	0	Timer 6 period match detected (while counting up)
1	1	1	Correct hall pattern on HAx detected

*: The mapping transfer is defined to that CPWMxx (xx = A ~ CB) is updated from MCPWMxx (xx = A ~ CB)

Bits 3~0: Not used. Set to 0 all the time

6.1.127 Bank 3 R11 T5OPMS (Timer 5 Operation Mode Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	T5CMS	-	T5BMS	-	T5AMS
0	0	0	R/W	0	R/W	0	R/W

Bits 7~5: Not used. Set to 0 all the time

Bit 4 (T5CMS): Timer 5C Mode Select

0: Timer mode (default)

1: PWM mode

Bit 3: Not used. Set to 0 all the time

Bit 2 (T5BMS): Timer 5B Mode Select

0: Timer mode (default)

1: PWM mode

Bit 1: Not used. Set to 0 all the time

Bit 0 (T5AMS): Timer 5A Mode Select

0: Timer mode (default)

1: PWM mode

6.1.128 Bank 3 R12 T6OPMS (Timer 6 Operation Mode Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6CMS3	T6CMS2	T6CMS1	T6CMS0	T6MS1	T6MS0	-	-
R/W	R/W	R/W	R/W	R/W	R/W	0	0

Bits 7~4 (T6CMS3~ T6CMS0): T6 Capture Mode Select

T6CMS3	T6CMS2	T6CMS1	T6CMS0	Function Description
0	0	0	0	If the rising edge is on PWME pin, the value of T6CD is copied to T6DCM and the present value of Timer 6 is saved to T6CD.
0	0	0	1	If the falling edge is on PWME pin, the value of T6CD is copied to T6CDM and the present value of Timer 6 is saved to T6CD
0	0	1	0	The present value of Timer 6 is saved to T6CD at rising edge of PMWE pin and saved to T6CDM at falling edge of PMWE pin
0	0	1	1	The present value of Timer 6 is saved to T5CD at falling edge of PMWE pin and saved to T5CDM at rising edge of PMWE pin
0	1	0	x	If the both edges (rising or falling) are on PWME pin, the value of T6CD is copied to T6CDM and the present value of Timer 6 is saved to T6CD
0	1	1	x	If both edges (Rising or Falling) are on HAA/HAB/HAC, the value of T6CD is copied to T6CDM and the present value of Timer 6 is saved to T6CD
1	0	0	0	The present value of Timer 6 is saved to T6CD at rising edge of PMWE pin and saved to T6CDM at rising edge of HAA/HAB/HAC pin
1	0	0	1	The present value of Timer 6 is saved to T6CD at falling edge of PMWE pin and saved to T6CDM at falling edge of HAA/HAB/HAC pin
1	0	1	x	The present value of Timer 6 is saved to T6CD at rising edge of PMWE pin and saved to T6CDM at falling edge of HAA/HAB/HAC pin
1	1	0	x	If the both edges (rising or falling) are on PWME pin, the present value of Timer 6 is saved to T6CD. If the both edges (rising or falling) are on HAA/HAB/HAC pin, the present value of Timer 6 is saved to T6CDM
1	1	1	x	If the falling edge is on PWME pin, the present value of Timer 6 is saved to T6CD. If the rising edgeis on HAA/HAB/HAC pin, the present value of Timer 6 is saved to T6CDM

Bits 3~2 (T6MS1~ T6MS0): Timer 6 Mode Select

T6MS1	T6MS0	Function Description
0	0	Timer mdoe
0	1	PWM mode
1	x	Capture mode

6.1.129 Bank 3 R13 ASPWM (PWM Active Status)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PWMCBAS	PWMCAS	PWMBBAS	PWMBAS	PWMABAS	PWMAAS
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used. Set to 0 all the time

Bit 5 (PWMCBAS): PWMCB Active States Select for Internal PWMCB Signal

0: The low state of PWMCS is active (default)

1: The high state of PWMCS is active

Bit 4 (PWMCAS): PWMC Active States Select for Internal PWMC Signal

0: The low state of PWMCS is active (default)

1: The high state of PWMCS is active

Bit 3 (PWMBBAS): PWMBB Active States Select for Internal PWMBB Signal

0: The low state of PWMBS is active (default)

1: The high state of PWMBS is active

Bit 2 (PWMBAS): PWMB Active States Select for Internal PWMB Signal

0: The low state of PWMBS is active (default)

1: The high state of PWMBS is active

Bit 1 (PWMABAS): PWMAB Active States Select for Internal PWMAB Signal

0: The low state of PWMAS is active (default)

1: The high state of PWMAS is active

Bit 0 (PWMAAS): PWMA Active States Select for Internal PWMA Signal

0: The low state of PWMAS is active (default)

1: The high state of PWMAS is active

6.1.130 Bank 3 R14 LVPWM (PWM Output Level Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PWMCBLV	PWMCLV	PWMBBLV	PWMBLV	PWMABLV	PWMALV
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used. Set to 0 all the time

Bit 5 (PWMCBLV): PWMCB Active States Level

0: Logic low level (default)

1: Logic high level

Bit 4 (PWMCLV): PWMC Active States Level

0: Logic low level (default)

1: Logic high level

Bit 3 (PWMBBLV): PWMBB Active States Level

0: Logic low level (default)

1: Logic high level

Bit 2 (PWMBLV): PWMB Active States Level

0: Logic low level (default)

1: Logic high level

Bit 1 (PWMABLV): PWMAB Active States Level

0: Logic low level (default)

1: Logic high level

Bit 0 (PWMALV): PWMA Active States Level

0: Logic low level (default)

1: Logic high level

6.1.131 Bank 3 R15 SLPWM (PWM Active States and Output Level Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PWMEAS	PWMELV
0	0	0	0	0	0	R/W	R/W

Bits 7~2: Not used. Set to 0 all the time

Bit 1 (PWMEAS): PWME Active States Select for Internal PWME Signal

0: The low state of PWMES is active (default)

1: The high state of PWMES is active

Bit 0 (PWMELV): PWME Active state Level

0: Logic low level (default)

1: Logic high level

6.1.132 Bank 3 R16 COPH (High Byte of Composite Mode Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	HACCHP	HABCHP	HAACHP	-	HACNHP	HABNHP	HAANHP
0	R	R	R	0	R	R	R

Bit 7: Not used. Set to 0 all the time

Bit 6 (HACCHP): Current Hall C Pattern

Bit 5 (HABCHP): Current Hall B Pattern

Bit 4 (HAACHP): Current Hall A Pattern

Bit 3: Not used. Set to 0 all the time

Bit 2 (HACNHP): Next Hall C Pattern

Bit 1 (HACNHP): Next Hall B Pattern

Bit 0 (HACNHP): Next Hall A Pattern

6.1.133 Bank 3 R17 COPL (Low Byte of Composite Mode Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CPWMCB	CPWMC	CPWMBB	CPWMB	CPWMAB	CPWMA
0	0	R	R	0	R	R	R

Bits 7~6: Not used. Set to 0 all the time

Bit 5 (CPWMCB): Composite PWM Mode for PWMCB

0: The PWMCB is at passive state

1: The generated waveform on PWMCB is dependent on T5EPWMCB and T6EPWMCB bit

Bit 4 (CPWMC): Composite PWM Mode for PWMC

0: The PWMC is at passive state

1: The generated waveform on PWMC is dependent on T5EPWMC and T6EPWMC bit

Bit 3 (CPWMBB): Composite PWM Mode for PWMBB

0: The PWMBB is at passive state

1: The generated waveform on PWMBB is dependent on T5EPWMBB and T6EPWMBB bit

Bit 2 (CPWMB): Composite PWM Mode for PWMB

0: The PWMB is at passive state

1: The generated waveform on PWMB is dependent on T5EPWMB and T6EPWMB bit

Bit 1 (CPWMAB): Composite PWM Mode for PWMAB

0: The PWMAB is at passive state

1: The generated waveform on PWMAB is dependent on T5EPWMAB and T6EPWMAB bit

Bit 0 (CPWMA): Composite PWM Mode for PWMA

0: The PWMA is at passive state

1: The generated waveform on PWMA is dependent on T5EPWMA and T6EPWMA bit

6.1.134 Bank 3 R18 MCOPH (High Byte of Mapping Composite Mode Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	MHACCHP	MHABCHP	MHAACHP	-	MHACNHP	MHABNHP	MHAANHP
0	R/W	R/W	R/W	0	R/W	R/W	R/W

Bit 7: Not used. Set to 0 all the time

Bit 6 (MHACCHP): Mapping Current Hall C Pattern

Bit 5 (MHABCHP): Mapping Current Hall B Pattern

Bit 4 (MHAACHP): Mapping Current Hall A Pattern

Bit 3: Not used. Set to 0 all the time

Bit 2 (MHACNHP): Mapping Next Hall C Pattern

Bit 1 (MHABNHP): Mapping Next Hall B Pattern

Bit 0 (MHAANHP): Mapping Next Hall A Pattern

6.1.135 Bank 3 R19 MCOPL (Low byte of Mapping Composite Mode Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	MCPWMCB	MCPWMC	MCPWMBB	MCPWMB	MCPWMAB	MCPWMA
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used. Set to 0 all the time

Bit 5 (MCPWMCB): Mapping PWMCB

Bit 4 (MCPWMC): Mapping PWMC

Bit 3 (MCPWMBB): Mapping PWMBB

Bit 2 (MCPWMB): Mapping PWMB

Bit 1 (MCPWMAB): Mapping PWMAB

Bit 0 (MCPWMA): Mapping PWMA

6.1.136 Bank 3 R1A T5DECR (Timer 5 Dead Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DEADTCF	DEADTBF	DEADTAF	-	DEADTCE	DEADTBE	DEADTAE
0	R/W	R/W	R/W	0	R/W	R/W	R/W

Bit 7: Not used. Set to 0 all the time

Bit 6 (DEADTCF): Run Flag of Dead-Time Function for PWMC and PWMCB

0: Dead-time is running

1: Dead-time is not running

Bit 5 (DEADTBF): Run Flag of Dead-Time Function for PWMB and PWMBB

0: Dead-time is running

1: Dead-time is not running

Bit 4 (DEADTAF): Run Flag of Dead-Time Function for PWMA and PWMAB

0: Dead-time is running

1: Dead-time is not running

Bit 3: Not used. Set to 0 all the time

Bit 2 (DEADTCE): Enable Dead-Time Function for PWMC and PWMCB

0: Disable (default)

1: Enable

Bit 1 (DEADTBE): Enable Dead-Time Function for PWMB and PWMBB

0: Disable (default)

1: Enable

Bit 0 (DEADTAE): Enable Dead-Time Function for PWMA and PWMAB

0: Disable (default)

1: Enable

6.1.137 Bank 3 R1B T5DEB (Timer 5 Dead Timer Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5DE7	T5DE6	T5DE5	T5DE4	T5DE3	T5DE2	T5DE1	T5DE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5DE7~T5DE0): The content of this register is a dead time value of Timer 5

6.1.138 Bank 3 R1C HACRH (High Byte of Hall Sensor Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HAMTE	HASAMP2	HASAMP1	HASAMP0	HANRE	HANRHL2	HANRHL1	HANRHL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (HAMTE): Mapping Transfer Enable for the Hall Pattern

0: If HANTE=0, HABNHP is not updated from MHABNHP.

1: If HANTE=1, HABNHP is updated from MHABNHP.

After finishing update, this bit is cleared to 0 automatically.

Bits 6~4 (HASAMP2~ HASAMP0): Hall Sampling

HASAMP2	HASAMP1	HASAMP0	Function Description
0	0	0	Only for IEHC bit.
0	0	1	A Timer 5 one match (while counting down) triggers the sampling
0	1	0	A Timer 5 period match (while counting up) triggers the sampling
0	1	1	A Timer5 compare(Duty) match of PWMA (while counting up) triggers the sampling
1	0	0	A Timer5 compare(Duty) match of PWMA (while counting down) triggers the sampling
1	0	1	Timer 6 compare(Duty) triggers the sampling
1	1	0	Timer 6 period match detected triggers the sampling
1	1	1	Both edge at one of the inputs HAx (x = A - C) triggers the sampling

Bit 3 (HANRE): Hall Sensor Noise Rejection Enable

0: Disable noise rejection

1: Enable noise rejection (Default).

Bits 2~0 (HANRHL2~ HANRHL0): Hall Sensor Input Noise Rejection High/Low Pulse Defined Bit.

HANRHL2	HANRHL1	HANRHL0	Function Description
0	0	0	8 x (1 / F_{HACK})
0	0	1	16 x (1 / F_{HACK})
0	1	0	32 x (1 / F_{HACK})
0	1	1	64 x (1 / F_{HACK})
1	0	0	128 x (1 / F_{HACK})
1	0	1	256 x (1 / F_{HACK})
1	1	0	512 x (1 / F_{HACK})
1	1	1	1024 x (1 / F_{HACK})

6.1.139 Bank 3 R1D HACRL (Low Byte of Hall Sensor Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HANRPRE1	HANRPRE0	HAER2COID	-	-	HACSF	HABSF	HAASF
R/W	R/W	R/W	0	0	R	R	R

Bits 7~6 (HANRPRE1~ HANRPRE0): Hall sensor noise rejection Pre-scaler options

HANRPRE1	HANRPRE0	Function Description
0	0	t5_tmr_clk / 1 = F_{HACK}
0	1	t5_tmr_clk / 2 = F_{HACK}
1	0	t5_tmr_clk / 4 = F_{HACK}
1	1	t5_tmr_clk / 8 = F_{HACK}

Bit 5 (HAER2COID): This bit defines if the CPWMxx is set to passive state as HAERRSF=1

0: The COIDF bit is not influenced by HAERRSF

1: The COIDF bit is set to one when HAERRSF=1

Bits 4~3: Not used. Set to 0 all the time

Bit 2 (HACSF): Sampled Hall C

Bit 1 (HABSF): Sampled Hall B

Bit 0 (HAASF): Sampled Hall A

6.1.140 Bank 3 R1E BRKCR1H (High Byte of Brake PWM Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CP1LVBRK	-	-	-	-	-	EIT1LVBRK	EIT0LVBRK
R/W	0	0	0	0	0	R/W	R/W

Bit 7 (CP1LVBRK): Select the CP1OUT level to trigger the brake PWM mode

0: Low level (default)

1: High level

Bits 6~2: Not used. Set to 0 all the time

Bit 1 (EIT1LVBRK): Select the EXINT1 pin level to trigger the brake PWM mode

0: Low level (default)

1: High level

Bit 0 (EIT0LVBRK): Select the EXINT0 pin level to trigger the brake PWM mode

0: Low level (default)

1: High level

6.1.141 Bank 3 R1F BRKCR1L (Low Byte of Brake PWM Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CP1BRKEN	-	-	-	-	-	EIT1BRKEN	EIT0BRKEN
R/W	0	0	0	0	0	R/W	R/W

Bit 7 (CP1BRKEN): Enable CP1OUT as a PWM brake signal

0: Disable (default)

1: Enable

Bits 6~2: Not used. Set to 0 all the time

Bit 1 (EIT1BRKEN): Enable EXINT1 as a PWM brake signal

0: Disable (default)

1: Enable

Bit 0 (EIT0BRKEN): Enable EXINT0 as a PWM brake signal

0: Disable (default)

1: Enable

6.1.142 Bank 3 R20 BRKCR2H (High Byte of Brake PWM Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	BRKFAC	-	BRKM1	BRKM0	BRKPWME
0	0	0	R/W	0	R/W	R/W	R/W

Bits 7~5: Not used. Set to 0 all the time

Bit 4 (BRKFAC): Brake Flag set-reset control

0: Disable (default)

1: Enable

Bit 3: Not used. Set to 0 all the time

Bits 2~1 (BRKM1~ BRKM0): Brake Mode Select

BRKM1	BRKM0	Function Description
0	0	Timer 6 period-matching triggers BRKS=0
0	1	Timer 5 period-matching (T5MS=0) or Timer 5 one-matching at down-counting(T5MS=1) triggers BRKS=0
1	X	BRKS is reset to 0 immediately once BRKF=0

Bit 0 (BRKPWME): Brake Signal Enable for PWME

0: Disable (default)

1: PWME can be switched to passive state by brake signal while BRKS signal is at a high level

6.1.143 Bank 3 R21 BRKCR2L (Low Byte of Brake PWM Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	BRKPWMCB	BRKPWMC	BRKPWMBB	BRKPWMB	BRKPWMAB	BRKPWMA
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used. Set to 0 all the time

Bit 5 (BRKPWMCB): Brake Signal Enable for PWMCB

0: Disable (default)

1: PWMCB can be switched to passive state by brake signal while BRKS signal is at a high level.

Bit 4 (BRKPWMC): Brake Signal Enable for PWMC

0: Disable (default)

1: PWMC can be switched to passive state by brake signal while BRKS signal is at a high level.

Bit 3 (BRKPWMBB): Brake Signal Enable for PWMBB

0: Disable (default)

1: PWMBB can be switched to passive state by brake signal while BRKS signal is at a high level.

Bit 2 (BRKPWMB): Brake Signal Enable for PWMB

0: Disable (default)

1: PWMB can be switched to passive state by brake signal while BRKS signal is at a high level.

Bit 1 (BRKPWMAB): Brake Signal Enable for PWMAB

0: Disable (default)

1: PWMAB can be switched to passive state by brake signal while BRKS signal is at a high level.

Bit 0 (BRKPWMA): Brake Signal Enable for PWMA

0: Disable (default)

1: PWMA can be switched to passive state by brake signal while BRKS signal is at a high level.

6.1.144 Bank 3 R22 TRADCR (PWM Trigger ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRADEN2	TRADTS2	TRAD2DIR1	TRAD1DIR0	TRADEN1	TRADTS1	TRAD1DIR1	TRAD1DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (TRADEN2): Trigger ADC Enable

0: Disable (default)

1: Enable, If the count value of Timer5 or Timer6 (Depend on TRADTS2) is equal to TRADV2 value, ADC is triggered to start (ADRUN is set by HW). However, the configuration of ADC must be set-up first.

Bit 6 (TRADTS2): Trigger ADC Source Select for TRADV2

0: Timer 5 (default)

1: Timer 6

Bits 5~4 (TRAD2DIR1~ TRAD2DIR0): If TRADTS2=0, the TRAD2DIR is valid, only for phase correct PWM mode

TRAD2DIR1	TRAD2DIR0	Function Description
0	0	Independent of the count direction of Timer5
0	1	Timer5 is counting down
1	0	Timer5 is counting up
1	1	Independent of the count direction of Timer5

Bit 3 (TRADEN1): Trigger ADC Enable

0: Disable (default)

1: Enable, If the count value of Timer5 or Timer6 (Depend on TRADTS1) is equal to TRADV1 value, ADC is triggered to start (ADRUN is set by HW). However, the configuration of ADC must be set-up first.

Bit 2 (TRADTS1): Trigger ADC Source Select for TRADV1

0: Timer 5 (default)

1: Timer 6

Bits 1~0 (TRAD1DIR1~ TRAD1DIR0): If TRADTS1=0, the TRAD1DIR is valid, only for phase correct PWM mode

TRAD1DIR1	TRAD1DIR0	Function Description
0	0	Independent of the count direction of Timer 5
0	1	Timer 5 is down-counting
1	0	Timer 5 is up-counting
1	1	Independent of the count direction of Timer 5

6.1.145 Bank 3 R23 TSF1H (High Byte of Timer Statue Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HAEDGEF	MTRF	TRAD2F	TRAD1F	COIDF	BRKF	BRKS	PWMES
R	R	R	R	R	R	R	R

Bit 7 (HAEDGEF): Composite PWM Mode Mapping Transfer Request Flag

0: No edge event on Hall pins which is processed by noise rejection (if HANRE=1)

1: There is an edge event on Hall pins which is processed by noise rejection (if HANRE=1)

H/W set and clear after read

Bit 6 (MTRF): Composite PWM Mode Mapping Transfer Request Flag

0: The mapping transfer doesn't happen

1: The mapping transfer happen

Bit 5 (TRAD2F): Trigger ADC source 2 Flag

0: If the count value of Timer5 or Timer6 (Depend on TRADTS2) is equal to TRADV2

1: Not action

Bit 4 (TRAD1F): Trigger ADC source 1 Flag

0: If the count value of Timer5 or Timer6 (Depend on TRADTS1) is equal to TRADV1

1: Not action

Bit 3 (COIDF): Composite PWM Mode Idle Flag

0: If this bit is equal to one, CPWMxx (xx = A, AB, B…CB) is cleared, the corresponding outputs are set to passive state

1: Not action

Bit 2 (BRKF): Brake Flag.

0: The brake condition has not been detected.

1: The brake condition has been detected.

Bit 1 (BRKS): Internal Brake signal

0: Active signal

1: Inactive signal

Bit 0 (PWMES): PWME State

0: The timer count is less than the compare value (T6CD)

1: The counter value is greater than or equal to the compare value (T6CD)

6.1.146 Bank 3 R24 TSF1L (Low Byte of Timer Statue Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PWMCS	PWMBS	PWMAS	T6MTF	T6RF	T5MTF	T5RF
0	R	R	R	R	R	R	R

Bit 7: Not used. Set to 0 all the time

Bit 6 (PWMCS): PWMC State

0: The timer count is less than the compare value (T5CCD)

1: The counter value is greater than or equal to the compare value (T5CCD)

Bit 5 (PWMBS): PWMB State

0: The timer count is less than the compare value (T5BCD)

1: The counter value is greater than or equal to the compare value (T5BCD)

Bit 4 (PWMAS): PWMA State

0: The timer count is less than the compare value (T5ACD)

1: The counter value is greater than or equal to the compare value (T5ACD)

Bit 3 (T6MTF): Timer 6 Mapping Transfer Flag

0: The mapping transfer is invalid

1: When T6MTS=1&T6MTR=0, the mapping transfer happens once

Bit 2 (T6RF): Timer 6 Run Flag

0: Stopped

1: Running

Bit 1 (T5MTF): Timer 5 Mapping Transfer Flag

0: The mapping transfer is invalid

1: When T5MTS=1 and T5MTR=0, the mapping transfer happens once

Bit 0 (T5RF): Timer 5 Run Flag

0: Stopped

1: Running

6.1.147 Bank 3 R25 SETM1H (High Byte of Timer Status Set Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IEHC	MTRS	-	-	COIDS	BRKFS	-	-
R/W	R/W	0	0	R/W	R/W	0	0

Bit 7 (IEHC): Immediate Execution the Hall Comparison

0: No action. It is reset after comparison.

1: Immediate execution of the Hall comparison

Bit 6 (MTRS): Set MTRF (Composite PWM Mode Mapping Transfer Request)

0: No action

1: Set MTRF to 1

Bits 5~4: Not used. Set to 0 all the time

Bit 3 (COIDS): Set COIDF (Composite PWM Mode Idle Flag)

0: No action

1: Set COIDF to 1

Bit 2 (BRKFS): Set BRKF

0: No action

1: Set BRKF to 1

Bits 1~0: Not used. Set to 0 all the time

6.1.148 Bank 3 R26 SETM1L (Low Byte of Timer Status Set Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	T6MTS	T6RS	T5MTS	T5RS
0	0	0	0	R/W	R/W	R/W	R/W

Bits 7~4: Not used. Set to 0 all the time

Bit 3 (T6MTS): Set Timer 6 Mapping Transfer

0: No action.

1: Set T6MTF to 1. This bit enables the mapping transfer.

Bit 2 (T6RS): Set Timer 6 Run

0: No action.

1: Set T6RF to 1. This bit enables the Timer 6

Bit 1 (T5MTS): Set Timer 5 Mapping Transfer

0: No action.

1: Set T5MTF to 1. This bit enables the mapping transfer.

Bit 0 (T5RS): Set Timer 5 Run

0: No action.

1: Set T5RF to 1. This bit enables the Timer 5

6.1.149 Bank 3 R27 RSTM1H (High Byte of Timer Status Reset Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	MTRR	-	-	COIDR	BRKFR	-	-
R	R/W	R	R	R/W	R/W	R	R

Bit 7: Not used. Set to 0 all the time

Bit 6 (MTRR): Reset MTRF (Composite PWM Mode Mapping Transfer Request)

0: No action.

1: Reset MTRF to 0

Bits 5~4: Not used. Set to 0 all the time

Bit 3 (COIDR): Reset COIDF (Composite PWM Mode Idle Flag)

0: No action.

1: Reset COPDF to 0

Bit 2 (BRKFR): Reset BRKF

0: No action.

1: Reset BRKF to 0.

Bits 1~0: Not used. Set to 0 all the time

6.1.150 Bank 3 R28 RSTM1L (High Byte of Timer Status Reset Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	T6MTR	T6RR	T5MTR	T5RR
0	0	0	0	R/W	R/W	R/W	R/W

Bits 7~4: Not used. Set to 0 all the time

Bit 3 (T6MTR): Reset Timer 6 Mapping Transfer

0: No action.

1: Reset T6MTF to 0.

Bit 2 (T6RR): Reset Timer 6 Run

0: No action.

1: T6RF is logic 0. Timer 6 stops counting

Bit 1 (T5MTR): Reset Timer 5 Mapping Transfer

0: No action.

1: Reset T5MTF to 0.

Bit 0 (T5RR): Reset Timer 5 Run

0: No action.

1: T5RF is logic 0. Timer 5 stops counting

6.1.151 Bank 3 R29~R2A: (Reserved)

6.1.152 Bank 3 R2B T5VALH (High Byte of Timer 5 Current Counter Value Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5VAL15	T5VAL14	T5VAL13	T5VAL12	T5VAL11	T5VAL10	T5VAL9	T5VAL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5VAL15~T5VAL8): Current counter value of Timer 5

6.1.153 Bank 3 R2C T5VALL (Low Byte of Timer 5 Current Counter Value Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5VAL7	T5VAL6	T5VAL5	T5VAL4	T5VAL3	T5VAL2	T5VAL1	T5VAL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5VAL7~T5VAL0): Current counter value of timer 5

6.1.154 Bank 3 R2D T5PDH (High Byte of Timer 5 Period Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5PD15	T5PD14	T5PD13	T5PD12	T5PD11	T5PD10	T5PD9	T5PD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5PD15~T5PD8): Period value of timer 5

6.1.155 Bank 3 R2E T5PDL (Low Byte of Timer 5 Period Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5PD7	T5PD6	T5PD5	T5PD4	T5PD3	T5PD2	T5PD1	T5PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5PD7~T5PD0): Period value of timer 5

6.1.156 Bank 3 R2F T5ACDH (High Byte of Timer 5 PWMA Duty Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5ACD15	T5ACD14	T5ACD13	T5ACD12	T5ACD11	T5ACD10	T5ACD9	T5ACD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5ACD15~T5ACD8): Duty value of timer 5 PWMA

6.1.157 Bank 3 R30 T5ACDL (Low Byte of Timer 5 PWMA Duty Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5ACD7	T5ACD6	T5ACD5	T5ACD4	T5ACD3	T5ACD2	T5ACD1	T5ACD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5ACD7~T5ACD0): Duty value of timer 5 PWMA

6.1.158 Bank 3 R31 T5BCDH (High Byte of Timer 5 PWMB Duty Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5BCD15	T5BCD14	T5BCD13	T5BCD12	T5BCD11	T5BCD10	T5BCD9	T5BCD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5BCD15~T5BCD8): Duty value of timer 5 PWMB

6.1.159 Bank 3 R32 T5BCDL (Low Byte of Timer 5 PWMB Duty Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5BCD7	T5BCD6	T5BCD5	T5BCD4	T5BCD3	T5BCD2	T5BCD1	T5BCD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5BCD7~T5BCD0): Duty value of timer 5 PWMB

6.1.160 Bank 3 R33 T5CCDH (High Byte of Timer 5 PWMC Capture / Duty Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5CCD15	T5CCD14	T5CCD13	T5CCD12	T5CCD11	T5CCD10	T5CCD9	T5CCD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5CCD15~T5CCD8): Duty value of timer 5 PWMC

6.1.161 Bank 3 R34 T5CCDL (Low Byte of Timer 5 PWMC Duty Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5CCD7	T5CCD6	T5CCD5	T5CCD4	T5CCD3	T5CCD2	T5CCD1	T5CCD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5CCD7~T5CCD0): Duty value of timer 5 PWMC

6.1.162 Bank 3 R35 T5ACDMH (High Byte of Timer 5 PWMA Duty Mapping Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5ACDM 15	T5ACDM 14	T5ACDM 13	T5ACDM 12	T5ACDM 11	T5ACDM 10	T5ACDM 9	T5ACDM 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5ACDM15~T5ACDM8): Duty mapping the value of Timer 5 PWMA

6.1.163 Bank 3 R36 T5ACDML (Low Byte of Timer 5 PWMA Duty Mapping Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5ACDM7	T5ACDM6	T5ACDM5	T5ACDM4	T5ACDM3	T5ACDM2	T5ACDM1	T5ACDM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5ACDM7~T5ACDM0): Duty mapping the value of timer 5 PWMA

6.1.164 Bank 3 R37 T5BCDMH (High Byte of Timer 5 PWMB Duty Mapping Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5BCDM 15	T5BCDM 14	T5BCDM 13	T5BCDM 12	T5BCDM 11	T5BCDM 10	T5BCDM 9	T5BCDM 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5BCDM15~T5BCDM8): Duty mapping the value of timer 5 PWMB

6.1.165 Bank 3 R38 T5BCDML (Low Byte of Timer 5 PWMB Capture / Duty Mapping Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5BCDM7	T5BCDM6	T5BCDM5	T5BCDM4	T5BCDM3	T5BCDM2	T5BCDM1	T5BCDM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5BCDM7~T5BCDM0): Duty mapping the value of timer 5 PWMB

6.1.166 Bank 3 R39 T5CCDMH (High Byte of Timer 5 PWMC Capture / Duty Mapping Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5CCDM 15	T5CCDM 14	T5CCDM 13	T5CCDM 12	T5CCDM 11	T5CCDM 10	T5CCDM 9	T5CCDM 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5CCDM15~T5CCDM8): Duty mapping the value of timer 5 PWMC

6.1.167 Bank 3 R3A T5CCDML (Low Byte of Timer 5 PWMC Duty Mapping Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5CCDM7	T5CCDM6	T5CCDM5	T5CCDM4	T5CCDM3	T5CCDM2	T5CCDM1	T5CCDM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T5CCDM7~T5CCDM0): Duty mapping the value of Timer 5 PWMC

6.1.168 Bank 3 R3B TRAD1VH (High Byte of Trigger ADC of Timer Value Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRAD1V 15	TRAD1V 14	TRAD1V 13	TRAD1V 12	TRAD1V 11	TRAD1V 10	TRAD1V 9	TRAD1V 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TRAD1V15~TRAD1V8): Trigger ADC of Timer Value

6.1.169 Bank 3 R3C TRAD1VL (Low Byte of Trigger ADC of Timer Value Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRAD1V 7	TRAD1V 6	TRAD1V 5	TRAD1V 4	TRAD1V 3	TRAD1V 2	TRAD1V 1	TRAD1V 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TRAD1V7~TRAD1V0): Trigger ADC of Timer Value

6.1.170 Bank 3 R3D TRAD2VH (High Byte of Trigger ADC of Timer Value Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRAD2V 15	TRAD2V 14	TRAD2V 13	TRAD2V 12	TRAD2V 11	TRAD2V 10	TRAD2V 9	TRAD2V 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TRAD2V15~TRAD2V8): Trigger ADC of Timer Value

6.1.171 Bank 3 R3E TRAD2VL (Low Byte of Trigger ADC of Timer Value Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRAD2V7	TRAD2V6	TRAD2V5	TRAD2V4	TRAD2V3	TRAD2V2	TRAD2V1	TRAD2V0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits

7~0 (TRAD2V7~TRAD2V0): Trigger ADC of Timer Value

6.1.172 Bank 3 R3F T6VALH (High Byte of Timer 6 Current Counter Value Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6VAL15	T6VAL14	T6VAL13	T6VAL12	T6VAL11	T6VAL10	T6VAL9	T6VAL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits

s 7~0 (T6VAL15~ T6VAL8): Current counter value of Timer 6

6.1.173 Bank 3 R40 T6VALL (Low Byte of Timer 6 Current Counter Value Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6VAL7	T6VAL6	T6VAL5	T6VAL4	T6VAL3	T6VAL2	T6VAL1	T6VAL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits

s 7~0 (T6VAL7~ T6VAL0): Current counter value of timer 6

6.1.174 Bank 3 R41 T6PDH (High Byte of Timer 6 Period Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6PD15	T6PD14	T6PD13	T6PD12	T6PD11	T6PD10	T6PD9	T6PD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits

s 7~0 (T6PD15~ T6PD8): Period value of timer 6

6.1.175 Bank 3 R42 T6PDL (Low Byte of Timer 6 Period Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6PD7	T6PD6	T6PD5	T6PD4	T6PD3	T6PD2	T6PD1	T6PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits

Bits 7~0 (T6PD7~ T6PD0): Period value of Timer 6

6.1.176 Bank 3 R43 T6CDH (High Byte of Timer 6 Capture / Duty Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6CD15	T6CD14	T6CD13	T6CD12	T6CD11	T6CD10	T6CD9	T6CD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T6CD15~ T6CD8): Capture / Duty value of timer 6

6.1.177 Bank 3 R44 T6CDL (Low Byte of Timer 6 Capture / Duty Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6CD7	T6CD6	T6CD5	T6CD4	T6CD3	T6CD2	T6CD1	T6CD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T6CD7~ T6CD0): Capture / Duty value of Timer 6

6.1.178 Bank 3 R45 T6CDMH (High Byte of Timer 6 Capture / Duty Mapping Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6CDM 15	T6CDM 14	T6CDM 13	T6CDM 12	T6CDM 11	T6CDM 10	T6CDM 9	T6CDM 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T6CDM15~ T6CDM8): Capture / Duty mapping the value of Timer 6

6.1.179 Bank 3 R46 T6CDML (Low Byte of Timer 6 Capture / Duty Mapping Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T6CDM7	T6CDM6	T6CDM5	T6CDM4	T6CDM3	T6CDM2	T6CDM1	T6CDM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (T6CDM7~ T6CDM0): Capture / Duty mapping the value of Timer 6

6.1.180 Bank 3 R47~R4B: (Reserved)

6.1.181 Bank 3 R4C: SFR9 (Status Flag Register 9)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5PDMSF	T5ONEMSF	IRT5CSF	IRT5BSF	IRT5ASF	IFT5CSF	IFT5BSF	IFT5ASF
F	F	F	F	F	F	F	F

Bit 7 (T5PDMSF): Timer 5 Period Match Status Flag

0: No Timer 5 period-matching.

1: Timer 5 period-matching.

Bit 6 (T5ONEMSF): Timer 5 One Match Status Flag

0: No Timer 5 one-matching.

1: Timer 5 one-matching (While counting down).

Bit 5 (IRT5CSF): Status Flag for Duty Match

0: No event happens.

1: T5CCD-Matching (up-counting) happens in PWM mode.

Bit 4 (IRT5BSF): Status Flag for Duty (Compare) Match

0: No event happens.

1: T5BCD-Matching (up-counting) happens in PWM mode.

Bit 3 (IRT5ASF): Status Flag for Duty (Compare) Match

0: No event happens.

1: T5ACD-Matching (up-counting) happens in PWM mode.

Bit 2 (IFT5CSF): Status Flag for Duty (Compare) Match

0: No event happens.

1: T5CCD-Matching (down-counting) happens in PWM mode.

Bit 1 (IFT5BSF): Status Flag for Duty (Compare) Match

0: No event happens.

1: T5BCD-Matching (down-counting) happens in PWM mode.

Bit 0 (IFT5ASF): Status Flag for Duty (Compare) Match

0: No event happens.

1: T5ACD-Matching (down-counting) happens in PWM mode

NOTE

If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.

6.1.182 Bank 3 R4D: SFR10 (Status Flag Register 10)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MTRSF	BRKSF	HAEGSF	HACOSF	HAERRSF	T6PDMSF	IRT6SF	IFT6SF
F	F	F	F	F	F	F	F

Bit 7 (MTRSF): Composite PWM Mode Mapping Transfer Request Status Flag

0: Invalid.

1: When MTRF =1

Bit 6 (BRKSF): Brake Status flag

0: Invalid.

1: When BRKF =1

Bit 5 (HAEGSF): Hall edge Status flag

0: Invalid.

1: When HAEDGSF =1

Bit 4 (HACOSF): Correct Hall Event Status flag

0: Invalid.

1: Means HAxSF=HAxNHP.

Bit 3 (HAERRSF): Error Hall Event Status Flag

0: Invalid.

1: The state of Hall event is error.

Bit 2 (T6PDMSF): Timer 6 Period Match Status Flag

0: No Timer 6 period-matching.

1: Timer 6 period-matching.

Bit 1 (IRT6SF): Status Flag for Duty (Compare) Match or rising captured PWME pin

0: No event happens.

1: T6CD-Matching (up-counting) happens in PWM mode or rising edge happens at PWME pin in captured mode.

Bit 0 (IFT6SF): Status Flag for falling captured PWME pin

0: No event happens.

1: Falling edge happens at PWME pin in captured mode.

6.1.183 Bank 3 R4E IMR9 (Interrupt Mask Register 9)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T5PDMIE	T5ONEMIE	IRT5CIE	IRT5BIE	IRT5AIE	IFT5CIE	IFT5BIE	IFT5AIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (T5PDMIE): Timer 5 Period Match Interrupt Enable Select bit

0: Not action.

1: If T5PDMSF = 1, T5PDM interrupt happens.

Bit 6 (T5ONEMIE): Timer 5 One Match Interrupt Enable Select bit.

0: Not action.

1: If T5ONEMSF = 1, T5ONEM interrupt happens.

Bit 5 (IRT5CIE): Timer 5 PWMC Rising Edge Interrupt Enable Select bit.

0: Not action.

1: If IRT5CSF = 1, IRT5C interrupt happens.

Bit 4 (IRT5BIE): Timer 5 PWMB Rising Edge Interrupt Enable Select bit.

0: Not action.

1: If IRT5BSF = 1, IRT5B interrupt happens.

Bit 3 (IRT5AIE): Timer 5 PWMA Rising Edge Interrupt Enable Select bit.

0: Not action.

1: If IRT5ASF = 1, IRT5A interrupt happens.

Bit 2 (IFT5CIE): Timer 5 PWMC Falling Edge Interrupt Enable Select bit.

0: Not action.

1: If IFT5CSF = 1, IFT5C interrupt happens.

Bit 1 (IFT5BIE): Timer 5 PWMB Falling Edge interrupt Enable Select bit.

0: Not action.

1: If IFT5BSF = 1, IFT5B interrupt happens.

Bit 0 (IFT5AIE): Timer 5 PWMA Falling Edge interrupt Enable Select bit.

0: Not action.

1: If IFT5ASF = 1, IFT5A interrupt happens.

NOTE

If the interrupt mask and instruction "ENI" is enabled, the program counter would jump into corresponding interrupt vector when the corresponding status flag is set.

6.1.184 Bank 3 R4F IMR10 (Interrupt Mask Register 10)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MTRIE	BRKIE	HAEGIE	HACOIE	HAERRIE	T6PDMIE	IRT6IE	IFT6IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (MTRIE): Interrupt Enable select bit

0: Not action.

1: If MTRSF=1, the interrupt will be triggered.

Bit 6 (BRKIE): Brake Status flag

0: Not action.

1: If BRKSF=1, the interrupt will be triggered.

Bit 5 (HAEGIE): Hall edge Status flag

0: Not action.

1: If HAEGSF=1, the interrupt will be triggered.

Bit 4 (HACOIE): Correct Hall Event Status flag

0: Not action.

1: If HACOSF = 1, HACO interrupt happens.

Bit 3 (HAERRIE): Error Hall Event Status Flag

0: Not action.

1: If HAERRSF = 1, HAERR interrupt happens.

Bit 2 (T6PDMIE): Timer 6 Period Match Interrupt Enable select bit.

0: Not action.

1: If the T6PDMIE = 1, T6PDMSF = 1, TMR6 interrupt happens.

Bit 1 (IRT6IE): Timer 6 Input Rising Edge Interrupt Enable select bit.

0: Not action.

1: If the IRT6IE = 1, and IRT6SF = 1, TMR6 interrupt happens.

Bit 0 (IFT6IE): Timer 6 Input Falling Edge Interrupt Enable select bit

0: Not action.

1: If the IFT6IE = 1, and IFT6SF = 1, TMR6 interrupt happens.

6.1.185 R50~R7F, Banks 0~3 R80~RFF

All of these are 8-bit general-purpose registers.

6.2 WDT and Prescaler

There is one 8-bit counter available as prescalers for the WDT respectively. The WPSR0~WPSR2 bits of the WDTCR register (Bank0 R21) are used to determine the prescaler of WDT. The WDT and prescaler will be cleared by the “WDTC” and “SLEP” instructions. Figure 6-4 depicts the circuit diagram of WDT.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit of WDTCR (Bank0 R21) register. With no prescaler, the WDT time-out period is approximately 16.5 ms[1] (one oscillator start-up timer period).

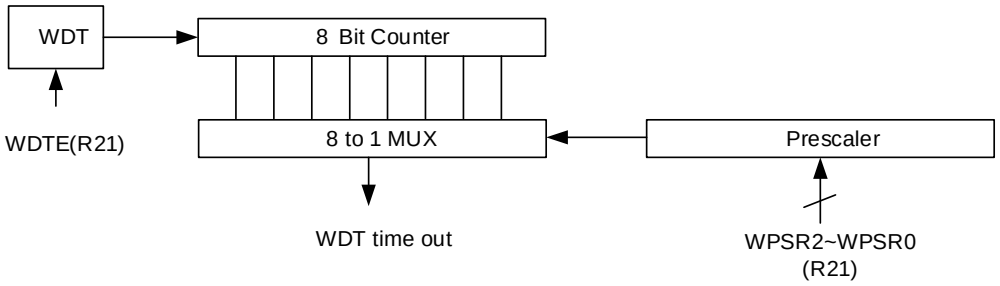


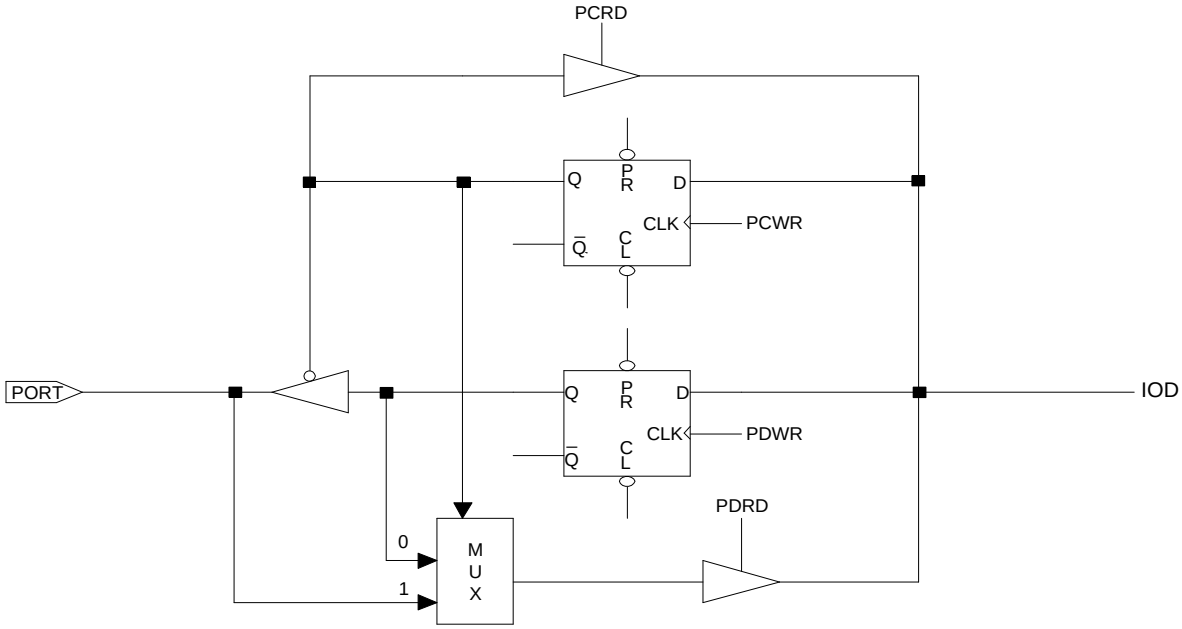
Figure 6-4 Block Diagram of WDT

[1] NOTE: VDD=5V, WDT time-out period = 16.5ms ± 10%

6.3 I/O Ports

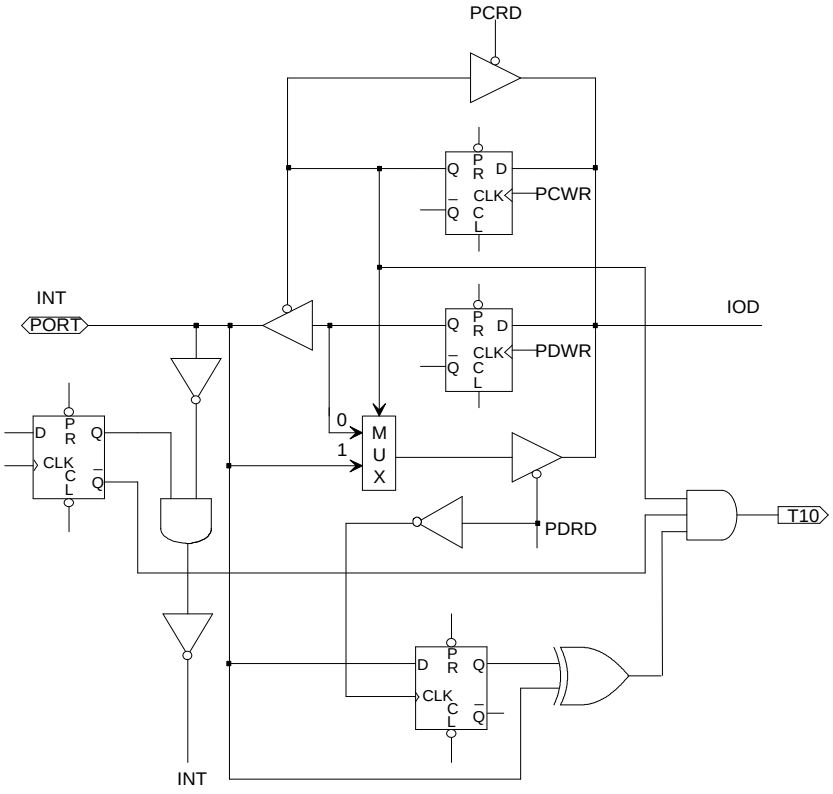
The I/O registers, Port 5~Port 7 are bi-directional tristate I/O ports. All can be pulled high or low internally by software. In addition, they can also have open-drain output and high sink/drive set by software. Besides wake-up and interrupt functions, the ports also have input status change interrupt function. Each I/O pin can be defined as an "input" or "output" pin by the I/O control register (IOCR5 ~ IOC7).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 7 are shown in the following Figure 6-5, Figure 6-6, Figure 6-7, and Figure 6-8.



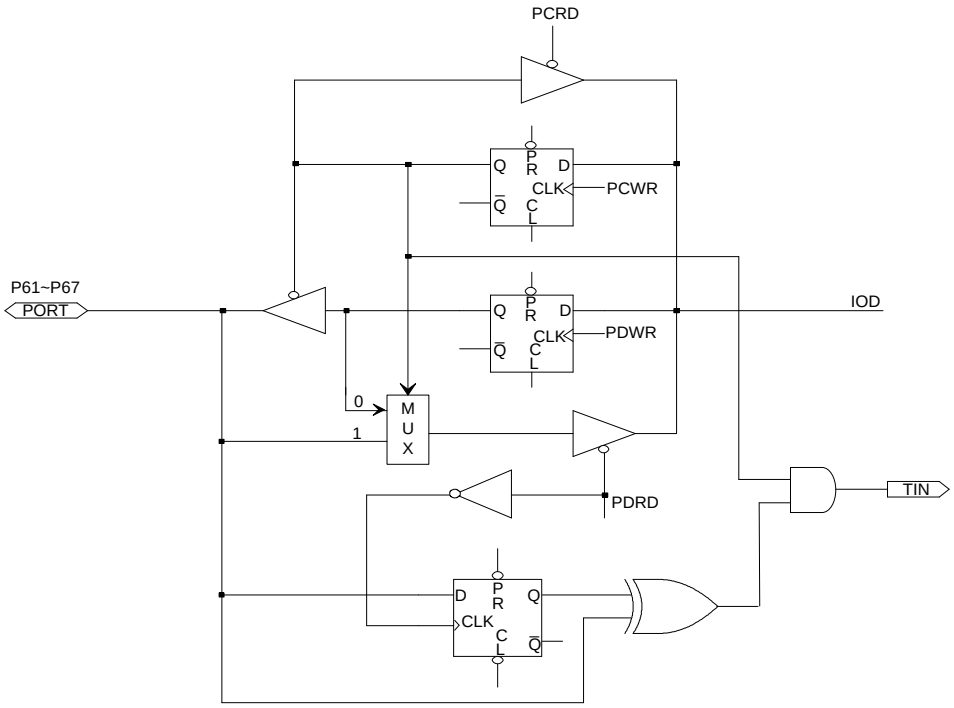
Note: Pull-down is not shown in the figure.

Figure 6-5 Circuit of I/O Port and I/O Control Register for Ports 5~7



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-6 Circuit of I/O Port and I/O Control Register for INT



***Note**: Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-7 Circuit of I/O Port and I/O Control Register for Port 5~7

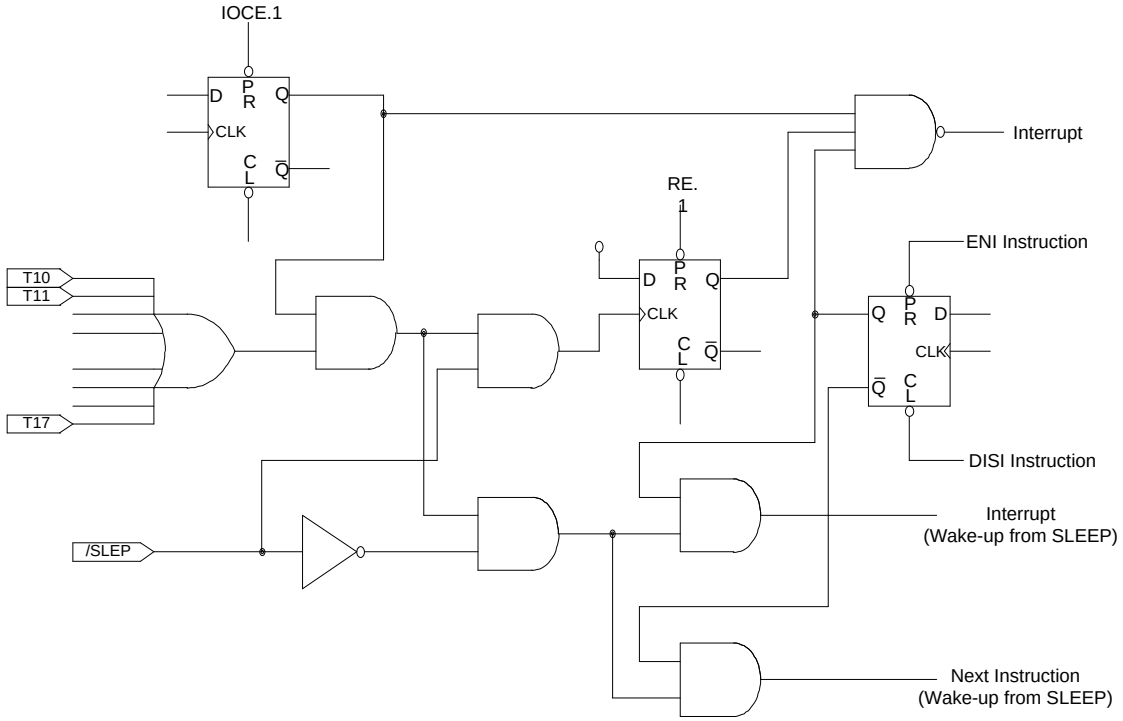


Figure 6-8 Block Diagram of I/O Ports 5~7 with Input Change Interrupt/Wake-up

Table 2 Usage of Ports 5~7 Input Changed Wake-up/Interrupt Function

Usage of Ports 5~7 Input Status Changed Wake-up/Interrupt	
(I) Wake-up	(II) Wake-up and interrupt
(a) Before SLEEP	(a) Before SLEEP
1. Disable WDT	1. Disable WDT
2. Read I/O Port (MOV R6,R6)	2. Read I/O Port (MOV R6,R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set ICWKPx*=1)	4. Enable wake-up bit (Set ICWKPx*=1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set PxICIE* =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (0004H)
	2. IF "DISI" → Next instruction

*x = 5~7

6.4 Reset and Wake-up

6.4.1 Reset

A Reset is initiated by one of the following events:

(1) Power-on reset.

(2) /RESET pin input "low"

(3) WDT time-out (if enabled).

(4) BOR (if enabled).

(5) Software Reset (instruction “RESET”)

The device is kept in a RESET condition for a period of approx. 16ms[2] (one oscillator start-up timer period) after the reset is detected. If the /Reset pin goes “low” or WDT time-out is active, a reset is generated, in IRC mode the reset time is WSTO and 8/16 clocks. Once a RESET occurs, the following functions are performed.

Refer to Figure 6-9.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The bits of the control register are set in Table 3.

The sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After wake-up is generated, in IRC mode the wake-up time is WSTO and 8/16 clocks. The controller can be awakened by:

(1) External reset input on /RESET pin,

(2) WDT time-out (if enabled).

(3) External (INT) pin changes (if INTWK is enabled).

(4) Port input status changes (if ICWKPx is enabled).

(5) Low Voltage Detector (if LVDWK enable).

(6) Completion of A/D conversion (if ADWK is enabled).

(7) Comparator 1 ~ 2 output statuses change (if CMP1WK/CMP2WK is enabled).

[2] NOTE: Vdd = 5V, set up time = 16.5ms ± 10%

The first two cases will cause the EM88F794N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3~7 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 0x02~0x62 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. Only one of the Cases 3 to 7 can be enabled before entering into sleep mode. That is,

[a] If WDT is enabled before SLEP, the EM88F794N can be woken-up only by Case 1 or Case 2. Refer to the section on Interrupt for further details.

[b] If External (INT0, INT1) pin change is used to wake up EM88F794N and INTWK bit is enabled before SLEP, WDT must be disabled. Hence, the EM88F794N can be woken up only by Case 3.

[c] If Port Input Status Change is used to wake up EM88F794N and corresponding wake-up setting is enabled before SLEP, WDT must be disabled. Hence, the EM88F794N can be woken up only by Case 4.

[d] If Low voltage detector is used to wake up EM88F794N and LVDWK bit is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F794N can be woken up only by Case 5

[e] If AD conversion completed is used to wake up EM88F794N and ADWK is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F794N can be woken up only by Case 6.

[g] If Comparator 1/2 output status change is used to wake up EM88F794N and CMP1/2WK bit is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F794N can be woken up only by Case 7.

Table 3 All kinds of wake-up and interrupt modes are shown below:

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	INTWK = 0, EXIE = 0	INT Pin Disable							
	INTWK = 0, EXIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	INTWK = 1, EXIE = 0	INT Pin Disable							
	INTWK = 1, EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Pin Change Interrupt	WKPxH/L = 0, PxICIE = 0	Wake-up is invalid				Interrupt is invalid			
	WKPxH/L = 0, PxICIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	WKPxH/L = 1, PxICIE = 0	Wake up + Next Instruction				Interrupt is invalid			
	WKPxH/L = 1, PxICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Detector Interrupt	LVDWK = 0 LVDIE = 0	Wake-up is invalid				Interrupt is invalid			
	LVDWK = 0 LVDIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVDWK = 1 LVDIE = 0	Wake up + Next Instruction				Interrupt is invalid			
	LVDWK = 1 LVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
AD Interrupt	ADWK = 0, ADIE = 0	Wake-up is invalid				Interrupt is invalid			
	ADWK = 0, ADIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ADWK = 1, ADIE = 0	Wake up + Next Instruction **Fs and Fh don't stop**				Interrupt is invalid			
	ADWK = 1, ADIE = 1	Wake up + Next	Wake up + Interrupt	Wake up + Next	Wake up + Interrupt	Next Instruction	Interrupt + Interrupt	Next Instruction	Interrupt + Interrupt

		Instruction **Fs and Fh don't stop**	Vector **Fs and Fh don't stop**	Instruction **Fs and Fh don't stop**	Vector **Fs and Fh don't stop**		Vector		Vector
Comparator 1/2 (Comparator output status change)	CMPxWK=0 CMPxIE=0	Wake-up is invalid.		Wake-up is invalid.		Wake-up is invalid.		Wake-up is invalid.	
	CMPxWK=0 CMPxIE=1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	CMPxWK=1 CMPxIE=0	Wake up + Next Instruction		Wake up + Next Instruction		Wake-up is invalid.		Wake-up is invalid.	
	CMPxWK=1 CMPxIE=1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TM1/2/3/4 Interrupt (Used as timer)	TM1/2/3/4 IE = 0	Wake-up is invalid		Wake-up is invalid.		Interrupt is invalid		Interrupt is invalid	
	TM1/2/3/4 IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TM1/2/3/4 Interrupt (Used as counter)	TM1/2/3/4 IE = 0	Wake-up is invalid		Wake-up is invalid.		Interrupt is invalid		Interrupt is invalid	
	TC1/2/3/4 IE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TM5 Period Match Interrupt	T5PDMIE = 0	Wake-up is invalid		Wake-up is invalid.		Interrupt is invalid		Interrupt is invalid	
	T5PDMIE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TM5 One Match Interrupt	T5ONEM IE = 0	Wake-up is invalid		Wake-up is invalid.		Interrupt is invalid		Interrupt is invalid	
	T5ONEM IE = 0			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TM6 Period Match Interrupt	T6PDMIE = 0	Wake-up is invalid		Wake-up is invalid.		Interrupt is invalid		Interrupt is invalid	
	T6PDMIE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
WDT time out		RESET	RESET	RESET	RESET	RESET	RESET	RESET	RESET

After wake-up:

1. If interrupt enable → interrupt + next instruction
2. If interrupt disable → next instruction

6.5 Status of RST, T, and P of Status Register

A RESET condition is initiated by the following events:

1. A power-on condition,

2. A high-low-high pulse on /RESET pin

3. Watchdog timer time-out.

4. BOR occurs

The values of T and P, listed in Table 5 are used to check how the processor wakes up. Table 6 shows the events that may affect the status of T and P.

Table 5 Values of RST, T and P after RESET

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during SLEEP mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during SLEEP mode	0	0
Wake-up on pin change during SLEEP mode	1	0

*P: Previous status before reset

Table 6 The Status of T and P Being Affected by Events.

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during SLEEP mode	1	0

*P: Previous value before reset

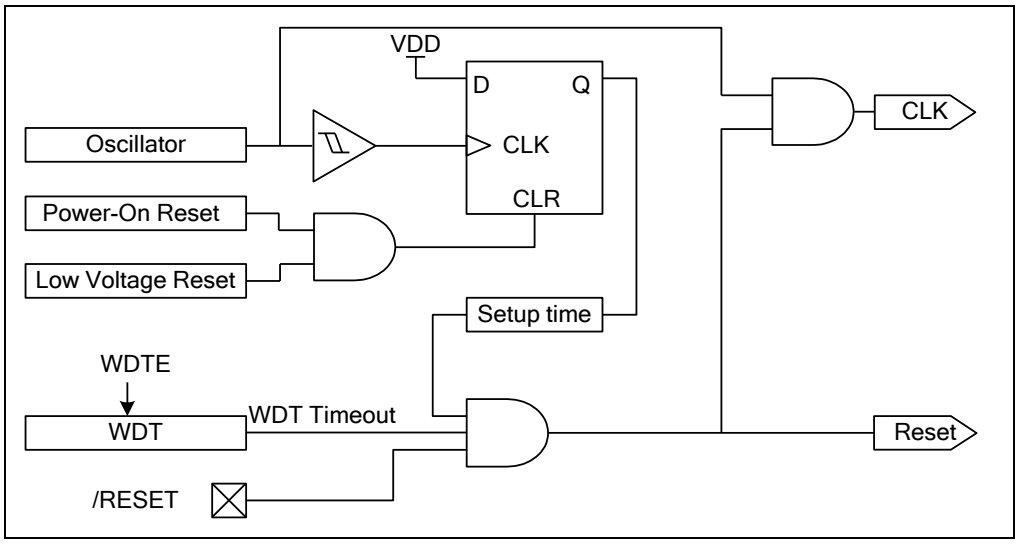


Figure 6-9 Block Diagram of Controller Reset

Table 4 Summary of the Initialized Values for Registers

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	IAR7	IAR6	IAR5	IAR4	IAR3	IAR2	IAR1	IAR0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x01	R1 (BSR)	Bit Name	-	-	SBS1	SBS0	-	-	-	GBS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	0	0	P	P
0x02	R2 (PCL)	Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	INT	N	OV	T	P	Z	DC	C
		Power-On	0	U	U	1	1	U	U	U
		/RESET and WDT	0	P	P	t	t	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 0, R5 (Port 5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x06	Bank 0, R6 (Port 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	Bank 0, R7 (Port 7)	Bit Name	-	-	-	-	-	-	P71	P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0X0B	Bank 0, RB (IOCR5)	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0C	Bank 0, RC (IOCR6)	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 0, RD (IOCR7)	Bit Name	-	-	-	-	-	-	IOC71	IOC70
		Power-On	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0x0E	Bank 0, RE (OMCR)	Bit Name	CPUS	IDLE	CLK2	CLK1	CLK0	-	RCM1	RCM0
		Power-On	Code option (HLFS)	1	Code option (CLK2)	Code option (CLK1)	Code option (CLK0)	0	Code option (RCM1)	Code option (RCM0)
		/RESET and WDT	Code option (HLFS)	1	P	P	P	0	Code option (RCM1)	Code option (RCM0)
		Wake-Up from Sleep/Idle	P	P	P	P	P	0	P	P
0x0F	Bank 0, RF EIESCR	Bit Name	-	-	-	-	EIES1	EIES0	-	-
		Power-On	0	0	0	0	1	1	0	0
		/RESET and WDT	0	0	0	0	1	1	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	0	0
0x10	Bank 0, R10 (WUCR1)	Bit Name	CMP2 WK	CMP1 WK	LVDWK	ADWK	INT1 WK	INT0 WK	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	0	0

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x12	Bank 0, R12 WUCR3	Bit Name	-	ICWKP7	ICWKP6	ICWKP5	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	0	0	0	0
0X14	Bank 0, R14 SFR1	Bit Name	CMP2SF	CMP1SF	LVDSF	ADSF	EXSF1	EXSF0	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	0	0
0X17	BANK 0, R17 SFR4	Bit Name	-	P7ICSF	P6ICSF	P5ICSF	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	0	0	0	0
0X19	BANK 0, R19 SFR6	Bit Name	SHSF	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	0	0	0	0
0X1B	BANK 0, R1B IMR1	Bit Name	CMP2IE	CMP1IE	LVDIE	ADIE	EXIE1	EXIE0	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	0	0
0X1E	BANK 0, R1E IMR4	Bit Name	-	P7ICIE	P6ICIE	P5ICIE	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	0	0	0	0
0X20	BANK 0, R20 IMR6	Bit Name	SHIE	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	0	0	0	0
0X21	BANK 0, R21 WDTCR	Bit Name	WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X3E	BANK 0, R3E ADCR1	Bit Name	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3F	BANK 0, R3F ADCR2	Bit Name	-	VPIS2	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	P	P	P	0
0X40	BANK 0, R40 ADISR	Bit Name	STPMK	-	-	-	ADIS3	ADIS2	ADIS1	ADIS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	P	P	P	P
0X41	BANK 0, R41 ADER1	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X43	BANK 0, R43 ADDL	Bit Name	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X44	BANK 0, R44 ADDH	Bit Name	ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X45	BANK 0, R45 ADCVL	Bit Name	ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X46	BANK 0, R46 ADCVH	Bit Name	ADCD 15	ADCD 14	ADCD 13	ADCD 12	ADCD 11	ADCD 10	ADCD 9	ADCD 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X47	BANK 0, R47 ADCONBUF	Bit Name	ADBFEN	ADBFOVR	ADBFINT	-	-	ADBFPTR2	ADBFPTR1	ADBFPTR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	0	P	P	P
0X08	BANK 1, R8 P5PHCR	Bit Name	PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X09	BANK 1, R9 P6PHCR	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0A	BANK 1, RA P7PHCR	Bit Name	-	-	-	-	-	-	-	P7LPH
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	0	P
0X0B	BANK 1, RB P5PLCR	Bit Name	PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0C	BANK 1, RC P6PLCR	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0D	BANK 1, RD P7PLCR	Bit Name	-	-	-	-	-	-	-	P7LPL
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	0	P
0X0E	BANK 1, RE P5HDSCR	Bit Name	H57	H56	H55	H54	H53	H52	H51	H50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	BANK 1, RF P6HDSCR	Bit Name	H67	H66	H65	H64	H63	H62	H61	H60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X10	BANK 1, R10 P7HDSCR	Bit Name	-	-	-	-	-	-	-	P7LHDS
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	0	P
0X11	BANK 1, R11 P5ODCR	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X12	BANK 1, R12 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X13	BANK 1, R13 P7ODCR	Bit Name	-	-	-	-	-	-	-	P7LOD
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	0	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X44	BANK 1, R44 FLKR	Bit Name	FLK7	FLK6	FLK5	FLK4	FLK3	FLK2	FLK1	FLK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X45	BANK 1, R45 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	BANK 1, R46 TBPTH	Bit Name	HLB	RDS	-	-	TB11	TB10	TB9	TB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	0	0	P	P	P	P
0X47	BANK 1, R47 STKMON	Bit Name	STOV	-	-	-	-	STL2	STL1	STL0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	0	P	P	P
0X48	BANK 1, R48 PCH	Bit Name	-	-	-	-	PC11	PC10	PC9	PC8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	P	P
0X49	BANK 1, R49 LVDCR	Bit Name	LVDEN	-	-	-	LVDB	-	-	-
		Power-On	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	P	0	0	0
0X4D	BANK 1, R4D TBWCR	Bit Name	-	-	-	-	-	-	-	IAPEN
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	0	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X4E	BANK 1, R4E TBWAL	Bit Name	TBWA7	TBWA6	TBWA5	TBWA4	TBWA3	TBWA2	TBWA1	TBWA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X4F	BANK 1, R4F TBWAH	Bit Name					TBWA 11	TBWA 10	TBWA 9	TBWA 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	P	P
0X05	BANK 2, R5 TM1CR1	Bit Name	TM1S	TM1RC	TM1SS1	-	TM1FF	TM1MOS	TM1IS1	TM1IS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	P	P	P	P
0X06	BANK 2, R6 TM1CR2	Bit Name	TM1M2	TM1M1	TM1M0	TM1SS0	TM1CK3	TM1CK2	TM1CK1	TM1CK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X07	BANK 2, R7 TM1DBH	Bit Name	TM1DB 15	TM1DB 14	TM1DB 13	TM1DB 12	TM1DB 11	TM1DB 10	TM1DB 9	TM1DB 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X8	BANK 2, R8 TM1DBL	Bit Name	TM1DB7	TM1DB6	TM1DB5	TM1DB4	TM1DB3	TM1DB2	TM1DB1	TM1DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X9	BANK 2, R9 TM1DAH	Bit Name	TM1DA 15	TM1DA 14	TM1DA 13	TM1DA 12	TM1DA 11	TM1DA 10	TM1DA 9	TM1DA 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0XA	BANK 2, RA TM1DAL	Bit Name	TM1DA7	TM1DA6	TM1DA5	TM1DA4	TM1DA3	TM1DA2	TM1DA1	TM1DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0XB	BANK 2, RB TM2CR1	Bit Name	TM2S	TM2RC	TM2SS1	-	TM2FF	TM2MOS	TM2IS1	TM2IS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	P	P	P	P
0X0C	BANK 2, RC TM2CR2	Bit Name	TM2M2	TM2M1	TM2M0	TM2SS0	TM2CK3	TM2CK2	TM2CK1	TM2CK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	BANK 2, RD TM2DBH	Bit Name	TM2DB15	TM2DB14	TM2DB13	TM2DB12	TM2DB11	TM2DB10	TM2DB9	TM2DB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0E	BANK 2, RE TM2DBL	Bit Name	TM2DB7	TM2DB6	TM2DB5	TM2DB4	TM2DB3	TM2DB2	TM2DB1	TM2DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	BANK 2, RF TM2DAH	Bit Name	TM2DA15	TM2DA14	TM2DA13	TM2DA12	TM2DA11	TM2DA10	TM2DA9	TM2DA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X10	BANK 2, R10 TM2DAL	Bit Name	TM2DA7	TM2DA6	TM2DA5	TM2DA4	TM2DA3	TM2DA2	TM2DA1	TM2DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X11	BANK 2, R11 TM3CR1	Bit Name	TM3S	TM3RC	TM3SS1	-	TM3FF	TM3MOS	TM3IS1	TM3IS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	P	P	P	P
0X12	BANK 2, R12 TM3CR2	Bit Name	TM3M2	TM3M1	TM3M0	TM3SS0	TM3CK3	TM3CK2	TM3CK1	TM3CK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X13	BANK 2, R13 TM3DBH	Bit Name	TM3DB15	TM3DB14	TM3DB13	TM3DB12	TM3DB11	TM3DB10	TM3DB9	TM3DB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X14	BANK 2, R14 TM3DBL	Bit Name	TM3DB7	TM3DB6	TM3DB5	TM3DB4	TM3DB3	TM3DB2	TM3DB1	TM3DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X15	BANK 2, R15 TM3DAH	Bit Name	TM3DA15	TM3DA14	TM3DA13	TM3DA12	TM3DA11	TM3DA10	TM3DA9	TM3DA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X16	BANK 2, R16 TM3DAL	Bit Name	TM3DA7	TM3DA6	TM3DA5	TM3DA4	TM3DA3	TM3DA2	TM3DA1	TM3DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X17	BANK 2, R17 TM4CR1	Bit Name	TM4S	TM4RC	TM4SS1	-	TM4FF	TM4MOS	TM4IS1	TM4IS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X18	BANK 2, R18 TM4CR2	Bit Name	TM4M2	TM4M1	TM4M0	TM4SS0	TM4CK3	TM4CK2	TM4CK1	TM4CK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	BANK 2, R19 TM4DBH	Bit Name	TM4DB 15	TM4DB 14	TM4DB 13	TM4DB 12	TM4DB 11	TM4DB 10	TM4DB 9	TM4DB 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1A	BANK 2, R1A TM4DBL	Bit Name	TM4DB7	TM4DB6	TM4DB5	TM4DB4	TM4DB3	TM4DB2	TM4DB1	TM4DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	BANK 2, R1B TM4DAH	Bit Name	TM4DA 15	TM4DA 14	TM4DA 13	TM4DA 12	TM4DA 11	TM4DA 10	TM4DA 9	TM4DA 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1C	BANK 2, R1C TM4DAL	Bit Name	TM4DA7	TM4DA6	TM4DA5	TM4DA4	TM4DA3	TM4DA2	TM4DA1	TM4DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	BANK 2, R1D EI01NCR	Bit Name	EI1NRE	-	EI1NR1	EI1NR0	EI0NRE	-	EI0NR1	EI0NR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	P	P	P	0	P	P
0X1E	BANK 2, R1E CMP1CR	Bit Name	C1PRS1	C1PRS0	C1NRS1	C1NRS0	-	CMP1EN	CMP1OE	CP1OUT
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	0	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1F	BANK 2, R1F CMP2CR	Bit Name	C2PRS1	C2PRS0	C2NRS1	C2NRS0	HYSEN2	CMP2EN	CMP2OE	CP2OUT
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X22	BANK 2, R22 CMPESCR	Bit Name	-	-	-	-	-	-	CMP2ES	CMP1ES
		Power-On	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0X23	BANK 2, R23 CMP12NCR	Bit Name	CO2NRE	-	CO2NR1	CO2NR0	CO1NRE	-	CO1NR1	CO1NR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	P	P	P	0	P	P
0X25	BANK 2, R25 CMPTCR1	Bit Name	CMPTEN	VOSF2	VOSF1	VOSF0	-	-	TRIMDU2	TRIMDU1
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X26	BANK 2, R26 CMPTCR2	Bit Name	-	-		TRIMOS			TRIMIS2	TRIMIS1
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	P	0	0	P	P
0X27	BANK 2, R27 TCMP1H	Bit Name	TCMP1HS	-	-	TCMP1H4	TCMP1H3	TCMP1H2	TCMP1H1	TCMP1H0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	P	P	P	P	P
0x28	BANK 2, R28 TCMP1L	Bit Name	TCMP1LS	-	-	TCMP1L4	TCMP1L3	TCMP1L2	TCMP1L1	TCMP1L0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2B	BANK 2, R2B THCMP2H	Bit Name	THCMP2Hs	-	THCMP2H5	THCMP2H4	THCMP2H3	THCMP2H2	THCMP2H1	THCMP2H0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	P	P	P	P	P	P
0x2C	BANK 2, R2C TLCMP2H	Bit Name	TLCMP2HS	-	TLCMP2H5	TLCMP2H4	TLCMP2H3	TLCMP2H2	TLCMP2H1	TLCMP2H0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	P	P	P	P	P	P
0x2D	BANK 2, R2D THCMP2L	Bit Name	THCMP2LS	-	THCMP2L5	THCMP2L4	THCMP2L3	THCMP2L2	THCMP2L1	THCMP2L0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	P	P	P	P	P	P
0x2E	BANK 2, R2E TLCMP2L	Bit Name	TLCMP2LS	-	TLCMP2L5	TLCMP2L4	TLCMP2L3	TLCMP2L2	TLCMP2L1	TLCMP2L0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	P	P	P	P	P	P
0x40	BANK 2, R40 MULMOD	Bit Name	-	-	-	PROD16	MACEN	MACM	SMCAND	SMIER
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	P	P	P	P	P
0x41	BANK 2, R41 PRODH	Bit Name	PROD15	PROD14	PROD13	PROD12	PROD11	PROD10	PROD9	PROD8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x42	BANK 2, R42 PRODL	Bit Name	PROD7	PROD6	PROD5	PROD4	PROD3	PROD2	PROD1	PROD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x43	BANK 2, R43 SFR7	Bit Name	TM4DBSF	-	-	-	TM4SF	TM3SF	TM2SF	TM1SF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	P	P	P	P
0x45	BANK 2, R45 IMR7	Bit Name	-	-	-	-	TM4IE	TM3IE	TM2IE	TM1IE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	P	P
0x47	BANK 2, R47 LOCKPR	Bit Name	LOCKPR7	LOCKPR6	LOCKPR5	LOCKPR4	LOCKPR3	LOCKPR2	LOCKPR1	LOCKPR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x48	BANK 2, R48 LOCKCR	Bit Name	LOCKEN							
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	0	0	0	0
0x05	BANK 3, R5 EIOPWMPE0	Bit Name			PWMCBEN	PWMCEN	PWMBBEN	PWMBEN	PWMABEN	PWMAEN
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P
0x06	BANK 3, R6 EOPWMPE0	Bit Name			PWMEEN	PWMEOE				
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	0	0	0	0
0x07	BANK 3, R7 EIOPHAPE	Bit Name			HACEN1	HACEN0	HABEN1	HABEN0	HAAEN1	HAAEN0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	BANK 3, R9 T5CRH	Bit Name	T5SP	T5CLR		T5CKS0	T5PRE3	T5PRE2	T5PRE1	T5PRE0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	0	P	P	P	P	P
0x0A	BANK 3, RA T5CRL	Bit Name	T5MS	T5CDIR	DECLR	FT6PRE SEL				TMR5P
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	0	0	0	P
0x0B	BANK 3, RB T6CRH	Bit Name	T6SP	T6CLR	T6CKS1	T6CKS0	T6PRE3	T6PRE2	T6PRE1	T6PRE0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0C	BANK 3, RC T6CRL	Bit Name	T6TMS3	T6TMS2	T6TMS1	T6TMS0	T6TDIR1	T6TDIR0	RPHT6	TMR6P
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0D	BANK 3, RD PWMCR1H	Bit Name			T6E PWMCB	T6E PWMC	T6E PWMBB	T6E PWMB	T6E PWMAB	T6E PWMA
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P
0x0E	BANK 3, RE PWMCR1L	Bit Name			T5E PWMCB	T5E PWMC	T5E PWMBB	T5E PWMB	T5E PWMAB	T5E PWMA
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P
0x0F	BANK 3, RF PWMCR2H	Bit Name	CPE	T6E PWME	CPMTE			TSYN2	TSYN1	TSYN0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	0	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	BANK 3, R10 PWMCR2L	Bit Name	MTF	TSMS2	TSMS1	TSMS0				
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	0	0	0	0
0x11	BANK 3, R11 T5OPMS	Bit Name				T5CMS		T5BMS		T5AMS
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	P	0	P	0	P
0x12	BANK 3, R12 T6OPMS	Bit Name	T6CM3	T6CM2	T6CM1	T6CM0	T6MS1	T6MS0		
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	0	0
0x13	BANK 3, R13 ASPWM	Bit Name			PWMCBAS	PWMCAS	PWMBBAS	PWMBAS	PWMABAS	PWMAAS
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P
0x14	BANK 3, R14 LVPWM	Bit Name			PWMCBLV	PWMCLV	PWMBBLV	PWMBLV	PWMABLV	PWMALV
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P
0x15	BANK 3, R15 SLPWM	Bit Name							PWMEAS	PWMELV
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0x16	BANK 3, R16 COPH	Bit Name		HACCHP	HABCHP	HAACHP		HACNHP	HABNHP	HAANHP
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	0	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x17	BANK 3, R17 COPL	Bit Name			CPWMCB	CPWMC	CPWMBB	CPWMB	CPWMAB	CPWMA
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P
0x18	BANK 3, R18 MCOPH	Bit Name		MHACCHP	MHABCHP	MHAACHP		MHACNHP	MHABNHP	MHAANHP
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	0	P	P	P
0x19	BANK 3, R19 MCOPL	Bit Name			MCPWMCB	MCPWMC	MCPWMBB	MCPWMB	MCPWMAB	MCPWMA
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P
0x1A	BANK 3, R1A T5DECR	Bit Name		DEADTCF	DEADTBF	DEADTAF		DEADTCE	DEADTBE	DEADTAE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	0	P	P	P
0x1B	BANK 3, R1B T5DEB	Bit Name	T5DE7	T5DE6	T5DE5	T5DE4	T5DE3	T5DE2	T5DE1	T5DE0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x1C	BANK 3, R1C HACRH	Bit Name	HAMTE	HASAMP2	HASAMP1	HASAMP0	HANRE	HANRHL2	HANRHL1	HANRHL0
		Power-On	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x1D	BANK 3, R1D HACRL	Bit Name	HANRPRE1	HANRPRE0	HAER2COID			HACSF	HABSF	HAASF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	0	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1E	BANK 3, R1E BRKCR1H	Bit Name	CP1 LVBRK						EIT1 LVBRK	EIT0 LVBRK
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	0	0	P	P
0x1F	BANK 3, R1F BRKCR1L	Bit Name	CP1 BRKEN						EIT1 BRKEN	EIT0 BRKEN
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	0	0	P	P
0x20	BANK 3, R20 BRKCR2H	Bit Name				BRKFAC		BRKM1	BRKM0	BRK PWME
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	P	0	P	P	P
0x21	BANK 3, R21 BRKCR2L	Bit Name			BRK PWMCB	BRK PWMC	BRK PWMBB	BRK PWMB	BRK PWMAB	BRK PWMA
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P
0x22	BANK 3, R22 TRADCR	Bit Name	TRAD EN2	TRAD TS2	TRAD2 DIR1	TRAD2 DIR0	TRAD EN1	TRAD TS1	TRAD1 DIR1	TRAD1 DIR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x23	BANK 3, R23 TSF1H	Bit Name	HAEDG EF	MTRF	TRAD2F	TRAD1F	COIDF	BRKF	BRKS	PWMES
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x24	BANK 3, R24 TSF1L	Bit Name		PWMCS	PWMBS	PWMAS	T6MTF	T6RF	T5MTF	T5RF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x25	BANK 3, R25 SETM1H	Bit Name	IEHC	MTRS			COIDS	BRKFS		
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	0	0	P	P	0	0
0x26	BANK 3, R26 SETM1L	Bit Name					T6MTS	T6RS	T5MTS	T5RS
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	P	P
0x27	BANK 3, R27 RSTM1H	Bit Name		MTRR			COIDR	BRKFR		
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	0	0	P	P	0	0
0x28	BANK 3, R28 RSTM1L	Bit Name					T6MTR	T6RR	T5MTR	T5RR
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	P	P
0x2B	BANK 3, R2B T5VALH	Bit Name	T5VAL 15	T5VAL 14	T5VAL 13	T5VAL 12	T5VAL 11	T5VAL 10	T5VAL 9	T5VAL 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x2C	BANK 3, R2C T5VALL	Bit Name	T5VAL7	T5VAL6	T5VAL5	T5VAL4	T5VAL3	T5VAL2	T5VAL1	T5VAL0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x2D	BANK 3, R2D T5PDH	Bit Name	T5PD15	T5PD14	T5PD13	T5PD12	T5PD11	T5PD10	T5PD9	T5PD8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2E	BANK 3, R2E T5PDL	Bit Name	T5PD7	T5PD6	T5PD5	T5PD4	T5PD3	T5PD2	T5PD1	T5PD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x2F	BANK 3, R2F T5ACDH	Bit Name	T5ACD 15	T5ACD 14	T5ACD 13	T5ACD 12	T5ACD 11	T5ACD 10	T5ACD 9	T5ACD 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x30	BANK 3, R30 T5ACDL	Bit Name	T5ACD7	T5ACD6	T5ACD5	T5ACD4	T5ACD3	T5ACD2	T5ACD1	T5ACD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x31	BANK 3, R31 T5BCDH	Bit Name	T5BCD 15	T5BCD 14	T5BCD 13	T5BCD 12	T5BCD 11	T5BCD 10	T5BCD 9	T5BCD 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x32	BANK 3, R32 T5BCDL	Bit Name	T5BCD7	T5BCD6	T5BCD5	T5BCD4	T5BCD3	T5BCD2	T5BCD1	T5BCD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x33	BANK 3, R33 T5CCDH	Bit Name	T5CCD 15	T5CCD 14	T5CCD 13	T5CCD 12	T5CCD 11	T5CCD 10	T5CCD 9	T5CCD 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x34	BANK 3, R34 T5CCDL	Bit Name	T5CCD7	T5CCD6	T5CCD5	T5CCD4	T5CCD3	T5CCD2	T5CCD1	T5CCD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x35	BANK 3, R35 T5ACDMH	Bit Name	T5ACD M15	T5ACD M14	T5ACD M13	T5ACD M12	T5ACD M11	T5ACD M10	T5ACD M9	T5ACD M8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x36	BANK 3, R36 T5ACDML	Bit Name	T5ACD M7	T5ACD M6	T5ACD M5	T5ACD M4	T5ACD M3	T5ACD M2	T5ACD M1	T5ACD M0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x37	BANK 3, R37 T5BCDMH	Bit Name	T5BCD M15	T5BCD M14	T5BCD M13	T5BCD M12	T5BCD M11	T5BCD M10	T5BCD M9	T5BCD M8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x38	BANK 3, R38 T5BCDML	Bit Name	T5BCD M7	T5BCD M6	T5BCD M5	T5BCD M4	T5BCD M3	T5BCD M2	T5BCD M1	T5BCD M0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x39	BANK 3, R39 T5CCDMH	Bit Name	T5CCD M15	T5CCD M14	T5CCD M13	T5CCD M12	T5CCD M11	T5CCD M10	T5CCD M9	T5CCD M8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x3A	BANK 3, R3A T5CCDML	Bit Name	T5CCD M7	T5CCD M6	T5CCD M5	T5CCD M4	T5CCD M3	T5CCD M2	T5CCD M1	T5CCD M0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3B	BANK 3, R3B TRAD1VH	Bit Name	TRAD1V15	TRAD1V14	TRAD1V13	TRAD1V12	TRAD1V11	TRAD1V10	TRAD1V9	TRAD1V8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x3C	BANK 3, R3C TRAD1VL	Bit Name	TRAD1V7	TRAD1V6	TRAD1V5	TRAD1V4	TRAD1V3	TRAD1V2	TRAD1V1	TRAD1V0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x3D	BANK 3, R3D TRAD2VH	Bit Name	TRAD2V15	TRAD2V14	TRAD2V13	TRAD2V12	TRAD2V11	TRAD2V10	TRAD2V9	TRAD2V8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x3E	BANK 3, R3E TRAD2VL	Bit Name	TRAD2V7	TRAD2V6	TRAD2V5	TRAD2V4	TRAD2V3	TRAD2V2	TRAD2V1	TRAD2V0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x3F	BANK 3, R3F T6VALH	Bit Name	T6VAL15	T6VAL14	T6VAL13	T6VAL12	T6VAL11	T6VAL10	T6VAL9	T6VAL8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x40	BANK 3, R40 T6VALL	Bit Name	T6VAL7	T6VAL6	T6VAL5	T6VAL4	T6VAL3	T6VAL2	T6VAL1	T6VAL0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x41	BANK 3, R41 T6PDH	Bit Name	T6PD15	T6PD14	T6PD13	T6PD12	T6PD11	T6PD10	T6PD9	T6PD8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x42	BANK 3, R42 T6PDL	Bit Name	T6PD7	T6PD6	T6PD5	T6PD4	T6PD3	T6PD2	T6PD1	T6PD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x43	BANK 3, R43 T6CDH	Bit Name	T6CD15	T6CD14	T6CD13	T6CD12	T6CD11	T6CD10	T6CD9	T6CD8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x44	BANK 3, R44 T6CDL	Bit Name	T6CD7	T6CD6	T6CD5	T6CD4	T6CD3	T6CD2	T6CD1	T6CD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x45	BANK 3, R43 T6CDMH	Bit Name	T6CD M15	T6CD M14	T6CD M13	T6CD M12	T6CD M11	T6CD M10	T6CD M9	T6CD M8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x46	BANK 3, R44 T6CDML	Bit Name	T6CD M7	T6CD M6	T6CD M5	T6CD M4	T6CD M3	T6CD M2	T6CD M1	T6CD M0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x4C	BANK 3, R4C SFR9	Bit Name	T5PDM SF	T5ONEM SF	IRT5CSF	IRT5BSF	IRT5ASF	IFT5CSF	IFT5BSF	IFT5ASF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x4D	BANK 3, R4D SFR10	Bit Name	MTRSF	BRKSF	HAEGSF	HACO SF	HAERR SF	T6PDM SF	IRT6SF	IFT6SF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4E	BANK 3, R4E IMR9	Bit Name	T5PDMIE	T5ONEMIE	IRT5CIE	IRT5BIE	IRT5AIE	IFT5CIE	IFT5BIE	IFT5AIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x4F	BANK 3, R4F IMR10	Bit Name	MTRIE	BRKIE	HAEGIE	HACOIE	HAERRIE	T6PDMIE	IRT6IE	IFT6IE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

U: Unknown or don't care.

P: Previous value before reset.

C: Same as Code option

t: Check Table 6

6.6 Interrupt

The EM88F794N has 31 interrupts (7 external, 24 internal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal/External	Reset	-	-	0	High 0
External	INT	ENI + EXIE0=1	EXSF0	2	27
		ENI + EXIE1=1	EXSF1		
External	Pin Change	ENI + P5ICIE=1	P5ICSF	4	28
		ENI + P6ICIE=1	P6ICSF		
		ENI + P7ICIE=1	P7ICSF		
Internal	LVD	ENI+LVDEN & LVDIE=1	LVDSF	8	29
External	Comparator1	ENI+CMP1IE=1	CMP1SF	A	17
External	Comparator2	ENI+CMP2IE=1	CMP2SF	E	18
Internal	AD	ENI + ADIE=1	ADSF	10	12
External	System hold	ENI+SHIE	SHSF	3A	21
Internal	MTR	ENI+MTRIE=1	MTRSF	3C	22
Internal	BRK	ENI+BRKIE=1	BRKSF	3E	16
Internal	HAEG	ENI+HAEGIE=1	HAEGSF	40	11
Internal	T5PDM	ENI + T5PDMIE=1	T5PDMSF	42	1
Internal	T5ONEM	ENI + T5ONEMIE=1	T5ONEMSF	44	2
Internal	IRT5A	ENI + IRT5AIE=1	IRT5ASF	46	3
Internal	IRT5B	ENI + IRT5BIE=1	IRT5BSF	48	4
Internal	IRT5C	ENI + IRT5CIE=1	IRT5CSF	4A	5
Internal	IFT5A	ENI + IFT5AIE=1	IFT5ASF	4C	6
Internal	IFT5B	ENI + IFT5BIE=1	IFT5BSF	4E	7
Internal	IFT5C	ENI + IFT5CIE=1	IFT5CSF	50	8
Internal	HAERR	ENI + HAERRIE=1	HAERRSF	52	9
Internal	HACO	ENI + HACOIE=1	HACOSF	54	10
Internal	T6PDM	T6PDMIE=1	T6PDMSF	56	13
Internal	IRT6	ENI + IRT6IE=1	IRT6SF	58	14
Internal	IFT6	ENI + IFT6IE=1	IFT6SF	5A	15
Internal	TM1	ENI + TM1IE=1	TM1SF	5C	26
Internal	TM2	ENI + TM2IE=1	TM2SF	5E	25
Internal	TM3	ENI + TM3IE=1	TM3SF	60	24
Internal	TM4	ENI + TM4IE=1	TM4SF	62	23

Bank 0 R14~R19, Bank 2 R43, Bank 3 R4C and R4D are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank 0 R1B~R20, Bank2 R45, Bank 3 R4E and R4F is the interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICSF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse less than **4 system clocks time** is eliminated as noise)**.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 002H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 (Bit 0~Bit 6) and R4 register will be saved by hardware. If another interrupt occurs, the ACC, R3 (Bit 0~Bit 6) and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC,R1, R3 (Bit 0~Bit 6) and R4 will be pushed back.

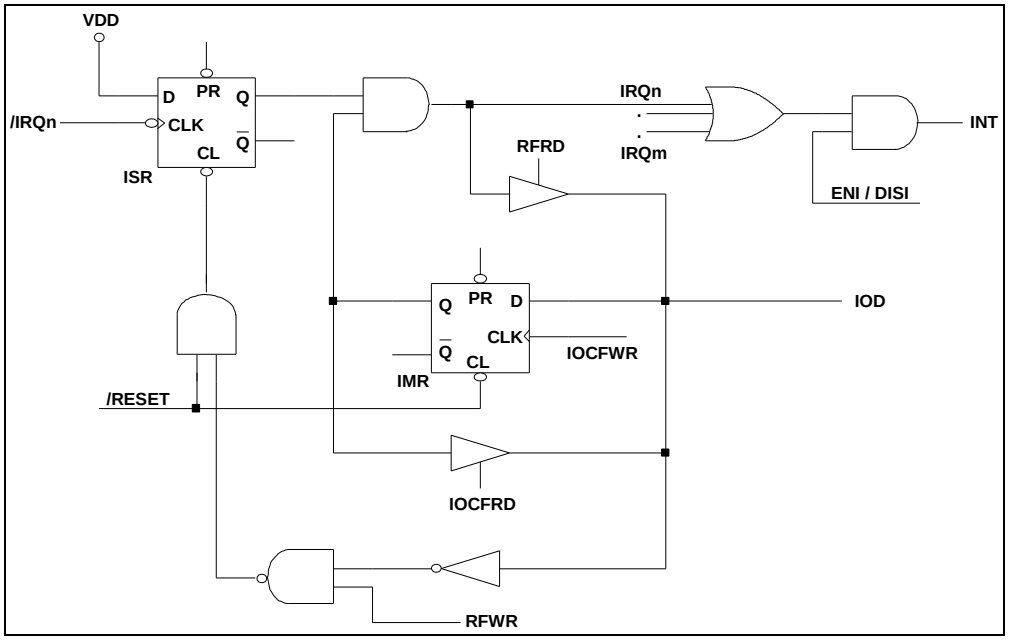


Figure 6-10 Interrupt Input Circuit

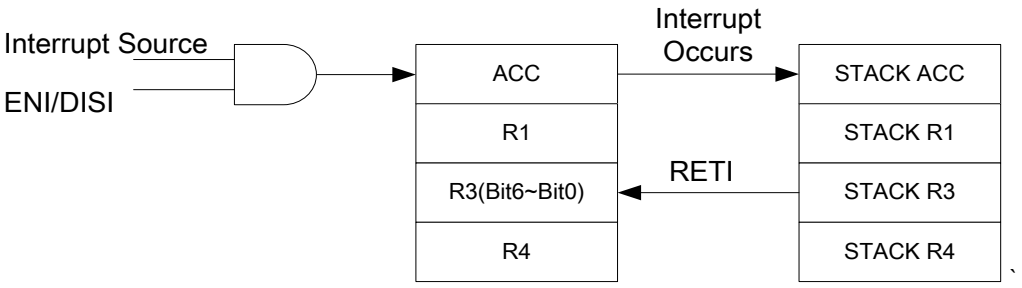


Figure 6-11 Interrupt Backup Diagram

6.7 A/D Converter

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x3E	ADCR1	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x3F	ADCR2		VPIS2	ADIM	ADCMS	VPIS1	VPIS0	VREFP	
				R/W	R/W	R/W	R/W	R/W	R/W	
Bank 0	0x40	ADISR					ADIS3	ADIS2	ADIS1	ADIS0
							R/W	R/W	R/W	R/W
Bank 0	0x41	ADER1	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE7
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x43	ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x44	ADDH	ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
			R	R	R	R	R	R	R	R
Bank 0	0x45	ADCVL	ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
			R	R	R	R	R	R	R	R
Bank 0	0x46	ADCVH	ADCD15	ADCD14	ADCD13	ADCD12	ADCD11	ADCD10	ADCD9	ADCD8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x47	ADCONBUF	ADBFEN	ADBFOVR	ADBFINT	STPMK		ADBFPTR2	ADBFPTR1	ADBFPTR0
			R/W	R/W	R/W	R/W		R/W	R/W	R/W
Bank 0	0x10	WUCR2				ADWK				
						R/W				
Bank 0	0x14	SFR1				ADSF				
						R/W				
Bank 0	0x1B	IMR1				ADIE				
						R/W				

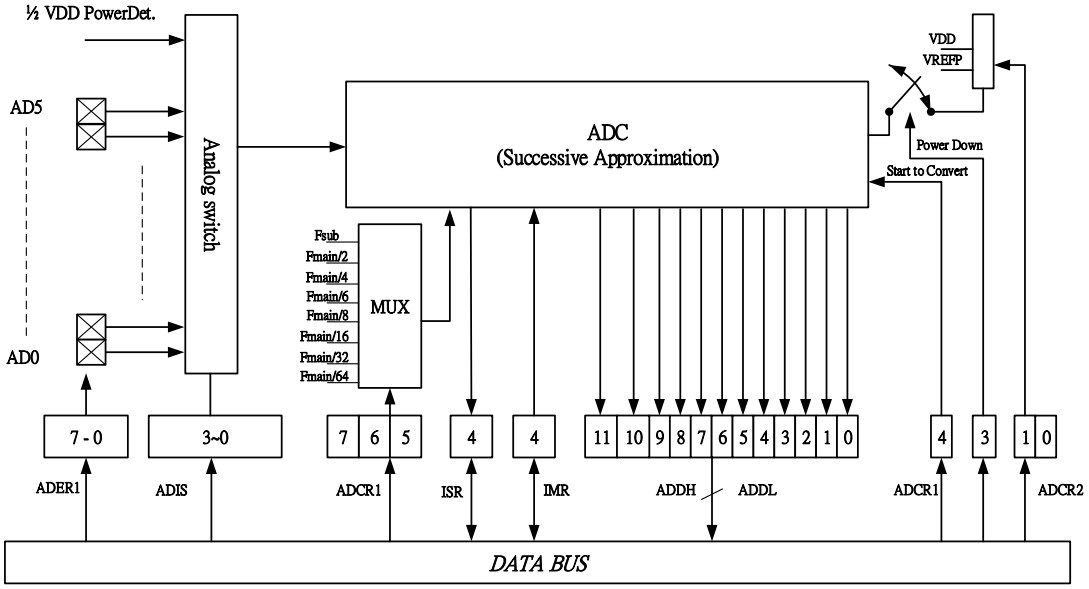


Figure 6-12 AD Converter

This is a 12-bit successive approximation register analog to digital converter (SAR ADC). There are two reference voltages for SAR ADC. The positive reference voltage can select internal AVDD, internal voltage sources or external input pin by setting the VREFP and VPIS [2:0] bits in ADCR2. Connecting to external positive reference voltage provides more accuracy than using internal AVDD.

6.7.1 ADC Data Register

When the AD conversion is completed, the result is loaded to the ADDH and ADDL. And the ADSF is set if ADIE is enabled.

6.7.2 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation AD converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample and hold capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 4 μs for each kilo ohms of the analog source impedance and at least 4 μs for the low-impedance source. The maximum recommended impedance for the analog source is 10KΩ at VDD = 5V. After the analog input channel is selected; this acquisition time must be done before AD conversion can be started.

6.7.3 A/D Conversion Time

CKR[2:0] selects the conversion time (T_{CT}) in terms of instruction cycles. This allows the MCU to run at maximum frequency without sacrificing accuracy of AD conversion. For the EM88F794N, the conversion time per bit is about 0.5 μs. The following table shows the relationship between T_{CT} and the maximum operating frequencies.

System Mode	CKR2~0	Clock Rate	Max. System Operation Frequency in 3~3.8V	Max. System Operation Frequency in 3.8~4.5V	Max. System Operation Frequency in 4.5~5.5V
Normal Mode	000	F_{HIRC}/16	20 MHz	28 MHz	32 MHz
	001	F_{HIRC}/8	20 MHz	28 MHz	32 MHz
	010	F_{HIRC}/4	-	-	20 MHz
	011	F_{HIRC}/2	-	-	-
	100	F_{HIRC}/64	20 MHz	28 MHz	32 MHz
	101	F_{HIRC}/32	20 MHz	28 MHz	32 MHz
	110	F_{HIRC}/6	-	20 MHz	32 MHz
	111	F_{Sub}	Fs	Fs	Fs
Green Mode	xxx	F_{Sub}	Fs	Fs	Fs

6.7.4 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TM1~TM4, PWM timers and AD conversion.

The ADC Conversion is considered completed as determined by**:**

1. The ADRUN bit is cleared to “0”.
2. The ADSF bit is set to “1”.
3. The ADWK bit is set to “1”. Wakes up from ADC conversion (where it remains in operation during sleep mode).
4. Wake up and execution of the next instruction if the ADIE bit is enabled and the “DISI” instruction is executed.
5. Wake up and enters into Interrupt vector if the ADIE bit is enabled and the “ENI” instruction is executed.
6. Enters into an Interrupt vector if the ADIE bit is enabled and the “ENI” instruction is executed.

The results are fed into the ADDL and ADDH registers when the conversion is completed. If the ADWK is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADP bit is.

6.7.5 Programming Process/Considerations

Follow these steps to obtain data from the ADC**:**

1. Write to the six bits (ADE[5:0]) on the ADER1 register to define the characteristics of P57, P62, P66~P67 and P70~P71 (digital I/O, analog channels, or voltage reference pin)
2. Write to the ADCON register to configure the AD module:
   a) Select the ADC input channel (ADIS[3:0])
   b) Define the AD conversion clock rate (CKR[2:0])
   c) Select the VREFP input source of the ADC
   d) Set the ADP bit to 1 to begin sampling
3. Set the ADWK bit, if the wake-up function is employed
4. Set the ADIE bit, if the interrupt function is employed
5. Write “ENI” instruction, if the interrupt function is employed
6. Set the ADRUN bit to 1
7. Write “SLEP” instruction or Polling.
8. Wait for wake-up or for the ADRUN bit to be cleared to “0” , status flag (ADSF) is set “1” or ADC interrupt occurs.
9. Read the ADDL and ADDH conversion data registers. If the ADC input channel changes at this time, the ADDL and ADDH values can be cleared to ‘0’.
10. Clear the status flag (ADSF).
11. For next conversion, go to Step 1 or Step 2 as required. At least two T_{CT} is required before the next acquisition starts.

NOTE
In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion

6.7.6 Buffer Mode Programming Process/Considerations

1. There are eight buffers. Every buffer is following its corresponding ADIS and STPMK. ADIS and STPMK for every buffer must be accessed by ADBFPTR.
2. Following are basic procedures for using buffer mode and single mode
   A. The bit ADBFEN is set to “1”.
   B. Set ADIS and STPMK for every buffer with ADBFPTR. STPMK=0 means ADC will work and result of conversion data will be stored in this buffer.

C. After setting ADRUN, ADBFPTR will be reset.

D. If STPMK of buffer (x: ADBFPTR) is cleared to 0, ADC will start to convert with the channel set by ADIS and conversion data will be stored in buffer (x: ADBFPTR). Then, ADBFPTR= ADBFPTR+1(automatically by hardware).

E. If STPMK of buffer (x: ADBFPTR) is cleared to 0, the actions would be the same as above procedure. If STPMK of eight buffers are all cleared to 0, the interrupt will be triggered (if corresponding interrupt is enabled) after eight consecutive ADC conversions.

F. If STPMK of buffer (x: ADBFPTR) is set to 1(stop mark), ADC will stop working and interrupt will be triggered (if corresponding interrupt is enabled).

3. For buffer and continuous mode, the procedures are:

   A. Procedure 2-A to 2-F (like above procedures). Then, ADBFPTR will be reset.

   B. Repeat procedure 3-A until ADRUN is set by software.

4. Compare mode can't be used in buffer mode.

5. The buffers (Buffers 0~7) are read at corresponding interrupt event is suggested. Or ADBFOVR will be set. ADBFOVR=1 means any of buffers is overwritten (not read).

6. In buffer mode and single mode, setting ADRUN will let ADC start to work. Then, ADC will keep working until STPMK of the buffer is set to1. Therefore, ADRUN is cleared to 0 by hardware. But In buffer mode and continuous mode, setting ADRUN will also let ADC start to work. And ADC will keep working until ADRUN is cleared by software.

7. When ADC buffer is disabled, ADBFPTR is always equal to 0 and ADC is used to common AD conversion.

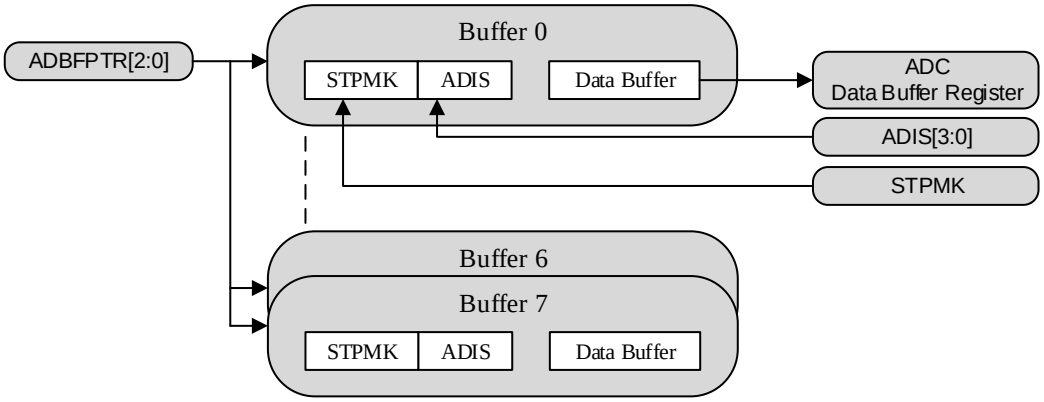


Figure 6-13 Block Diagram of ADC Buffer Mode

NOTE
In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion

6.7.7 Programming Process for Detecting Internal VDD

VDD is detected within the operation, as described in the previous section. The difference is that before starting the ADC conversion, the first detection of VDD is ready. Therefore in Detecting VDD:

It should be noted that before starting the AD conversion operation, the channel has to be switched to 1/2VDD channel, the voltage divider needs to start before AD can be converted. Several points to note is that, precise conversion values can be added in the VDD Pin capacitance. Taking the average of more than two conversions or the last few strokes of data can help increasing the reliability of the data.

Generally before VDD is detected, the channel should not be switched to 1/2VDD, as it has always been a DC current consumption. Instead, it must be switched to another channel analog multiplexer, and it will be shut out of the resistor divider.

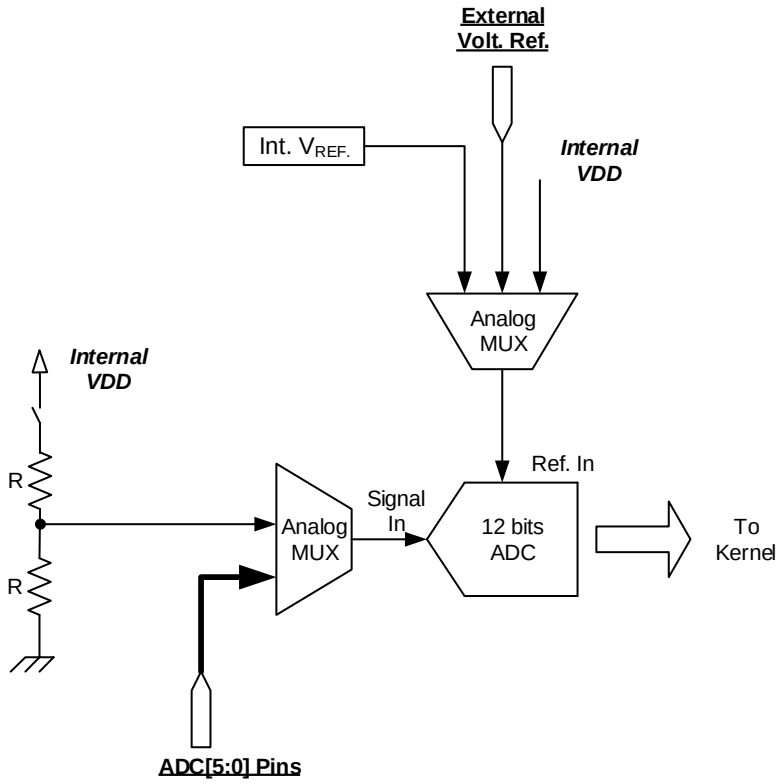


Figure 6-14 ADC and VDD Detection Block Diagram

6.8 Timer

There are four Timers in the EM88F794N. TM1 ~ TM4 are 16 bits up-counter.

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 2	0x05	TM1CR1	TM1S	TM1RC	TM1SS1		TM1FF	TM1MOS	TM1IS1	TM1IS0
			R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bank 2	0x06	TM1CR2	TM1M2	TM1M1	TM1M0	TM1SS0	TM1CK3	TM1CK2	TM1CK1	TM1CK0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x07	TM1DBH	TM1DB 15	TM1DB 14	TM1DB 13	TM1DB 12	TM1DB 11	TM1DB 10	TM1DB 9	TM1DB 8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x08	TM1DBL	TM1DB7	TM1DB6	TM1DB5	TM1DB4	TM1DB3	TM1DB2	TM1DB1	TM1DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x09	TM1DAH	TM1DA 15	TM1DA 14	TM1DA 13	TM1DA 12	TM1DA 11	TM1DA 10	TM1DA 9	TM1DA 8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x0A	TM1DAL	TM1DA7	TM1DA6	TM1DA5	TM1DA4	TM1DA3	TM1DA2	TM1DA1	TM1DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x0B	TM2CR1	TM2S	TM2RC	TM2SS1		TM2FF	TM2MOS	TM2IS1	TM2IS0
			R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bank 2	0x0C	TM2CR2	TM2M2	TM2M1	TM2M0	TM2SS0	TM2CK3	TM2CK2	TM2CK1	TM2CK0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x0D	TM2DBH	TM2DB15	TM2DB14	TM2DB13	TM2DB12	TM2DB11	TM2DB10	TM2DB9	TM2DB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x0E	TM2DBL	TM2DB7	TM2DB6	TM2DB5	TM2DB4	TM2DB3	TM2DB2	TM2DB1	TM2DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x0F	TM2DAH	TM2DA 15	TM2DA 14	TM2DA 13	TM2DA 12	TM2DA 11	TM2DA 10	TM2DA 9	TM2DA 8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x10	TM2DAL	TM2DA7	TM2DA6	TM2DA5	TM2DA4	TM2DA3	TM2DA2	TM2DA1	TM2DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x11	TM3CR1	TM3S	TM3RC	TM3SS1		TM3FF	TM3MOS	TM3IS1	TM3IS0
			R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bank 2	0x12	TM3CR2	TM3M2	TM3M1	TM3M0	TM3SS0	TM3CK3	TM3CK2	TM3CK1	TM3CK0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x13	TM3DBH	TM3DB 15	TM3DB 14	TM3DB 13	TM3DB 12	TM3DB 11	TM3DB 10	TM3DB 9	TM3DB 8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x14	TM3DBL	TM3DB7	TM3DB6	TM3DB5	TM3DB4	TM3DB3	TM3DB2	TM3DB1	TM3DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x15	TM3DAH	TM3DA 15	TM3DA 14	TM3DA 13	TM3DA 12	TM3DA 11	TM3DA 10	TM3DA 9	TM3DA 8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x16	TM3DAL	TM3DA7	TM3DA6	TM3DA5	TM3DA4	TM3DA3	TM3DA2	TM3DA1	TM3DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bank 2	0x17	TM4CR1	TM4S	TM4RC	TM4SS1		TM4FF	TM4MOS	TM4IS1	TM4IS0
			R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bank 2	0x18	TM4CR2	TM4M2	TM4M1	TM4M0	TM4SS0	TM4CK3	TM4CK2	TM4CK1	TM4CK0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x19	TM4DBH	TM4DB 15	TM4DB 14	TM4DB 13	TM4DB 12	TM4DB 11	TM4DB 10	TM4DB 9	TM4DB 8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x1A	TM4DBL	TM4DB7	TM4DB6	TM4DB5	TM4DB4	TM4DB3	TM4DB2	TM4DB1	TM4DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x1B	TM4DAH	TM4DA 15	TM4DA 14	TM4DA 13	TM4DA 12	TM4DA 11	TM4DA 10	TM4DA 9	TM4DA 8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x1C	TM4DAL	TM4DA7	TM4DA6	TM4DA5	TM4DA4	TM4DA3	TM4DA2	TM4DA1	TM4DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x43	SFR7	TM4DBSF				TM4SF	TM3SF	TM2SF	TM1SF
			F				F	F	F	F
Bank 2	0x45	IMR7					TM4IE	TM3IE	TM2IE	TM1IE
							R/W	R/W	R/W	R/W

6.8.1 Timer/Counter mode

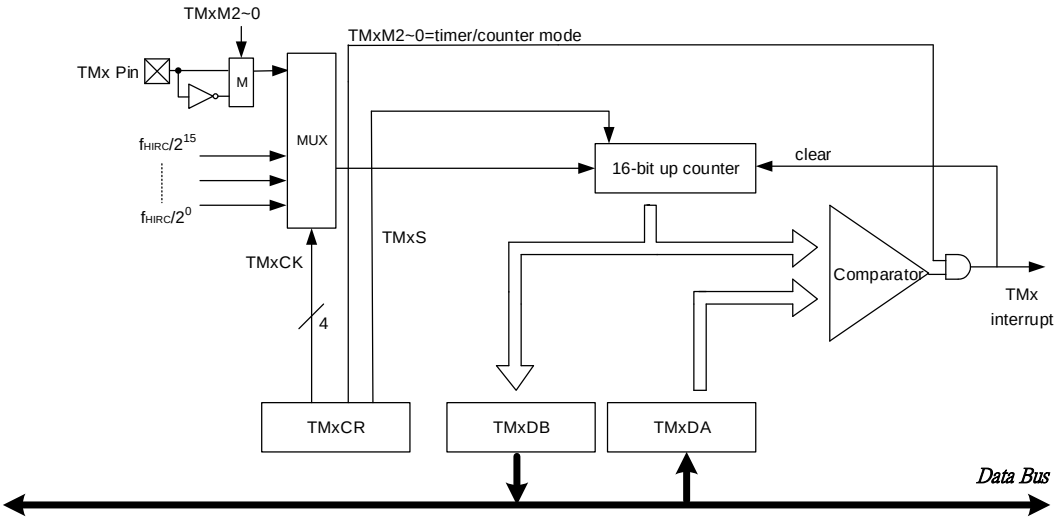


Figure 6-15 Timer/Counter Modes

In Timer/Counter mode, counting up is performed using internal clock or TMx pin. When the contents of up-counter are matched the TMxDA, then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared. The current contents of up-counter are loaded into TMxDB by setting TMxRC to “1”.

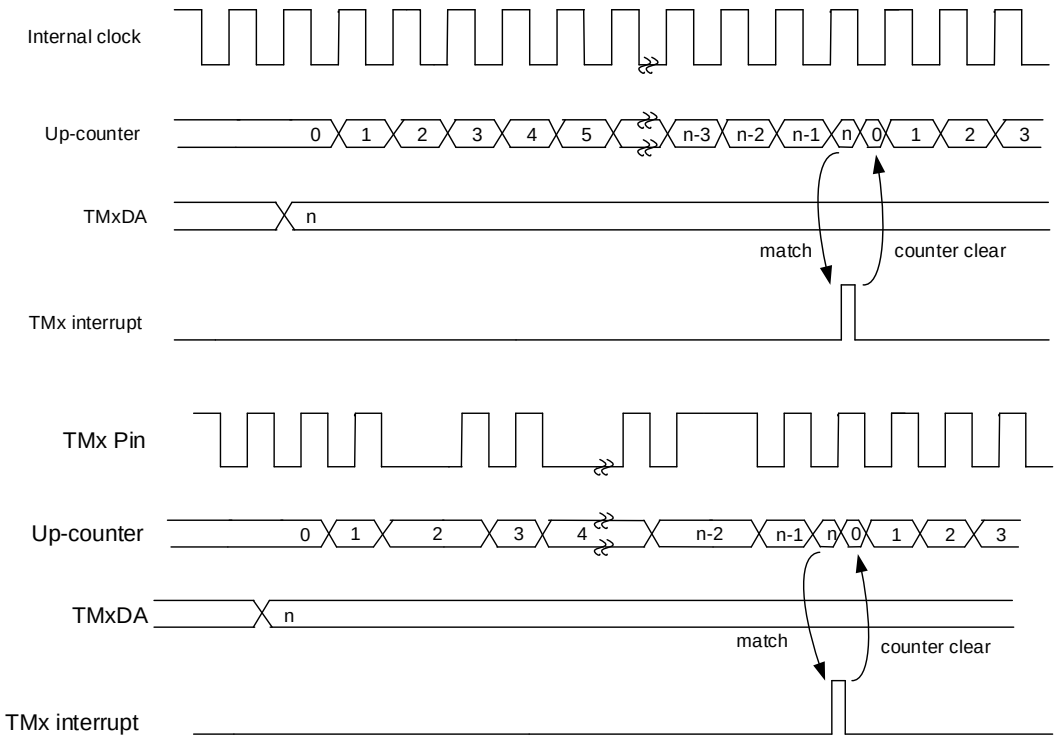


Figure 6-16 Timer/Counter Mode Waveforms

6.8.2 Window Mode

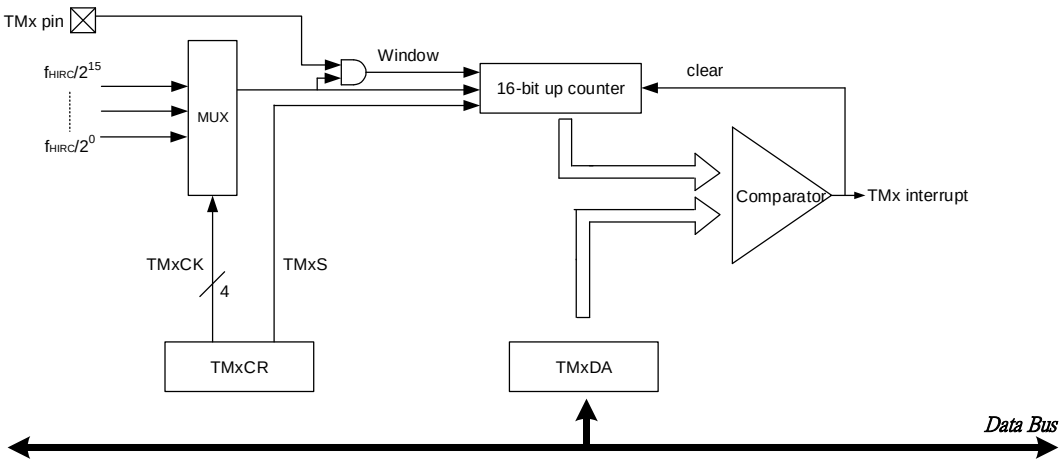


Figure 6-17 Window Mode

In Window mode, countering up is performed on rising edge of the pulse that is logical AND of an internal clock and the TMx pin (window pulse). When the contents of up-counter match the TMxDA, an interrupt is generated and counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

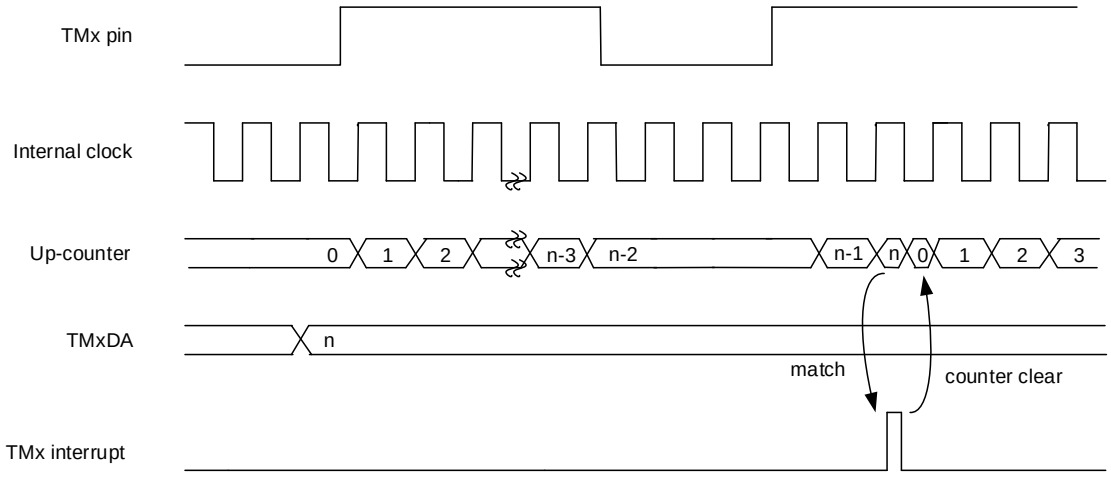


Figure 6-18 Window Mode Waveforms

6.8.3 Capture Mode

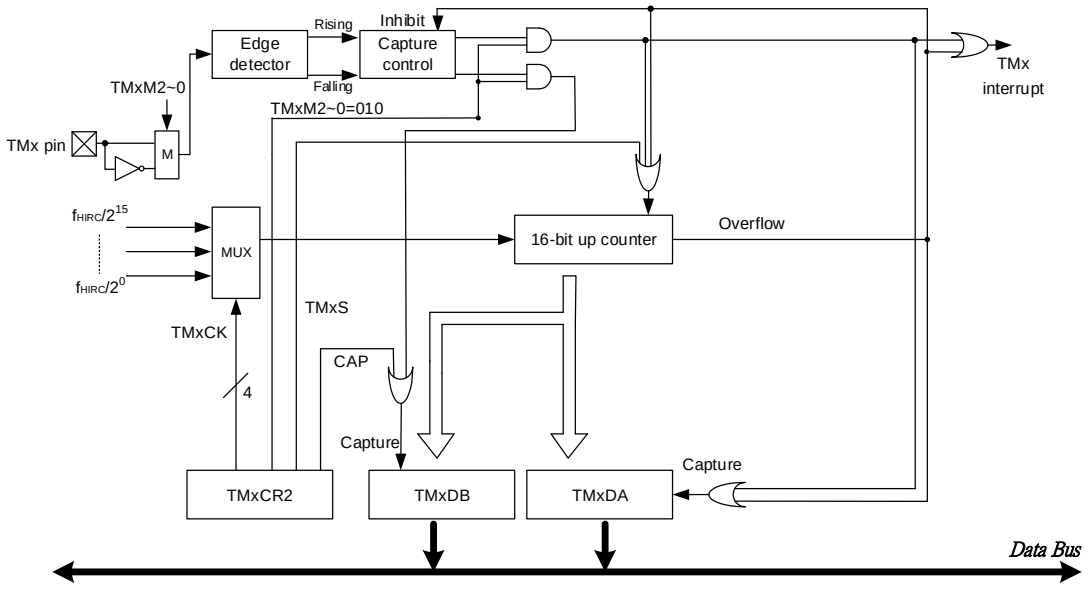


Figure 6-19 Capture Mode

In Capture mode, the pulse width, period and duty of the TMx input pin are measured in this mode, which can be used to decoding the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of TMx pin , the contents of counter is loaded into TMxDA, then the counter is cleared and interrupt is generated. On the falling (rising) edge of TMx pin, the contents of counter are loaded into TMxDB. At this time, the counter is still countering.

Once the next rising edge of TMx pin is triggered, the contents of counter are loaded into TMxDA, the counter is cleared and interrupt is generated again. If overflow before the edge is detected, the 0xFFFF is loaded into TMxDA and the overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TMxDA value is 0xFFFF. After an interrupt (capture to TMxDA or overflow detection) is generated, capture and overflow detection are halted until TMxDA is read out.

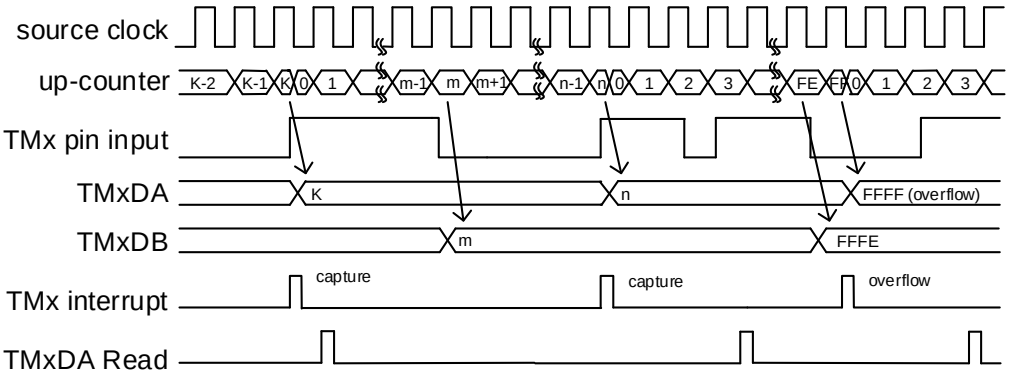
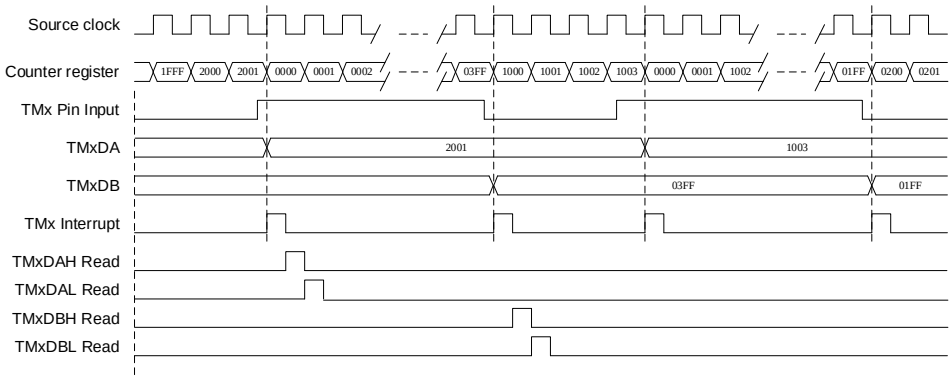


Figure 6-20 (a) Capture Mode Waveform

TM4 Capture Mode

TM4DBSF, another flag of TM4, is used in capture mode. On the rising (falling) edge of TM4 pin, TM4SF is set as one, the contents of counter are loaded into TM4DA, then the counter is cleared and an interrupt is generated. On the falling (rising) edge of TM4 pin, TM4DBSF is set as one, the contents of counter are loaded into TM4DB. At the same time, the counter is still countering. Once the next rising edge of TM4 pin triggers, the contents of counter are loaded into TM4DA, the counter is cleared and the interrupt is generated again.

When a new interrupt is generated, the new capture value will overwrite the TM4DA or



TM4DB, whether old data in TM4DA and TM4DB is read out or not.

Figure 6-20 (b) Capture Mode Waveform (only for Timer 4)

6.8.4 Programmable Divider Output Mode and Pulse Width Modulation Mode

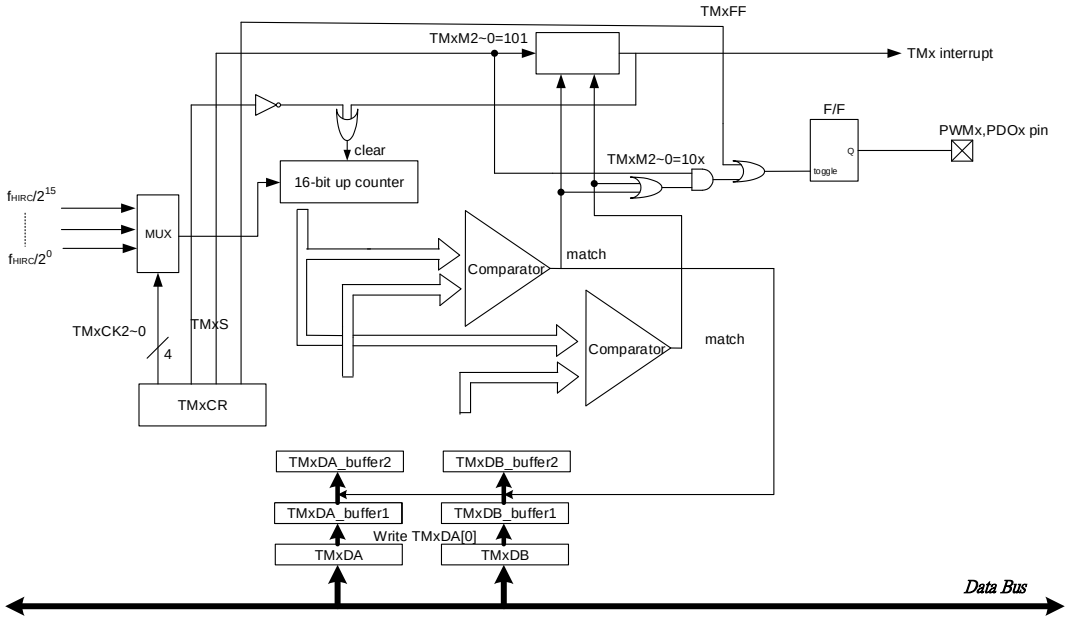


Figure 6-21 PWM/PDO Mode

6.8.5 PDO

In Programmable Divider Output (PDO) mode, counting up is performed using internal clock. The contents of TMxDA are compared with the contents of up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to PDO pin. This mode can generate 50% duty pulse output. The PDO pin is initialized to “0” during reset. A TMx interrupt is generated each time the PDO output is toggled.

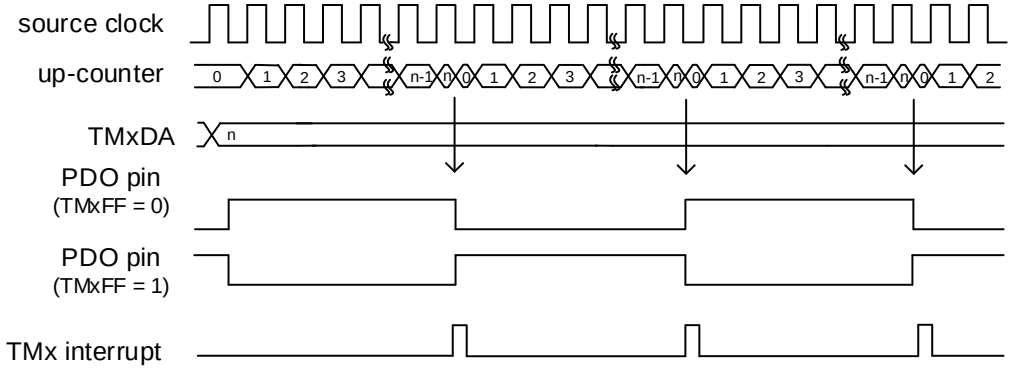


Figure 6-22 PDO Mode Waveform

6.8.6 PWM

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock with prescaler. The Duty of PWMx control by TMxDB, and the period of PWMx control by TMxDA. The pulse at the PWMx pin is held to high level as long as TMxS=1 or timerx matches TMxDA, while the pulse is held to low level as long as timer matches TMxDB. Once TMxFF is set to 1, the signal of PWMx is inverted. A TMx interrupt is generated and defined by TMxIS. On the other hand, the TMxDA and TMxDB can be written anytime, but the data of TMxDA and TMxDB are latched only at writing TMxDA[0]. Therefore, the new duty and new period of PWM appear at the PMW pin at the last period–match.

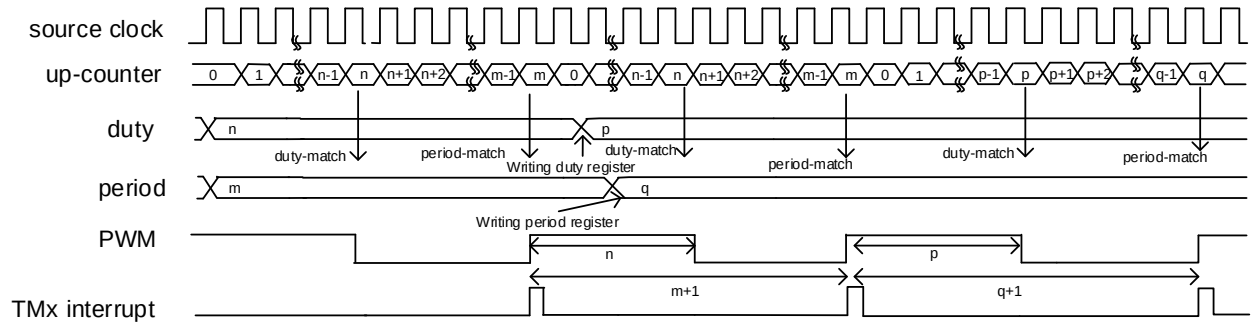


Figure 6-23 PWM Mode Waveform

6.8.7 Buzzer Mode

TMx pin output the clock after dividing the frequency

6.9 PWM for Motor Control

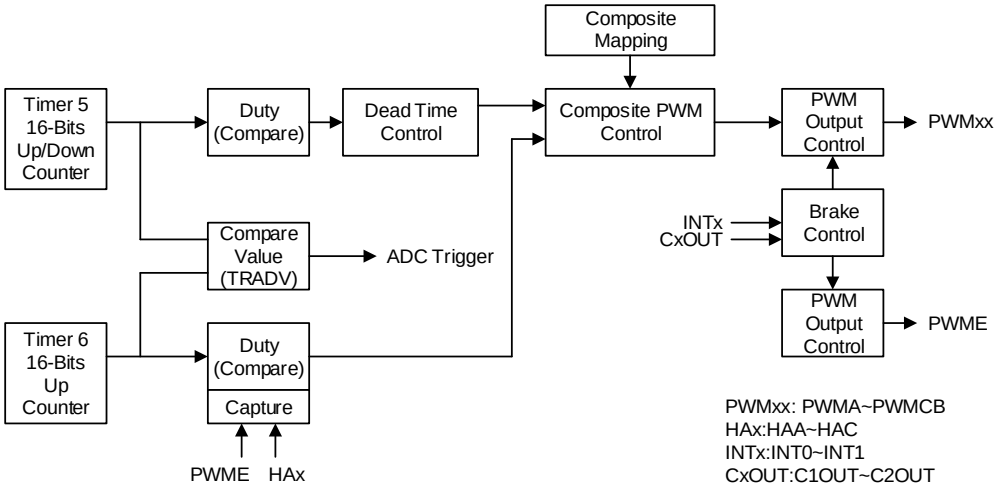


Figure 6-24 PWM for Motor Control Block Diagram

Timer 5 and Timer 6 are two 16-bit timers to be used as PWM control for motor. The features of Timer 5 and Timer 6 are described below. The block diagram of Timer 5 and Timer 6 are also shown in Figure 6-24. No matter what mode Timer 5 and Timer 6 operate in, TxRF flag must be equal to a high level first.

Features of Timer 5:

1. Three channels with 6 outputs: PWMA/PWMAB ~ PWMC/PWMCB
2. 16-bit resolution with selectable pre-scalar
3. Dead-time control for each channel
4. Operation mode: Normal PWM output mode/Phase correct PWM output mode
5. Support single pulse mode
6. Support brake PWM control
7. Channel A~C : PWM output mode (supports composite PWM)
8. Trigger ADC function

Features of Timer 6:

1. One channel with one output：PWME
2. 16-bit resolution with selectable pre-scalar
3. Only Normal PWM output mode
4. Synchronized to Timer 5
5. Support single pulse mode
6. Support Brake PWM control
7. Channel E : PWM output mode/Capture mode
8. Trigger ADC function

6.9.1 Normal PWM Output Mode

Timer 5 / Timer 6 is up-counter in this mode. In single pulse mode, Timer5/Timer6 starts to count from zero once T5RF/T6RF=1. When counting value of Timer5/Timer6 is equal to T5PD/T6PD, the counting value of Timer5/Timer6 would be reset to zero and Timer5/Timer6 would stop counting. However, if the timer operates in continuous mode, the timer would count from zero to T5PD/T6PD consecutively and not stop as T5RF/T6RF=0. Therefore, the corresponding PWM waveforms are as shown in Figure 6-25, Figure 6-26, Figure 6-27 and Figure 6-28.

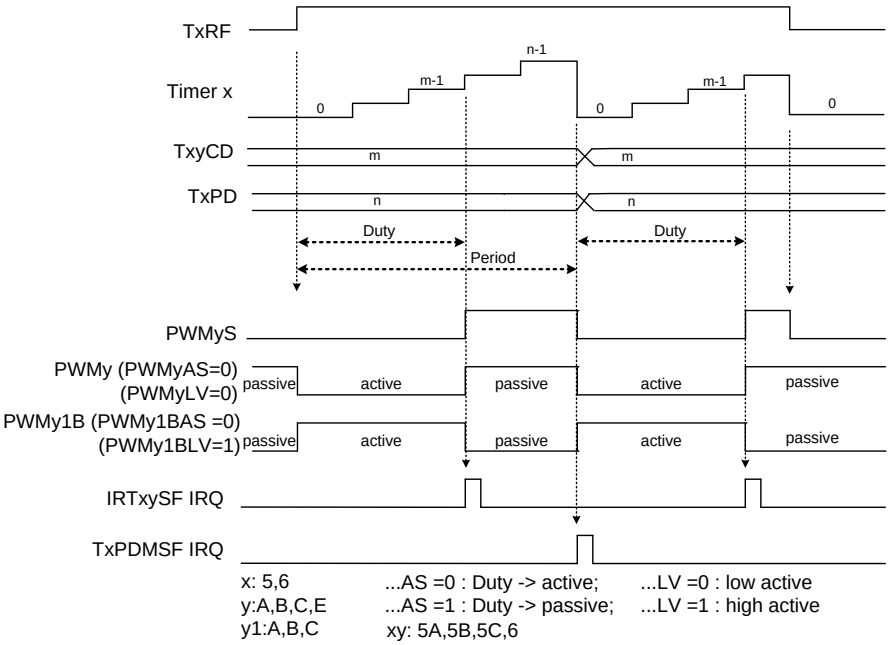


Figure 6-25 Normal PWM Waveform(1)

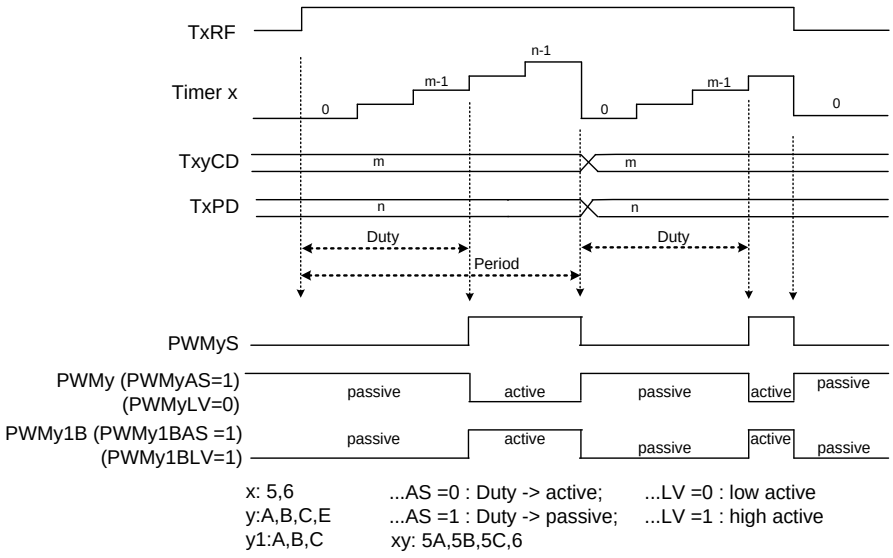


Figure 6-26 Normal PWM Waveform (2)

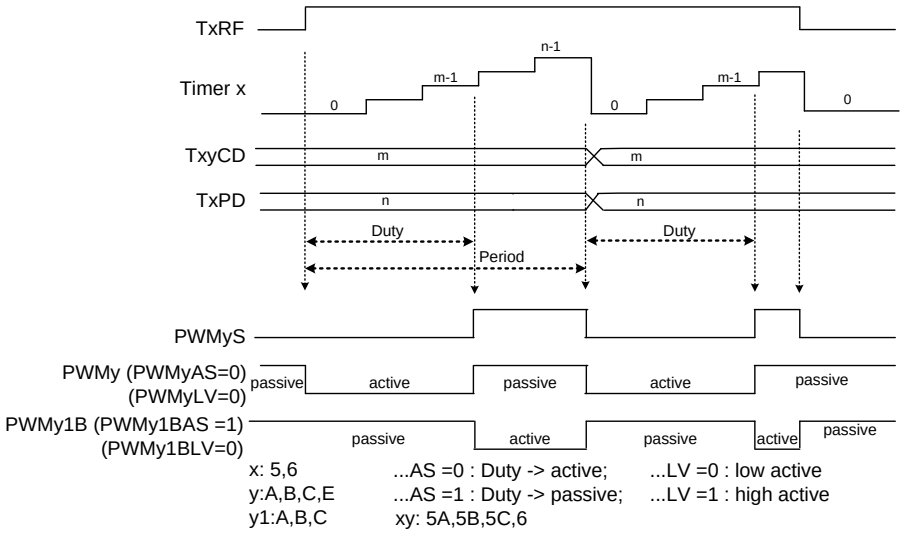


Figure 6-27 normal PWM waveform(3)

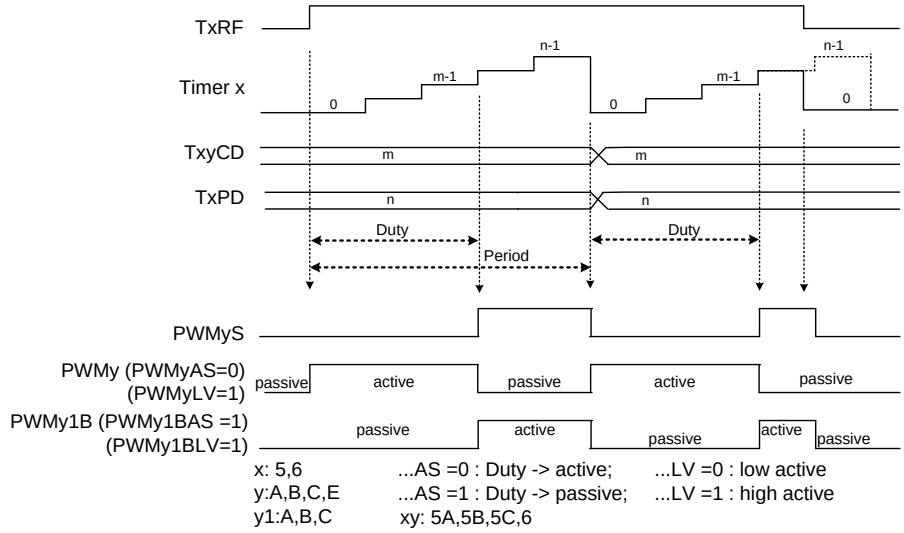


Figure 6-28 Normal PWM Waveform(4)

The deadtime control is only for Timer 5. There are three pairs of PWM (PWMA/PWMAB, PWMB/PWMBB, PWMC/PWMCB) which can be used for deadtime control as T5EPWMx/ T5EPWMxB=1. The time of deadtime is the value of T5DE register multiplied by 1/t5_tmr_clk (The clock of deadtime timer is not processed by prescaler). If the deadtime is enabled for the conditions as shown in Figure 6-25, Figure 6-26, Figure 6-27 and Figure 6-28, the passive state will be held additionally for the deadtime as illustrated in Figure 6-29 and Figure 6-30.

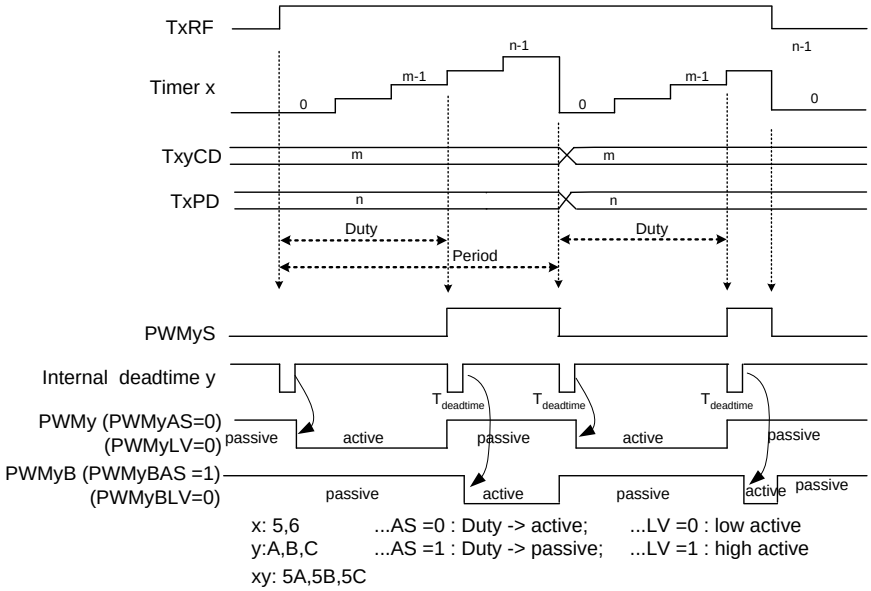


Figure 6-29 Passive State 1 for Deadtime

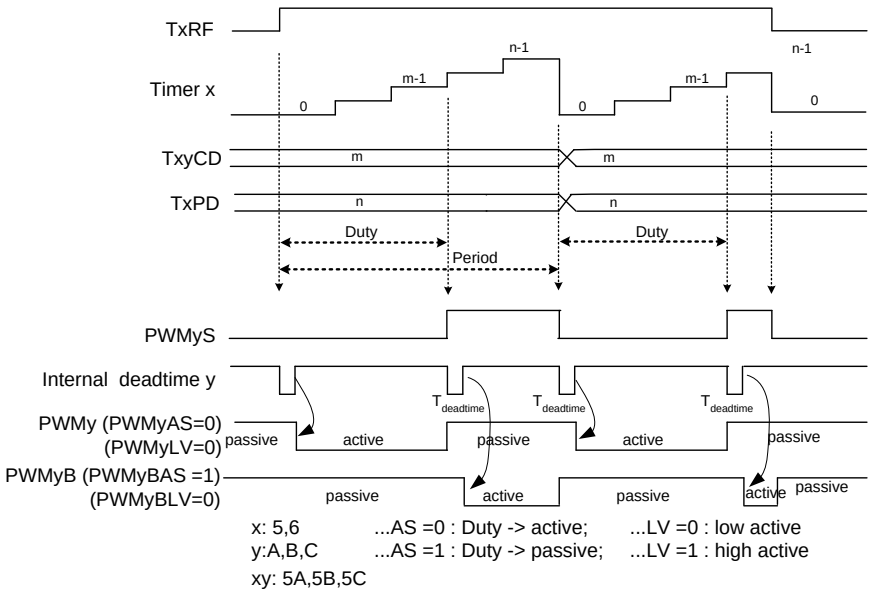


Figure 6-30 Passive State 2 for Deadtime

6.9.2 Phase Correct PWM Output Mode

Only Timer 5 can be used at phase correct PWM mode. Once TxRF=1, Timer5 starts to count from zero for single pulse mode. When counting value of Timer 5 is equal to T5PD, Timer 5 would continuous to down-count from the value of T5PD until the counting value of Timer 5=zero. However, if Timer 5 is in continuous mode, the timer would count from zero to T5PD and then count from T5PD to zero consecutively until T5RF=0.

The corresponding PWM waveforms are shown in Figure 6-31, Figure 6-32, Figure 6-33 and Figure 6-34. And the corresponding PWM waveforms with deadtime are shown in Figure 6-35 and Figure 6-36. However, if the deadtime is enabled, the passive state will be held additionally for the time of deadtime.

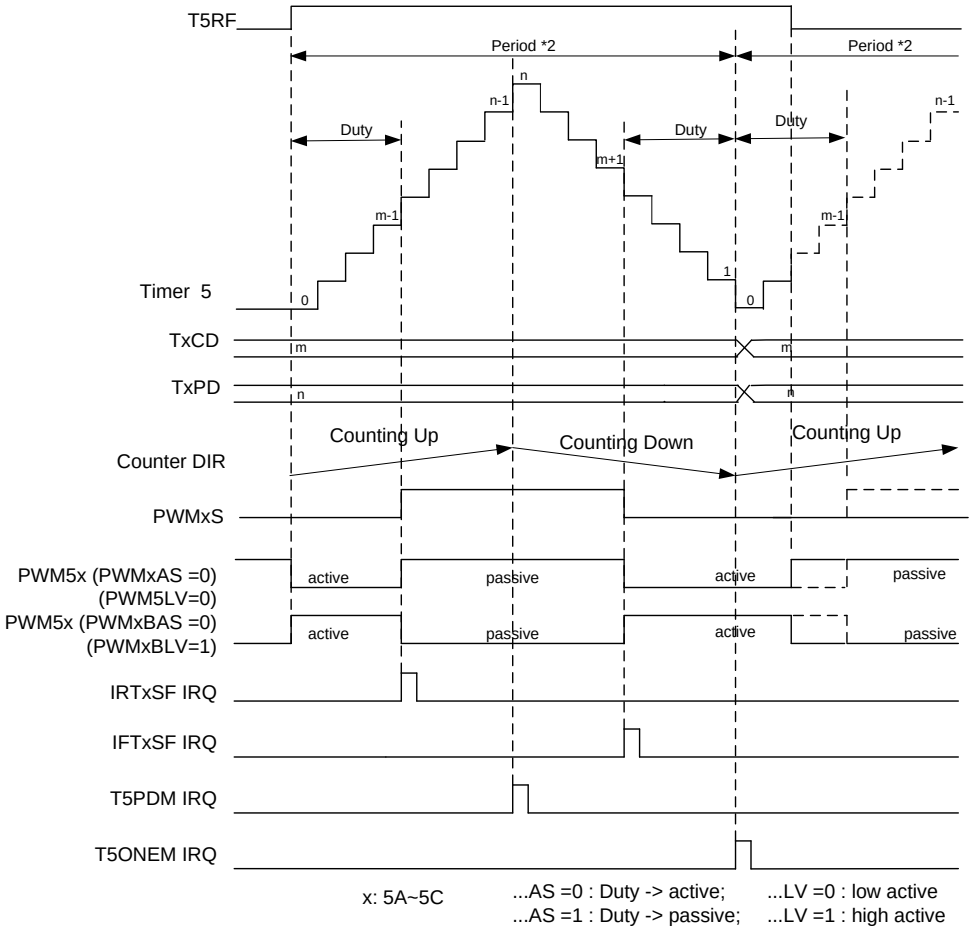


Figure 6-31 Corresponding PWM Waveforms

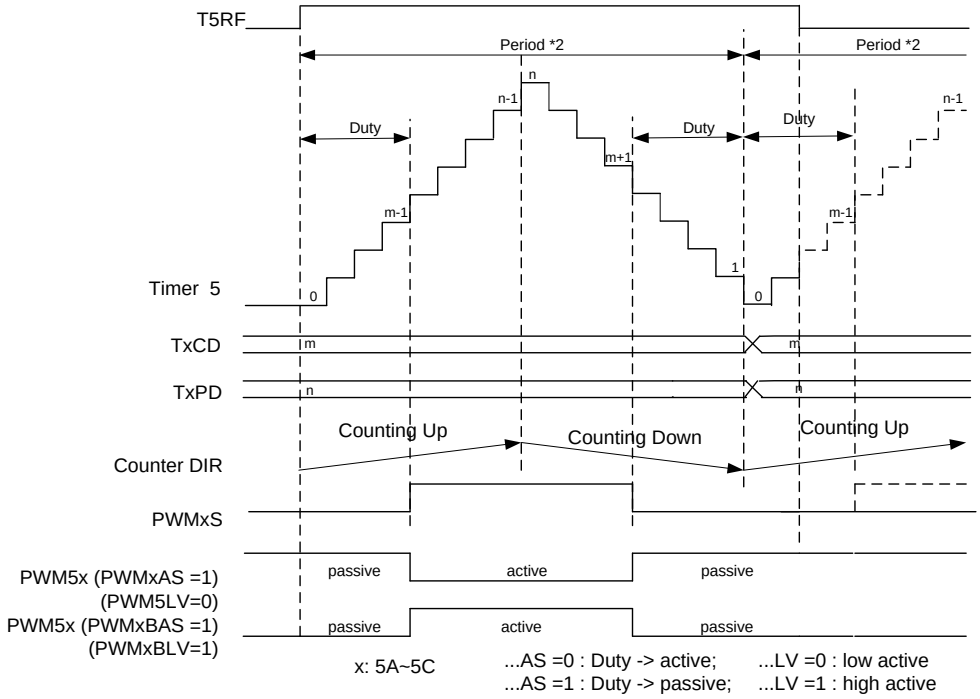


Figure 6-32 Corresponding PWM Waveforms

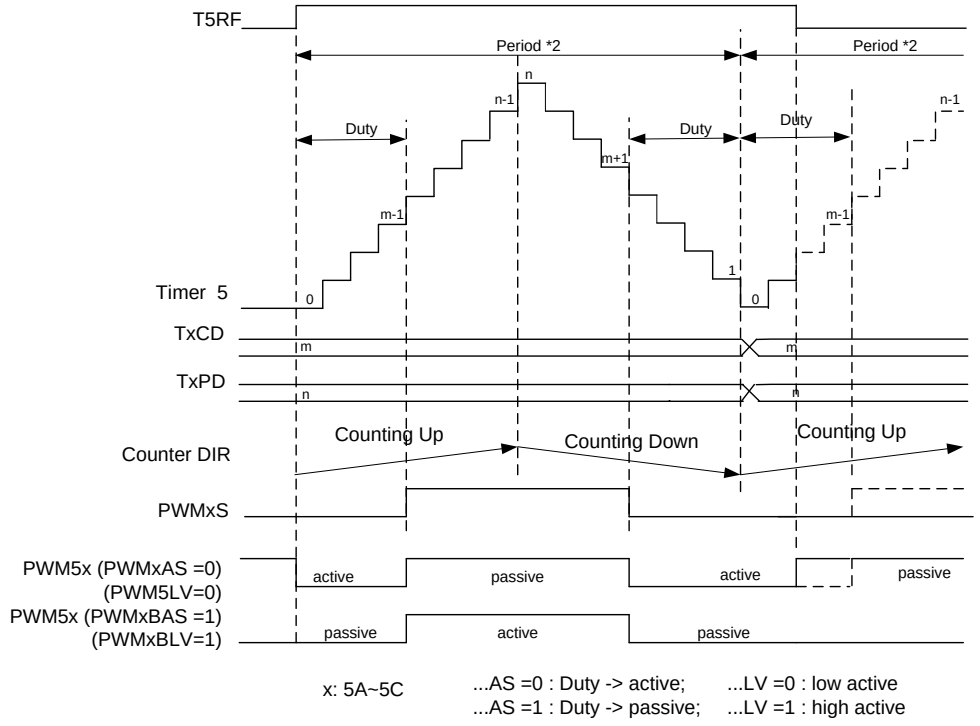


Figure 6-33 Corresponding PWM Waveforms

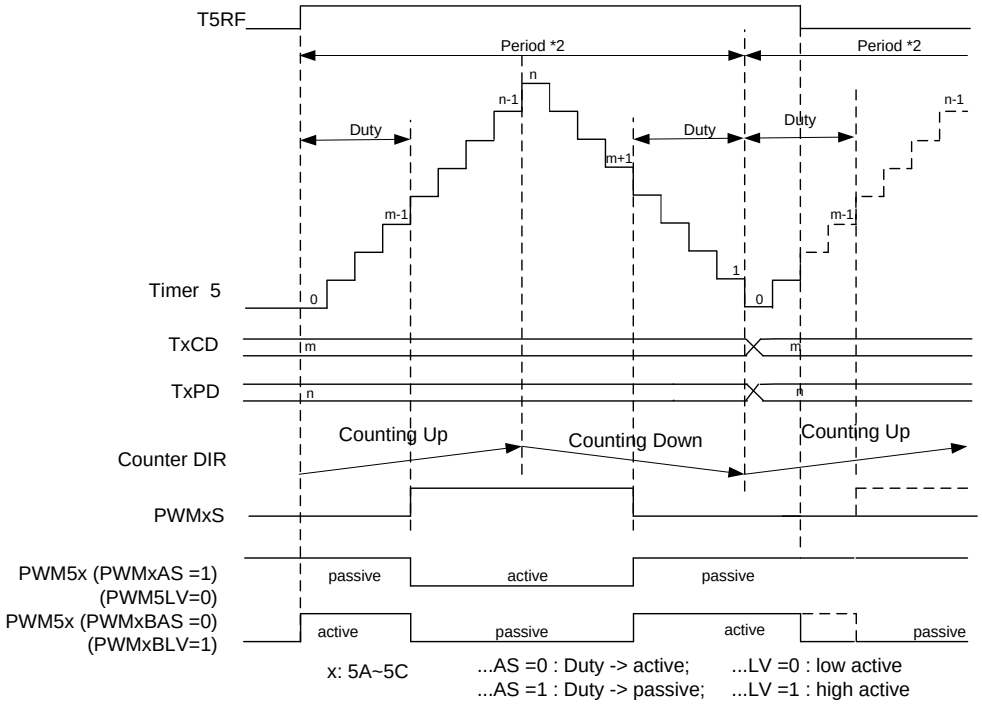


Figure 6-34 Corresponding PWM Waveform

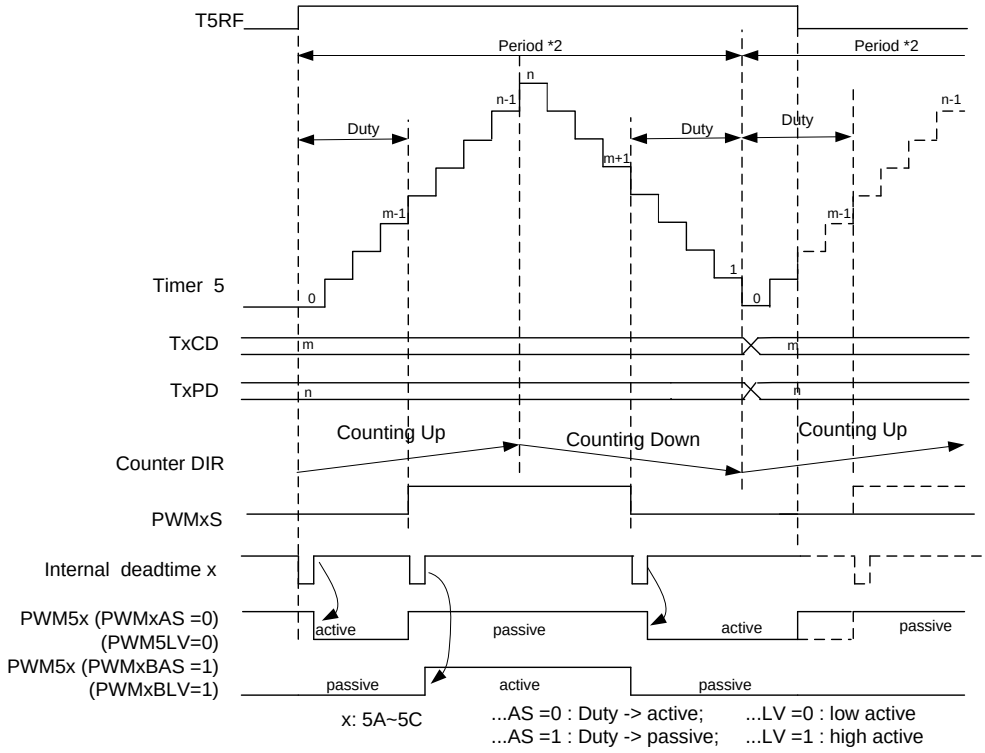


Figure 6-35 Corresponding PWM Waveform with Deadtime

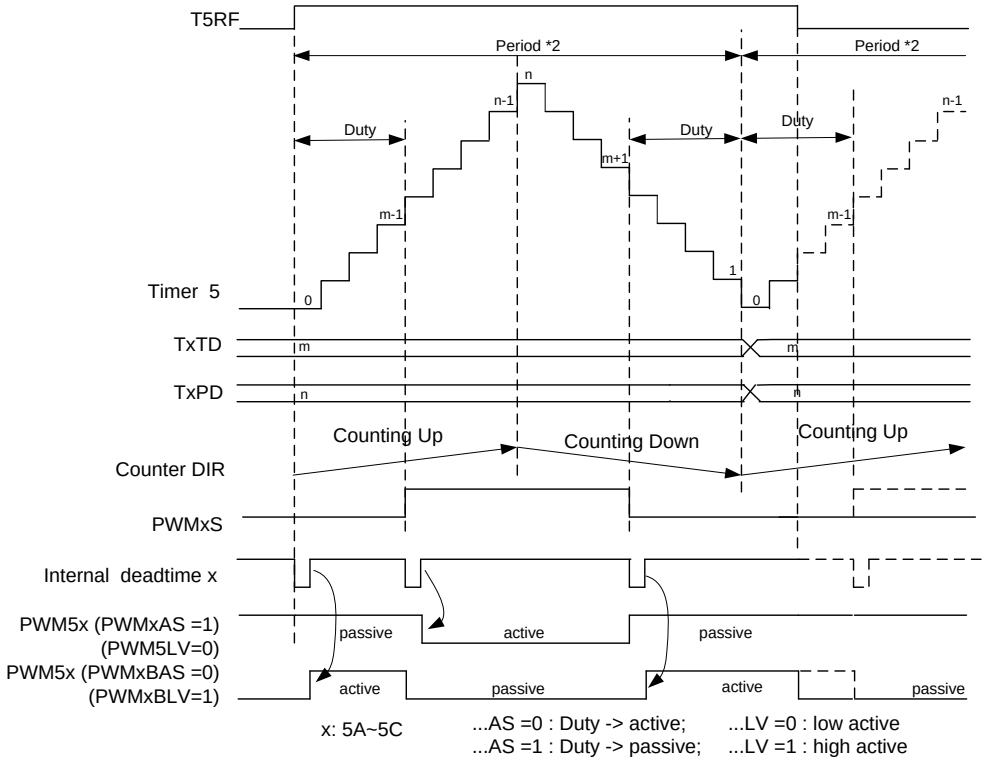


Figure 6-36 Corresponding PWM Waveform with Deadtime

6.9.3 Timer 6 is Synchronized to Timer 5

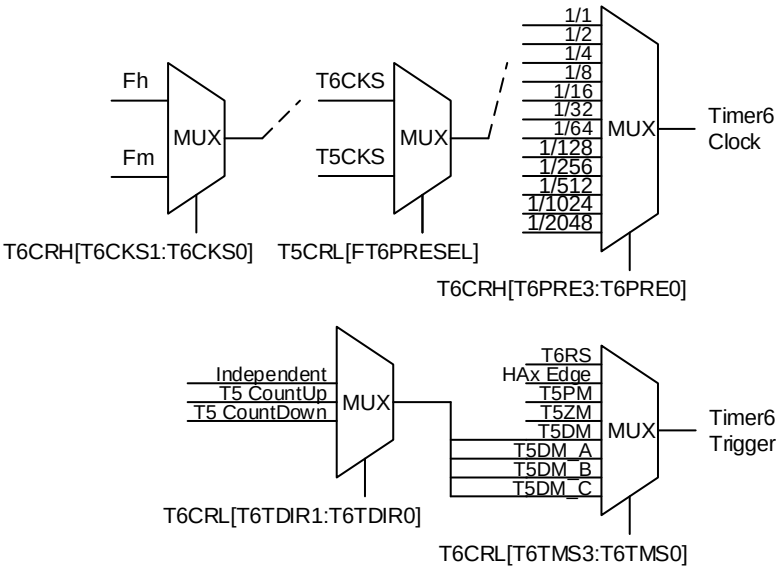
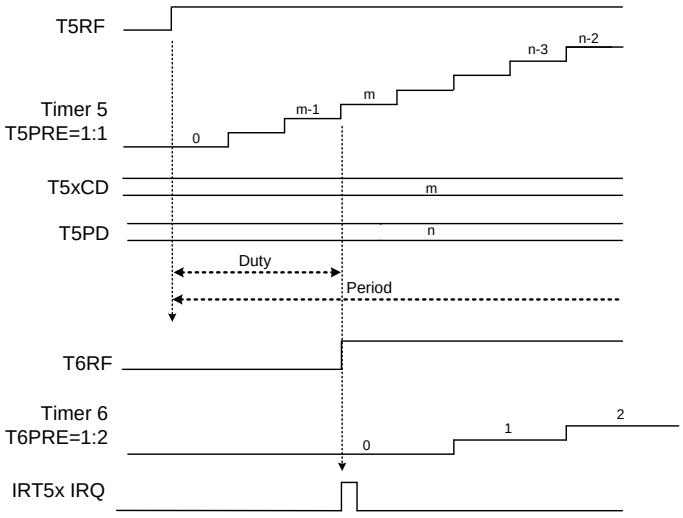
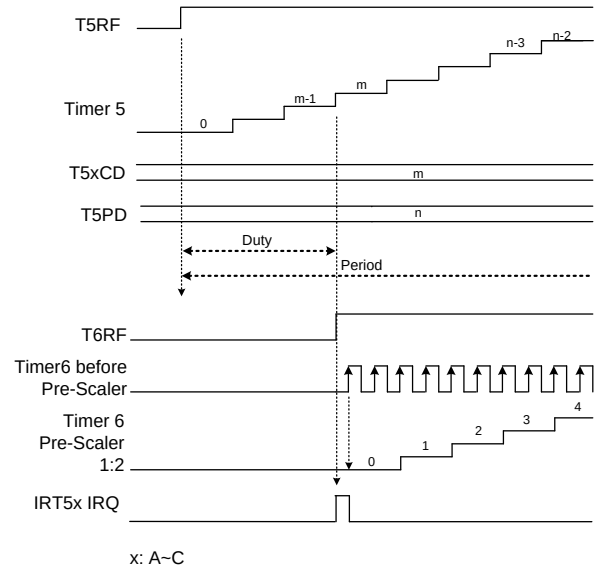


Figure 6-37 Function Block of Timer 6 Synchronized to Timer 5

Timerx (x=5, 6) clock is determined by TxCKS and TxPRE. But for good synchronization, Timer 6 clock source can be determined by FT6PRESEL. On the other hand, one of T6RF setting methods is determined by T6TMS. Therefore, if T6TMS and T6DIR are set to be determined to duty compare event of up-counting Timer 5, the corresponding waveform are as shown in Figure 6-38.



(a) FT6PRESEL=1



(b) FT6PRESEL=0

Figure 6-38 Waveform for different value of FT6PRESEL

6.9.4 Composite PWM Mode

PWMxx(xx=A,AB,B,BB,C,CB) can be used in composite PWM mode dependent on CPE, T5EPWMxx, and T6EPWMxx. If CPE=1, the state of PWMxx output is determined by CPWMxx. The timing for updating the value of CPWMxx is decided by CPMTE, TMSM, and TSYN as shown in Figure 6-39.

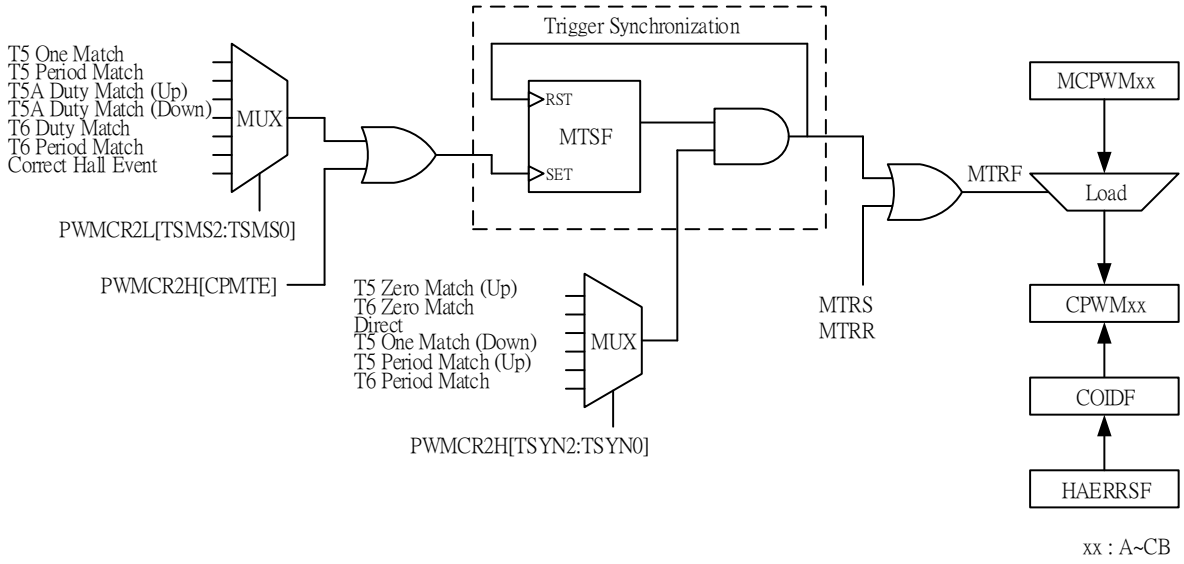


Figure 6-39 Function Block of Composite Mapping

However, the CPWMxx is valid as CPE=1. Therefore, the corresponding waveform of PWMxx is the result of T5_PWMxx, T6_PWME, CPWMxx, and BRKS. The corresponding waveform of PWME is the result of T6_PWME and BRKS. The functional block of composite mode are shown below. Here, T5_PWMxx is the signal determined by PWMxxAS from PWMxxS and T6_PWME is the signal determined by PWMEAS from PWMES.

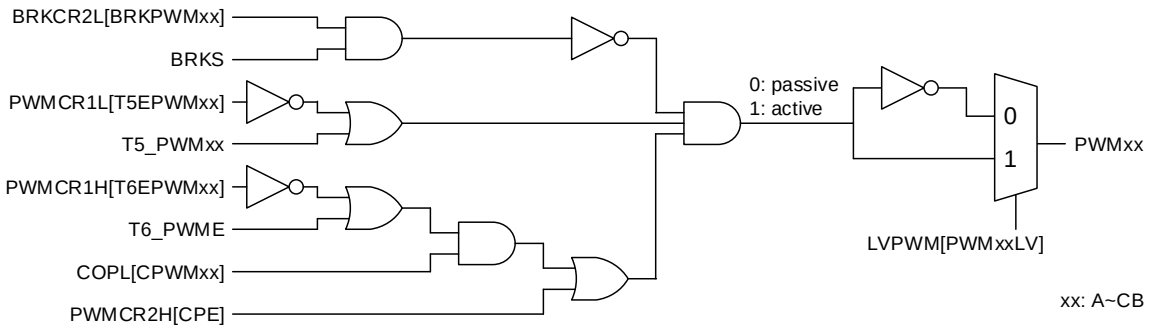


Figure 6-40 Composite PWM Mode for PWMA, PWMAB, PWMB, PWMBB, PWMC,PWMCB

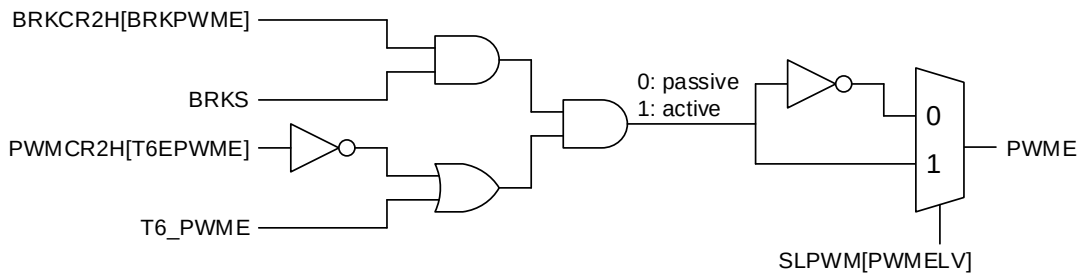


Figure 6-41 Composite PWM Mode for PWME

6.9.5 Hall Function

The hall function includes noise rejection, sampling trigger source and pattern compare.

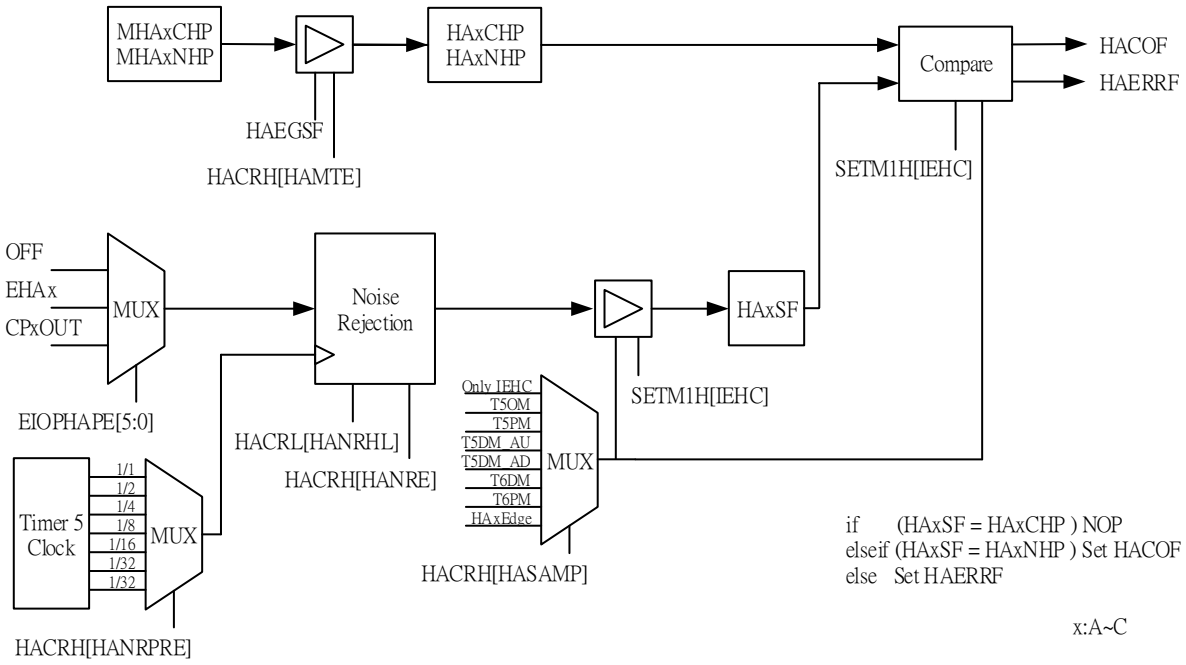


Figure 6-42 Hall Function Block Diagram

6.9.6 Brake Function

Brake signal can be as comparator1 output, comparator2 output, and EINT0~1, which is determined by BRKCR1. And the active level of Brake signal can also be determined. BRKF is the flag which corresponds to the actual event from HW. When BRKFAC=0, the timing of BRKS rising is equal to the timing of BRKF rising and the timing of BRKS falling is determined by BRKM. The corresponding waveform is as below. If BRKS=1, the corresponding PWMxx is at passive level.

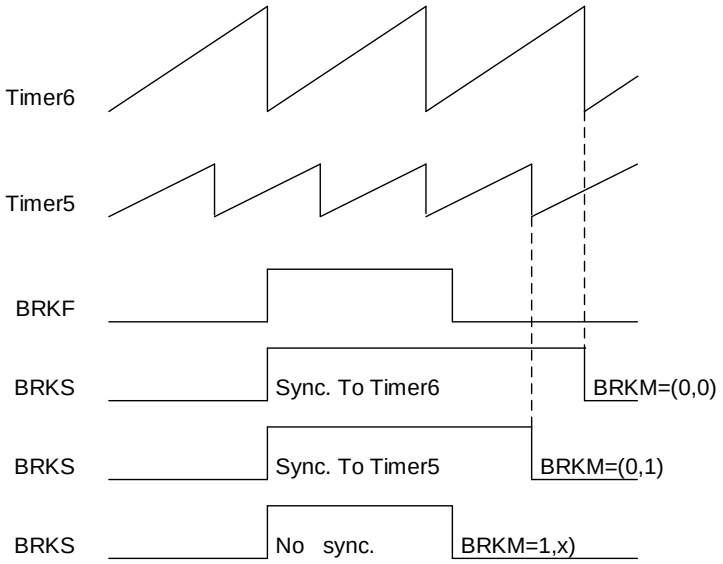


Figure 6-43 BRKS waveform

6.9.7 Trigger ADC Mode

The configuration of Tigger ADC mode is determined by TRADCR register. There are two registers (TRADV1 and TRADV2) that can be used to define when ADC would be triggered to work as Timer 5 or Timer 6 starts to count.

6.9.8 Capture Mode

The configuration of Timer 6 captured mode is determined by T6OPMS register. At first, the T6RF must be set. Once the captured event happens, the corresponding duty-matching flag (IRTxSF or IFTxSF, x:6) will be set automatically. Then, Timer 6 continuous to count until period-matching. After period-matching, Timer 6 will be reset to zero and continuous to count. On the other hand, Timer 6 can also be cleared to zero by T6CLR and stop counting by T6RF.

6.10 Comparator

R_BANK	Addres	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x10	WUCR2	CMP2WK	CMP1WK						
			R/W	R/W						
Bank 0	0x15	SFR1	CMP2SF	CMP1SF						
			R/W	R/W						
Bank 0	0x1B	IMR1	CMP2IE	CMP1IE						
			R/W	R/W						
Bank 2	0x1E	CMP1CR	C1PRS1	C1PRS0	C1NRS1	C1NRS0		CMP1EN	CMP1OE	CP1OUT
			R/W	R/W	R/W	R/W		R/W	R/W	R/W
Bank 2	0x1F	CMP2CR	C2PRS1	C2PRS0	C2NRS1	C2NRS0	HYSEN2	CMP2EN	CMP2OE	CP2OUT
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x22	CMPESCR							CMP2ES	CMP1ES
									R/W	R/W
Bank 2	0x23	CMP12NCR	CO2NRE		CO2NR1	CO2NR0	CO1NRE		CO1NR1	CO1NR0
			R/W		R/W	R/W	R/W		R/W	R/W
Bank 2	0x25	CMPTCR1	CMPTEN	VOSFS2	VOSFS1	VOSFS0			TRIMDU2	TRIMDU1
			R/W	R/W	R/W	R/W			R/W	R/W
Bank 2	0x26	CMPTCR2			TRIMOS				TRIMIS2	TRIMIS1
					R/W				R/W	R/W
Bank 2	0x27	TCMP1H	TCMP1 HS			TCMP1 H4	TCMP1 H3	TCMP1 H2	TCMP1 H1	TCMP1 H0
			R/W			R/W	R/W	R/W	R/W	R/W
Bank 2	0x28	TCMP1L	TCMP1 LS			TCMP1 L4	TCMP1 L3	TCMP1 L2	TCMP1 L1	TCMP1 L0
			R/W			R/W	R/W	R/W	R/W	R/W
Bank 2	0x2B	THCMP2H	THCMP2 HS		THCMP2 H5	TCMP2 H4	THCMP2 H3	THCMP2 H2	THCMP2 H1	THCMP2 H0
			R/W		R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x2C	TLCMP2H	TLCMP2 HS		TLCMP2 H5	TLCMP2 H4	TLCMP2 H3	TLCMP2 H2	TLCMP2 H1	TLCMP2 H0
			R/W		R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x2D	THCMP2L	THCMP2 LS		THCMP2 L5	THCMP2 L4	THCMP2 L3	THCMP2 L2	THCMP2 L1	THCMP2 L0
			R/W		R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x2E	TLCMP2L	TLCMP2 LS		TLCMP2 L5	TLCMP2 L4	TLCMP2 L3	TLCMP2 L2	TLCMP2 L1	TLCMP2 L0
			R/W		R/W	R/W	R/W	R/W	R/W	R/W

Overview

The MCU has two comparators comprising of two analog inputs and one output. Comparator 1 uses the trim function to calibrate the offset. Comparator 2 uses trim function to setting hysteresis range. The comparator circuit diagram is depicted in the following figure.

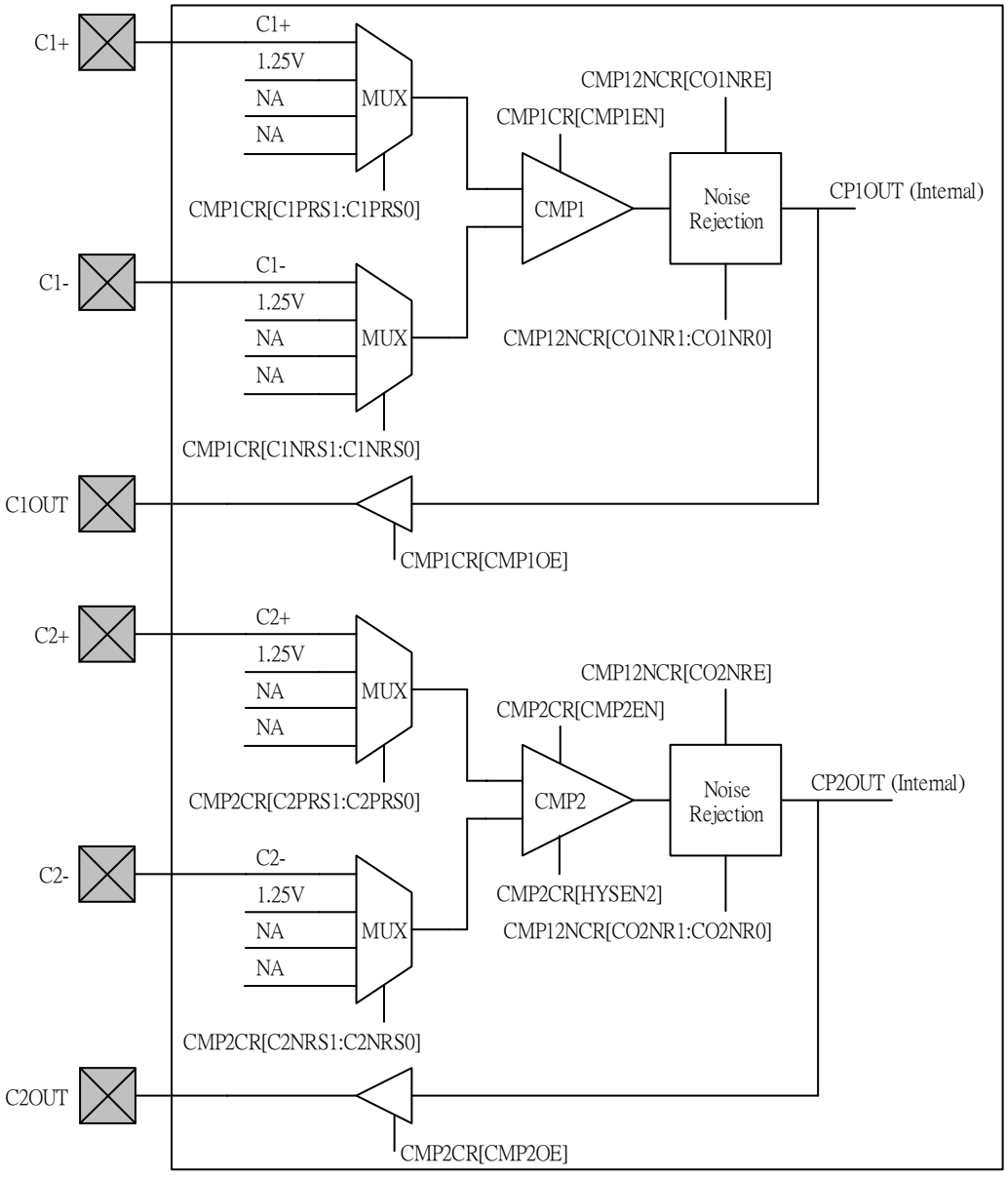


Figure 6-44 Comparator Circuit Diagram and Operating Mode

Comparator Interrupt

- CMPxIE must be enabled for the “ENI” instruction to take effect
- Interrupt is triggered whenever a change occurs on the comparator output pin
- The actual change on the pin can be determined by reading the Bit CPxOUT
- CMPXIF the comparator interrupt flag, can only be cleared by software

Wake-up from SLEEP Mode

- The comparator and the interrupt remains active in SLEEP mode when CMPxIE=1 and CMPxWK=1.
- If a comparator output changes state, the interrupt will wake up the device from SLEEP mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during SLEEP mode, turn off comparator before entering into sleep mode.

6.11 Enhance Protect

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 2	0x47	LOCKPR	LOCKPR7	LOCKPR6	LOCKPR5	LOCKPR4	LOCKPR3	LOCKPR2	LOCKPR1	LOCKPR0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x48	LOCKCR	LOCKEN							
			R/W							

The EM88F794N supports a protect function to prevent source code from overwriting or reading. When the instruction TBRDA/TBRD/TBWR is executed at a protect area, it can write or read all flash ROM. When the instruction TBRDA/TBRD/TBWR is executed at a normal area, it can write or read the ROM at normal area only.

6.11.1 Enhance Protect Programming

The Enhance Protect operates as follows:

1. Set LOCKEN.
2. Write 0xC5 into FLKR.
3. Write LOCKPR to set lock range.

   *Instruction “TBRDA/TBRD/TBWR” cannot be writing at the end of lock area

   *The base unit of LOCKPR is 128 words.

   *When use the TBWR instruction, the code option “TBWEN” must be enabled.

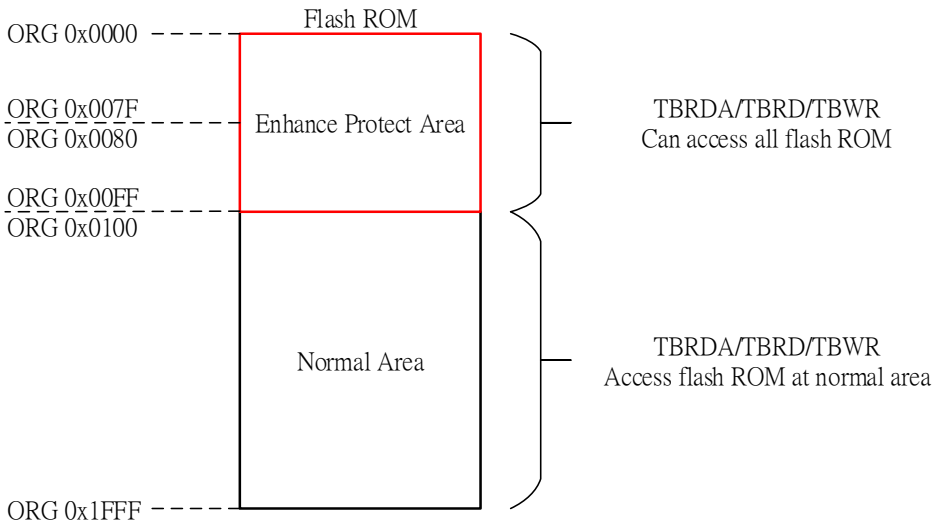


Figure 6-45 Enhance Protect

6.12 In Application Programing

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0x4D	TBWCR								IAPEN
										R/W
Bank 1	0x4E	TBWAL	TBWA[7]	TBWA[6]	TBWA[5]	TBWA[4]	TBWA[3]	TBWA[2]	TBWA[1]	TBWA[0]
			R/W	R/W	R/W	R	R	R	R	R
Bank 1	0x4F	TBWAH					TBWA[11]	TBWA[10]	TBWA[9]	TBWA[8]
							R/W	R/W	R/W	R/W

The EM88F794N supports In Application Programming. It can copy data from RAM to ROM and overwrite 32-word flash ROM.

6.12.1 In Application Programming

The IAP operates as follows:

1. Set Code Option Word 2[TBWEN]
2. Move data what you want to save in flash into RAM.
3. Set TBWAH/ TBWAL register with programming address.
4. Enable IAP mode by set TBWCR[IAPEN]
5. Write 0xB4 to FLKR register.
6. Execute TBWR instruction.
7. Then data will be written to ROM.

   *The bas unit of IAP is 32 words, the programming address bit 0~4 is read-only.

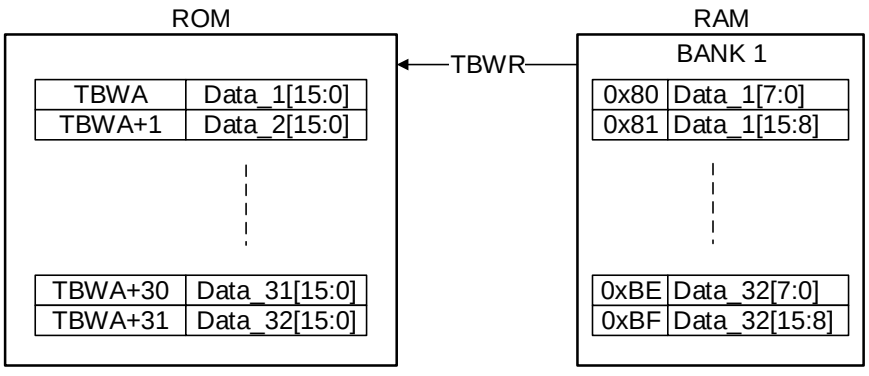


Figure 6-46 In Application Programming

6.13 Low Voltage Detector

During the power source unstable situation, such as external power noise interference or EMS test condition, it will cause the power to vibrate fiercely. At that time, VDD is unsettled, it may be below the operating voltage.

EM88F794N has BOR and LVD module detect the voltage, when user enables the LVD by setting LVDEN or enable BOR by setting BOREN or enable both, the current consumption will increase about 100μA.

6.13.1 LVD and BOR

The following steps are needed to setup the LVD and BOR function:

1. Set Code Option Word 2[BOREN] to enable the BOR function.
2. Use Code Option Word 1[BORS1:BORS0] to decide the LVD and BOR voltage detection level.
3. Set the Bank1 R49 LVDCR[LVDEN] to enable the LVD function.
4. Waiting for low voltage to occur leads to LVD interrupt or BOR reset.

During sleep mode, the LVD module continues to operate. If the device voltage drop slowly and crosses the detect point. The LVDSF bit will be set and the device won't wake-up from Sleep mode. Until the others wake-up source to wake-up EM88F794N, the LVD interrupt flag still be set as the prior status.

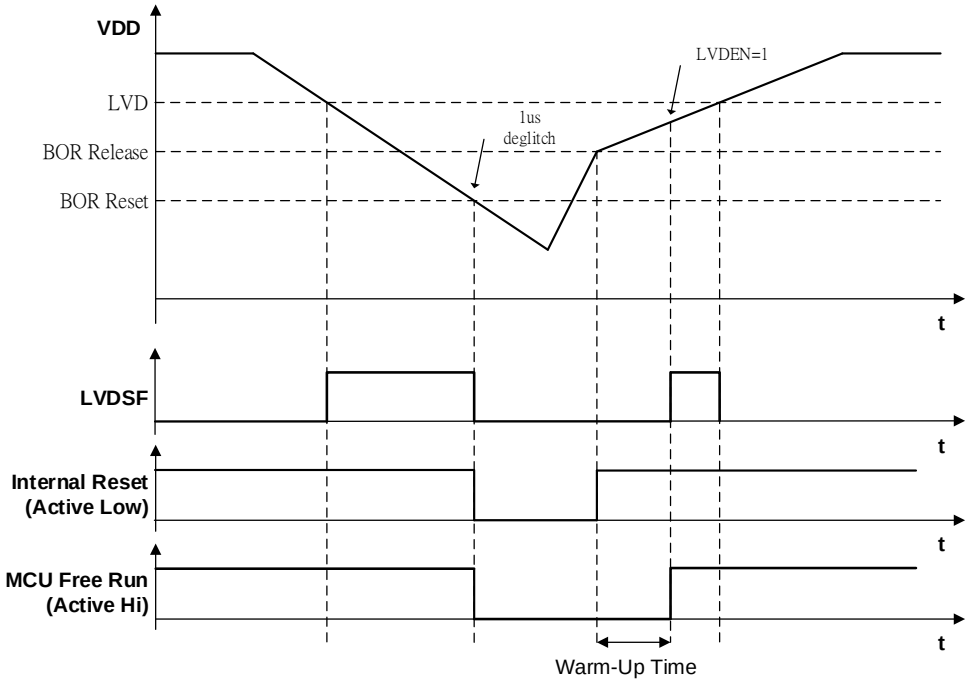


Figure 6-47 LVD and BOR Waveform

6.13.2 Time Sharing Mode

EM88F794N supports time-sharing mode, To enable the time-sharing mode and set the time interval by Code Option Word 2[BORT2:BORT0], user can use time-sharing mode to decrease the average current consumption of LVD and BOR functions, especially in IDLE and SLEEP mode.

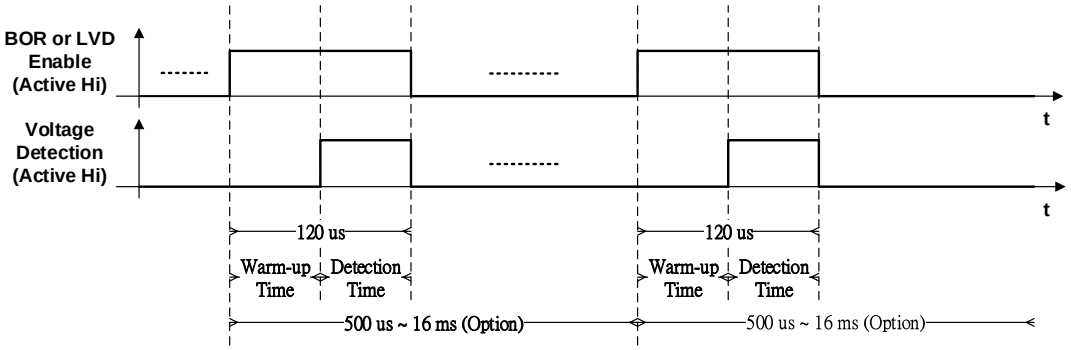


Figure 6-48 LVD and BOR Time Sharing Mode Timing

6.14 Oscillator

6.14.1 Oscillator Modes

The EM88F794N can be operated in one oscillator mode, such as Internal RC oscillator mode (IRC). User needs to set main-oscillator modes by selecting the OSC0, and set the sub-oscillator modes by selecting the FSS in the CODE Option register to complete the overall oscillator mode setting.

Table 10 Main-oscillator modes defined by OSC[1:0]

Main-oscillator mode	OSC1	OSC0
IRC (Internal RC oscillator mode) (default) RCOUT (P71) acts as I/O pin	0	0
IRC (Internal RC oscillator mode) RCOUT (P71) acts as clock output pin	0	1

Table 11 Sub-oscillator modes defined by FSS

Sub-oscillator Mode	FSS
Fs is 16kHz (default)	0
Fs is 128kHz	1

Note: WDT frequency is always 16kHz whatever the FSS bits are set.

Table 13 Summary of Maximum Operating Speeds

Conditions	VDD	F_{XT} max. (MHz)
Two cycles with two clocks	3.0	20
	4.2	24
	4.2	28
	4.5	32

6.14.2 Internal RC Oscillator Mode

EM88F794N offers a versatile internal RC mode with default frequency value of 20 MHz. Internal RC oscillator mode has other frequencies (20 MHz, 24 MHz, 28 MHz, 32 MHz) that can be set by Code Option bits RCM1 ~ RCM0.

Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+125°C)	Voltage	Process	Total
20 MHz	±3.5% (3V~5.5V)		±1.5%	±5%
24 MHz	±3.5% (3V~5.5V)		±1.5%	±5%
28 MHz	±3.5% (3V~5.5V)		±1.5%	±5%
32 MHz	±2.8% (4.5V~5.5V)		±0.2%	±3%

Note: Theoretical values are for reference only. Actual values may vary depending on actual process.

6.15 Power–on Considerations

No microcontroller is guaranteed to start operating properly before the power supply stabilizes. The EM88F794N has an on-chip Power–on Voltage Detector (POVD) with a detecting level of 2.1V. It will work well if VDD is rising quick enough (50ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.16 External Power–on Reset Circuit

The circuit has shown in Figure 6-49 implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for VDD to reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

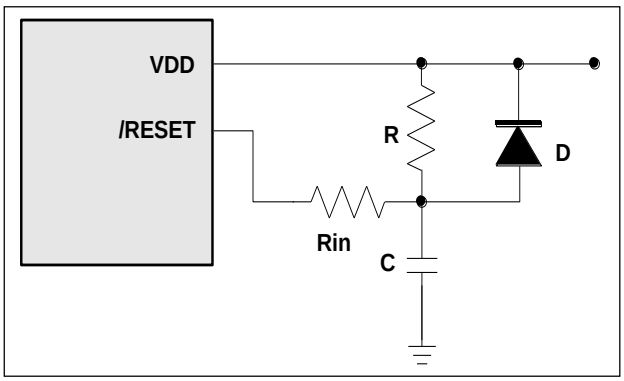


Figure 6-49 External Power-Up Reset Circuit

6.17 Residue-Voltage Protection

When battery is replaced, device power (VDD) is taken off but residue-voltage remains. The residue-voltage may trips below VDD minimum, but not to zero. This condition may cause a poor power on reset. Figure 6-50 and Figure 6-51 show how to build a residue-voltage protection circuit.

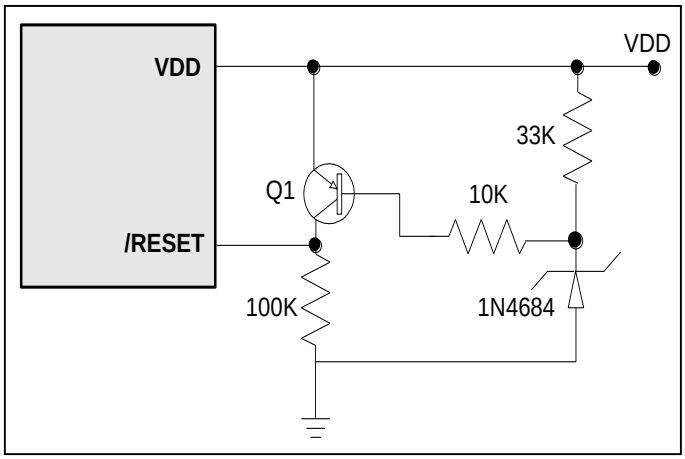


Figure 6-50 Circuit 1 for the Residue Voltage Protection

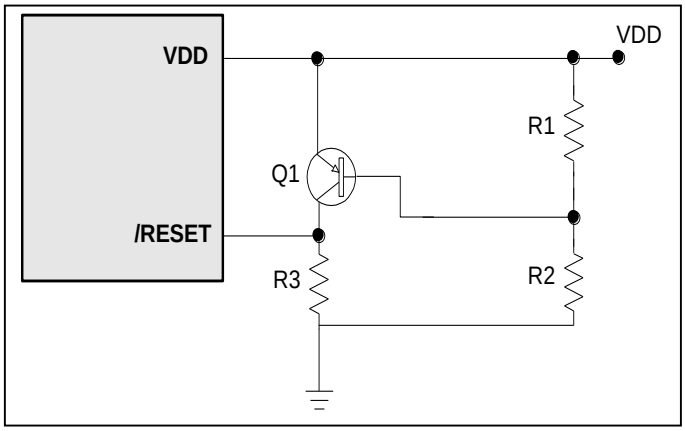


Figure 6-51 Circuit 2 for the Residue Voltage Protection

6.18 Code Option

6.18.1 Code Option Register (Word 0)

Word 0								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
Mnemonic	-	-	IRCWUT	-	-	HLFS	HLP	-
1	High		16 clks	High	High	Green	Low PWR	High
0	Low		8 clks	Low	Low	Normal	High PWR	Low
Default	0		1	0	0	0	0	0
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	RESETEN	ENWDT	-	-	-	-	-
1	High	/RST	Enable	High	High	High	High	High
0	Low	P66	Disable	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0

Bits 15~14: Not used, set to "0" all the time.

Bit 13 (IRCWUT): IRC Warm-Up Time

1: 16 clocks (default)

0: 8 clocks

CPU mode switch	IRC Frequency	Waiting Time before CPU Starts to Work
Sleep → Normal **Idle → Normal** **Green → Normal**	**20M, 24M, 28M, 32M**	**WSTO + 8/16 clocks (sub frequency)**
Sleep → Green **Idle → Green**	**128kHz**	**WSTO + 8 clocks (sub frequency)**

Bits 12~11: Not used, set to “0” all the time

Bit 10 (HLFS): Reset to Normal or Green Mode Select Bit

1: CPU is selected as Green mode when a reset occurs.

0: CPU is selected as Normal mode when a reset occurs (default)

Bit 9 (HLP): Power Consumption Select

1: Low power consumption, apply to working frequency at 4 MHz or below 4 MHz

0: High power consumption, apply to working frequency above 4 MHz

Bits 8~7: Not used, set to “0” all the time

Bit 6 (RESETEN): P66/RESET pin select bit

1: Enable, P66 as RESET pin.

0: Disable, P66 as I/O pin (default)

Bit 5 (ENWDT): WDT enable bit

1: Enable

0: Disable (default)

Bits 4~0: Not used, set to "0" all the time.

6.18.2 Code Option Register (Word 1)

Word 1								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
Mnemonic	-	-	FSS	-	BORS1	BORS0	CLK2	CLK1
1	High	High	128K	High	High	High	High	High
0	Low	Low	16K	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	CLK0	-	RCM1	RCM0	-	OSC1	OSC0	RCOUT
1	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0

Bits 15~14: Not used, set to "0" all the time.

Bit 13 (FSS): Sub-oscillator mode select bit

1: Fs is 128kHz

0: Fs is 16kHz

Bit 12: Not used, set to "0" all the time.

Bits 11~10 (BORS1~BORS0): Voltage Level select bit

LVDEN	BORS1, BORS0	LVD Voltage Interrupt Level	LVDSF
1	00	3.0V	1
1	01	4.1V	1
1	10	4.7V	1
0	xx	NA	0
BOREN	**BORS1, BORS0**	**BOR Voltage Reset Level**	
1	00	2.8V	
1	01	3.9V	
1	10	4.6V	
0	xx	NA	

Bits 9~7 (CLK2~CLK0): Instruction period option bits

CLK2	CLK1	CLK0	Scale of Main Clock
0	0	0	/2
0	0	1	/4
0	1	0	/8
0	1	1	/16
1	0	0	/32
1	0	1	/64

Bit 6: Not used, set to "0" all the time.

Bits 5~4 (RCM1~RCM0): IRC frequency select.

* Corresponding with control register Bank0 RE RCM2~RCM0

RCM1	RCM0	Frequency (MHz)
0	0	20 (default)
0	1	24
1	0	28
1	1	32

Bit 3: Not used, set to "0" all the time.

Bits 2~1 (OSC1~OSC0): Main-oscillator mode select bits.

Main-oscillator mode	OSC1	OSC0
IRC (Internal RC oscillator mode) (default) RCOUT (P71) acts as I/O pin	0	0
IRC (Internal RC oscillator mode) RCOUT (P71) acts as clock output pin	0	1

Bit 0 (RCOUT): System Clock Output Enable Bit in IRC mode

1: RCOUT pin is open drain

0: RCOUT output instruction cycle time (default)

RCOUT pin output frequency = Fm / n (CLK2~0)

6.18.3 Code Option Register (Word 2)

Word 2								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
Mnemonic	-	SHEN	-	-	BOREN	BORT2	BORT1	BORT0
1	High	Disable	High	High	High	High	High	High
0	Low	Enable	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	1	0	0	0
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	-	-	-	-	-	-	-
1	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0

Bit 15: Not used, set to "0" all the time.

Bit 14 (SHEN): System hold enable bit.

1: Disable

0: Enable

Bits 13~12: Not used, set to "0" all the time.

Bit 11 (BOREN): BOR Enable bit.

1: BOR Disable (default)

0: BOR Enable

Bits 10~8 (BORT2~ BORT0)

BORT2~0	BOR Sample Time (μs)
000	Always On (default)
001	16000
010	8000

011	4000
100	2000
101	1000
110	500

Bits 7~0: Not used, set to "0" all the time.

6.18.4 Code Option Register (Word 3)

Word 3								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
Mnemonic	-	EFTIM	-	-	ADFM	-	-	-
1	High	Enable	High	High	High	High	High	High
0	Low	Disable	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Mnemonic	-	TBWEN	ID5	ID4	ID3	ID2	ID1	ID0
1	High	Enable	Customer ID					
0	Low	Disable						
Default	0	0						

Bit 15: Not used, set to "0" all the time.

Bit 14 (EFTIM): Low Pass Filter

1: Enable (DC~40 MHz)

0: Disable (default)

Bits 13~12: Not used, set to "0" all the time.

Bit 11 (ADFM): This bit controls the format of AD data buffer (ADDH & ADDL), refer to the following table,

ADFM			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	0	ADDH					ADD11	ADD10	ADD9	ADD8
		ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	1	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		ADDL					ADD3	ADD2	ADD1	ADD0

Note: There is no use to have the hardware bit set to 0. As ADFM=0 and when 12-bit resolution, ADDH<7:4> = 0000.

Bits 10~7: Not used, set to "0" all the time.

Bit 6 (TBWEN): Table Write Enable bit.

1: Enable

0: Disable (default)

Bits 5~0 (ID5~ID0): Customer ID Code

6.19 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

“LCALL”, “LJMP”, or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA","SJC","SJNC","SJZ","SJNZ") commands which were tested to be true, are executed within two instruction cycles.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b" represents a bit field designator that selects the value for the bit which is located in the register "R", and affects operation. "k" represents an 8 or 10-bit constant or literal value.

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T,P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
RESET	Software Device Reset	ALL Registers = Reset Value Flags* = Reset Value
TBWR	Table Writer Start instruction	None
INT k	PC+1 → [SP], k*2 → PC	None

Mnemonic	Operation	Status Affected
BTG R,b	Bit Toggle R ; /(R<b>)->R<b> *Range R5~RA	None
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C,DC, OV, N
SUB R,A	R-A → R	Z, C, DC, OV, N
DECA R	R-1 → A	Z, C, DC, OV, N
DEC R	R-1 → R	Z, C, DC, OV, N
OR A,R	A ∨ R → A	Z, N
OR R,A	A ∨ R → R	Z, N
AND A,R	A & R → A	Z, N
AND R,A	A & R → R	Z, N
XOR A,R	A ⊕ R → A	Z, N
XOR R,A	A ⊕ R → R	Z, N
ADD A,R	A + R → A	Z, C, DC, OV, N
ADD R,A	A + R → R	Z, C, DC, OV, N
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z,N
COM R	/R → R	Z,N
INCA R	R+1 → A	Z, C, DC, OV, N
INC R	R+1 → R	Z, C, DC, OV, N
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C,N
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C,N
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C,N
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C,N
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None

Mnemonic	Operation	Status Affected
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None <Note2>
BS R,b	1 → R(b)	None <Note3>
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
JE R	Compare R with ACC, Skip =	None
JGE R	Compare R with ACC, Skip >	None
JLE R	Compare R with ACC Skip <	None
OR A,k	A ∨ k → A	Z,N
JE k	Compare K with ACC, Skip =	None
TBRDA R	ROM[(TABPTR)] → R, A A ← program code (low byte) ; R ← program code (high byte)	None
AND A,k	A & k → A	Z,N
SJC k	Jump to K if Carry *Range [Address+127~-128]	None
SJNC k	Jump to K if Not Carry *Range [Address+127~-128]	None
SJZ k	Jump to K if Zero *Range [Address+127~-128]	None
XOR A,k	A ⊕ k → A	Z,N
SJNZ k	Jump to K if Not Zero *Range [Address+127~-128]	None
RRA R	R(n) → A(n-1), R(0) → A(7)	N
RR R	R(n) → R(n-1), R(0) → R(7)	N
RETL k	k → A, [Top of Stack] → PC	None
XCH R	R ⟷ A	None
RLA R	R(n) → A(n+1), R(7) → A(0)	N
RL R	R(n) → R(n+1), R(7) → R(0)	N
SUB A,k	k-A → A	Z, C, DC, OV, N

Mnemonic	Operation	Status Affected
MUL A,R	PRODH:PRODL = R x A	None
SUBB A,R	R-A-/C → A	Z, C, DC, OV, N
SUBB R,A	R-A-/C → R	Z, C, DC, OV, N
SBANK k	K->R1(5:4)	None
GBANK k	K->R1(1:0)	None
LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→[SP], k→PC	None
LJMP k	Next instruction : k kkkk kkkk kkkk K→PC	None
TBRD R	ROM[(TABPTR)] → R	None
ADD A,k	k+A → A	Z, C, DC, OV, N
NEG R	2's complement, /R +1 → R	Z, C, DC, OV, N
ADC A,R	A+R+C → A	Z, C, DC, OV, N
ADC R,A	A+R+C → R	Z, C, DC, OV, N

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	125°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	3.0V	to	5.5V
Working Frequency	DC	to	32MHz

8 DC Electrical Characteristics

VDD=5.0V, VSS=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	IRC: VDD to 5V	20 MHz,24 MHz,28MHz,32M	–	F	–	MHz
IRCE1	Internal RC oscillator error per stage	IRC:32MHz	–	±0.2	–	%
IRCE2	Internal RC oscillator error per stage	IRC:20,24,28 MHz	–	±1.5	–	%
IRC1	IRC:VDD to 5V	RCM2~RCM0=00	–	20	–	MHz
IRC2	IRC:VDD to 5V	RCM2~RCM0=01	–	24	–	MHz
IRC3	IRC:VDD to 5V	RCM2~RCM0=10	–	28	–	MHz
IRC4	IRC:VDD to 5V	RCM2~RCM0=11	–	32	–	MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9, A	0.7VDD	–	VDD+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9, A	-0.3V	–	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7VDD	–	VDD+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	–	0.3VDD	V
IOH1	Output High Voltage (Ports 5, 6, 7)	VOH = VDD-0.1VDD	-2.2	-3.7	–	mA
IOH2	Output High Voltage(Hi Drive) (Ports 5, 6, 7)	VOH = VDD-0.1VDD	-7.2	-12.0	–	mA
IOL1	Output Low Voltage (Ports 5, 6, 7)	VOL = GND+0.1VDD	12.0	20	–	mA
IOL2	Output Low Voltage(Hi Sink) (Ports 5, 6, 7)	VOL = GND+0.1VDD	19.8	33	–	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-26	-51	-76	μA
IPL	Pull-low current	Pull-low active, input pin at VDD	7	17	42	μA
ISB1	Power down current (Sleep mode)	/RESET= 'High', Fm & Fs off All input and I/O pins at VDD, output pin floating, WDT disabled		1	1.5	μA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ISB2	Power down current (Sleep mode)	/RESET= 'High', Fm & Fs off All input and I/O pins at VDD, output pin floating, WDT enabled		4		µA
ISB3	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=128KHz (IRC type) output pin floating, WDT disabled,		5		µA
ISB4	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=128K/Hz (IRC type), output pin floating, WDT enabled		5		µA
ICC1	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=128KHz (IRC type), output pin floating, WDT disabled		55		µA
ICC2	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=128KHz (IRC type), output pin floating, WDT enabled		55		µA
ICC3	Operating supply current (Green mode)	/RESET= 'High', Fm off, HLP=0,Fs=16KHz (IRC type), output pin floating, WDT enabled		31		µA
ICC4	Operating supply current (Normal mode)	/RESET= 'High', Fm=20MHz (IRC type), Fs on, output pin floating, WDT enabled		4000		µA
ICC5	Operating supply current (Normal mode)	/RESET= 'High', Fm =24MHz (IRC type), Fs on, output pin floating, WDT enabled		4500		µA
ICC6	Operating supply current (Normal mode)	/RESET= 'High', Fm =28MHz (IRC type), Fs on, output pin floating, WDT enabled		5100		µA
ICC7	Operating supply current (Normal mode)	/RESET= 'High', Fm=32MHz (IRC type), Fs on, output pin floating, WDT enabled		5700		µA

Note: *These parameters are theoretical values and have not been tested. Such parameters are for design reference only.*

Data in the Minimum, Typical, Maximum (“Min.”, “Typ.”, “Max.”) columns are based on characterization results at 25°C.

Program Flash Memory Electrical Characteristics (VDD=3.0V to 5.5V, VSS=0V, Ta = -40 to 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 125°C	-	1	-	Ms
Treten	Data Retention		-	10	-	Years
Tendu	Endurance time		-	100K	-	Cycles

9 AC Electrical Characteristics

EM88F794N, (-40 ≤ Ta ≤ 125°C, VDD=5V, VSS=0V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time	RC type	62.5	–	DC	Ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	Ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	Ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	Ms
Tset	Input pin setup time	–	–	0	–	Ns
Thold	Input pin hold time	–	–	20	–	Ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	Ns

Note: *These parameters are theoretical values and have not been tested. Such parameters are for design reference only.*

Data in the Minimum, Typical, Maximum ("Min.", "Typ.", "Max.") columns are based on characterization results at 25°C.

** N = selected prescaler ratio*

A/D Converter Characteristics (VDD=3.0V to 5.5V, VSS=0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operating Range	Vdd	For 5.5v Fs=266kHz, Fin=5kHz For 3.0v Fs=125kHz, Fin=2kHz	3.0	-	5.5	V
	V_{REFT}		3.0	-	Vdd	V
Current Consumption	Ivdd	V_{REFT}= Vdd=5.5V Fs=266kHz, Fin=5kHz	-	-	1.6	mA
	Iref		-	-	100	µA
Standby Current	Isb		-	-	0.1	µA
ZAI	ZAI		-	-	5k	Ω

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SNR	SNR	V_{REFT}= Vdd=4.5V Fs=266kHz, Fin=5kHz	70	-	-	dBc
THD	THD	V_{REFT}= Vdd=4.5V Fs=266kHz, Fin=5kHz	-	-	-70	dBc
SNDR	SNDR	V_{REFT}= Vdd=4.5V Fs=266kHz, Fin=5kHz	68	-	-	dBc
Worst Harmonic	WH	V_{REFT}= Vdd=4.5V Fs=266KHz, Fin=5kHz	-	-	-73	dBc
SFDR	SFDR	V_{REFT}= Vdd=4.5V Fs=266kHz, Fin=5kHz	73	-	-	dBc
Offset Error	OE	V_{REFT}= Vdd=3.3V Fs=100kHz	-	-	+/-4	LSB
Gain Error	GE	V_{REFT}= Vdd=3.3V Fs=100kHz	-	-	+/-8	LSB
DNL	DNL	V_{REFT}= Vdd=3.3V Fs=100KHz, Fin=2kHz	-	-	+/-1	LSB
INL	INL	V_{REFT}= Vdd=3.3V Fs=100KHz, Fin=2kHz	-	-	+/-8	LSB
Conversion Rate	Fs1	Vdd=4.5~5.5V, Fin=5kHz	-	-	266	K SPS
	Fs2	Vdd=3.0~4.5V, Fin=2kHz	-	-	125	K SPS
Power Supply Rejection Ratio	PSRR	V_{REFT}=2.5V Vdd=3.0V ~ 5.5V Fs=125kHz, Vin=0V ~ 2.7V	-	-	2	LSB

Note: *[1]These parameters are hypothetical (not tested) and are provided for design reference only.*

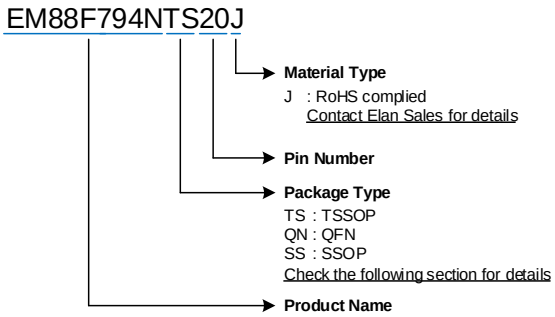
[2]There is no current consumption when ADC is off other than minor leakage current.

[3]The A/D conversion result will not decrease with an increase in the input voltage, and has no missing code.

[4]These parameters are subject to change without prior notice.

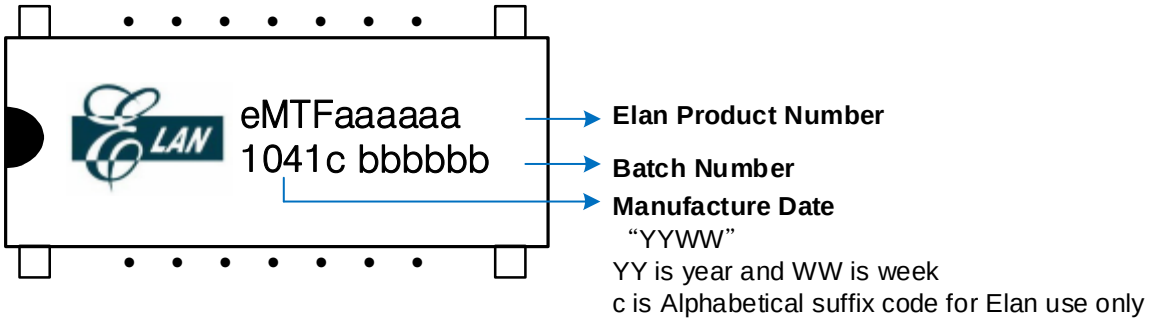
APPENDIX

A Ordering and Manufacturing Information

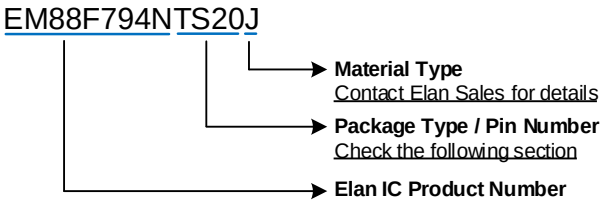


For example:
EM88F794NTS20J
is EM88F758NTS20J with Flash program memory, industrial grade product, in 20-pin TSSOP package with ROHS complied

IC Mark



Ordering Code



B Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM88F794NTS20J	TSSOP	20	173mil

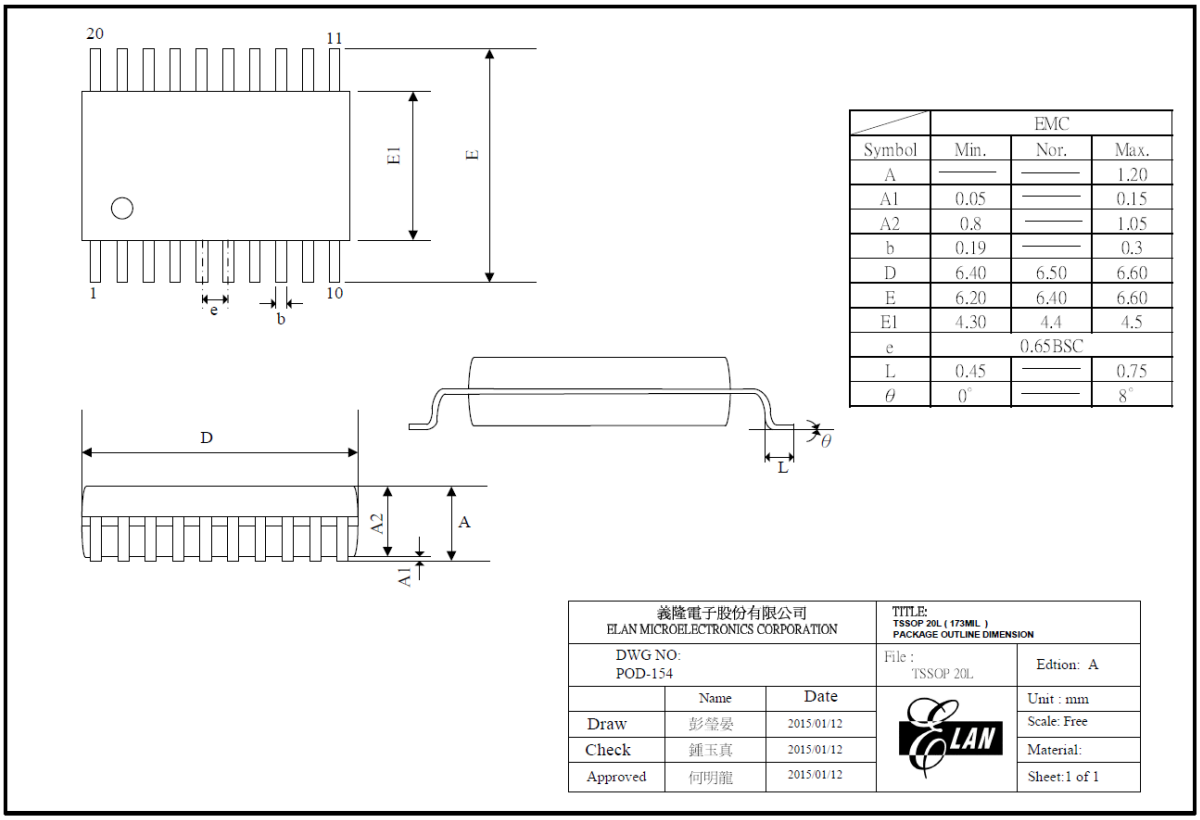
These are Green products which do not contain hazardous substances.

Pb content is less than 100ppm

Part No.	EM88F794NxJ
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Package Information

C.1 EM88F794NTS20



	EMC		
Symbol	Min.	Nor.	Max.
A	———	———	1.20
A1	0.05	———	0.15
A2	0.8	———	1.05
b	0.19	———	0.3
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.4	4.5
e	0.65 BSC		
L	0.45	———	0.75
θ	0°	———	8°

義隆電子股份有限公司 ELAN MICROELECTRONICS CORPORATION			TITLE: TSSOP 20L (173MIL) PACKAGE OUTLINE DIMENSION	
DWG NO: POD-154			File : TSSOP 20L	Edtion: A
	Name	Date		Unit : mm
Draw	彭瑩晏	2015/01/12		Scale: Free
Check	鍾玉真	2015/01/12		Material:
Approved	何明龍	2015/01/12		Sheet:1 of 1

Figure C-1 EM88F794N 20-pin TSSOP Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60% , TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240±5°C)	
Temperature cycle test	-65°C (15mins)~150°C (15min), 200 cycles	
Pressure cooker test	TA =121°C, RH=100%, pressure = 2 atm, TD (endurance)= 96 hrs	
High temperature / High humidity test	TA=85°C , RH=85% , TD (endurance)=168 , 500 hrs	
High-temperature storage life	TA=150°C, TD (endurance)=500, 1000 hrs	
High-temperature operating life	TA=125°C, VDD=Max. operating voltage, TD (endurance) =168, 500, 1000 hrs	
Latch-up	TA=25°C, VDD=Max. operating voltage, 800mA/40V	
ESD (HBM)	TA=25°C, ≥ | ± 4KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+), VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ | ± 400V |	

D.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or alike. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is automactically started. If a noise caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.

E EM88F794N Program Pin List

UWTR is used to program the EM88F794N IC's. The UWTR connector is selected by using Table E-1. The software is selected by EM88F794N.

UWTR-ADP		UWTR-ADP115			
Program Pin Name	**IC Pin Name**	**TSSOP-20 Pin Number**			
2W_SCL	P52	3			
2W_SDA	P60	10			
VDD	VDD	4			
VSS	VSS	19			

Table E-1 EM88F794N Program Pin Lis