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**eLD5016**

**8-BIT  
Microcontroller**

**Product  
Specification**

**DOC. VERSION 1.0**

**ELAN MICROELECTRONICS CORP.**

February 2017


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### Specification Revision History

Doc. Version	Revision Description	Date
1.0	Official original version	2017/2/16

## 1 General Description

This is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. Integrated onto a single chip are on-chip Watchdog Timer (WDT), RAM, ROM, programmable real time clock/counter, internal interrupt, power down mode, ASPCM voice synthesizer (decoder), voice ROM, Current DAC, and tri-state I/O. It provides a single IC solution to design an electric wall mount clock.

## 2 Features

- Single power supply
  - Operating voltage range:
    - 2.5V ~ 3.6V (Normal mode under 14.331 MHz ~ 17.913 MHz)
    - 2.2V ~ 3.6V (Normal mode under 447.829kHz ~ 14.331 MHz)
    - 2.2V ~ 3.6V (Sleep/Idle/Green mode)
- CPU
  - 8-bit RISC kernel
  - 99.9% single instruction cycle commands
- Clock
  - 32.768 kHz clock source
  - Built-in PLL to generate main clock 3.5826 MHz x 0.125, 0.25, 0.5, 1, 2, 3, 4 or 5
- Timer and Counter
  - Watchdog: Programmable free running on-chip Watchdog Timer
  - TCC: 8-bit real time clock/counter (TCC) with 8-bit prescaler
  - Counter 1: 8-bit counter with 8-bit prescaler can be an interrupt source
  - Counter 2: 8-bit counter with 8-bit prescaler can be an interrupt source
- Memory
  - 16k x 13 on-chip program ROM
  - 40k x 5 on-chip voice ROM (the max. timing from voice ROM enable to its data finish = 1.25 μs)
  - 0.25k x 8 on-chip Data RAM
  - 144 x 8 common registers
- I/O
  - Up to 26 bi-directional tri-state I/O ports (18 independent I/O)
  - I/O with internal Pull high, wake-up and interrupt functions
- Operation Mode
 

Three modes can be selected (Main clock is generated by internal PLL)

Mode	CPU Status	Main Clock	32768 Hz Clock
Sleep mode	Turn off	Turn off	Turn off
Idle mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on
- Interrupt
  - Selective signal sources and overflow interrupt
  - Stack: 8-level stack for subroutine nesting
  - Eight interrupt sources: 4 external, 4 internal
- Reset
  - Power-on reset, /POVD reset (by code option) or external /RESET pin
- DAC
  - 8-bit current DAC
  - Can be accessed by ASPCM hardware or from DAC input register
- Package
  - 42-pad die (eLD5016H)

### 3 Pin Assignment

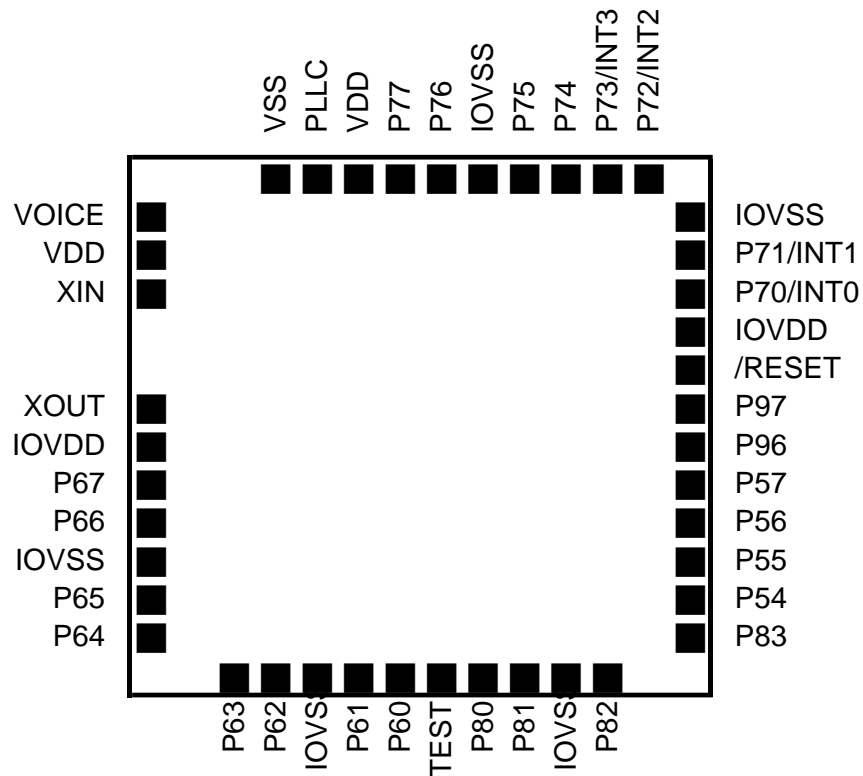


Figure 3-1 42-Pin eLD5016 Pin Assignment

## 4 Pin Description

Name	Function	Input Type	Output Type	Description
<b>Power</b>				
IOVDD		Power	–	VDD for I/O
VDD		Power	–	VDD for other circuit
IOVSS		Ground		GND for I/O
VSS		Ground	–	GND for circuit
<b>Clock for MCU</b>				
XIN		XTAL		Input pin for 32768 Hz crystal
XOUT			XTAL	Output pin for 32768 Hz crystal
PLLCC		AN		Phase locked loop capacitor; connect a 0.01 $\mu$ to 0.047 $\mu$ capacitor to the ground.
<b>Current DAC</b>				
Voice			AN	DAC output
<b>Test</b>				
TEST		ST		Test pin into test mode, normal low
<b>Reset</b>				
/RESET		ST		Reset input. Low enable
<b>I/O</b>				
P54 ~ P57	P54 ~ P57	ST	CMOS	Bidirectional I/O pin
P60 ~ P67	P60 ~ P67	ST	CMOS	Bidirectional I/O pin
P70 / INT0 P71 / INT1 P72 / INT2 P73 / INT3	P70 ~ P73	ST	CMOS	Bidirectional I/O pin with programmable pull- high
	INT0~INT3	ST	–	External interrupt pin triggered by a falling edge
P74 ~ P75	P74 ~ P75	ST	CMOS	Bidirectional I/O pin
P76, P77	P76, P77	ST	CMOS	Bidirectional I/O pin with programmable open-drain
P80 ~ P83	P74 ~ P77	ST	CMOS	Bidirectional I/O pin
P96, P97	P96, P97	ST	CMOS	Bidirectional I/O pin and wake-up pin from sleep mode when the pin status changes.



## 5.1 Operational Registers

### 5.1.1 R0 (IndA: Indirect Addressing Register)

R0 is not a physically implemented register. It is useful as an indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
MOV  A, @0x20    ; store an address at R4 for indirect addressing
MOV  0x04, A
MOV  A, @0xAA    ; write data 0xAA to R20 at Bank0 through R0
MOV  0x00, A
```

### 5.1.2 R1 (TCCD: TCC Data)

- Increased by the instruction cycle clock.
- Writable and readable by the program as any other register.
- Defined by PAB (CONT-3) reset.
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when the TCC register is written with a value.

### 5.1.3 R2 (PC: Program Counter and Stack)

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.

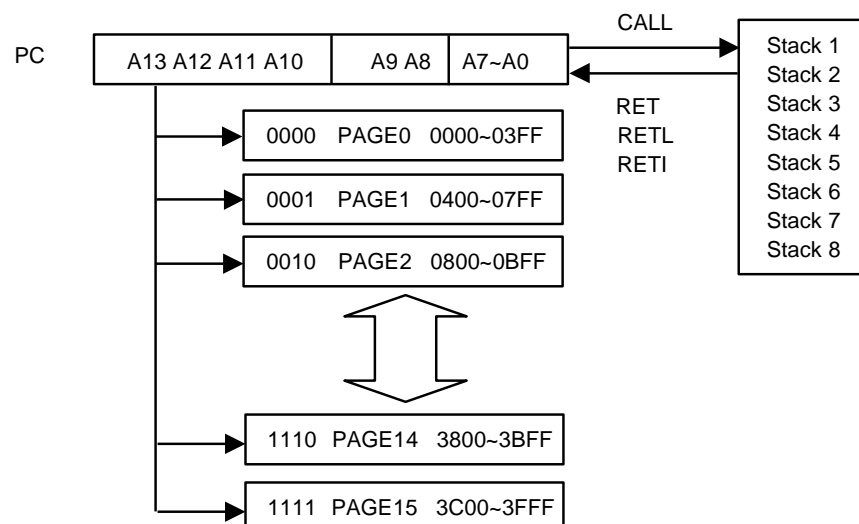


Figure 5-3 Program Counter Organization



- The configuration structure generates 16k × 13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0" under RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC + 1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- Any instruction written to R2 (e.g., "ADD R2, A", "MOV R2, A", "BC R2, 6", etc.) will cause the 9<sup>th</sup> and the 10<sup>th</sup> bits (A8 ~ A9) of the PC to be cleared. Hence, the computed jump is limited to the first 256 locations of a page.
- "TBL" allows a relative address to be added to the current PC while contents of the 9<sup>th</sup> and the 10<sup>th</sup> bits remain unchanged. The most significant bits (A10 ~ A13) will be loaded with the content of bit PS0 ~ PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2, A", or "MOV R2, A" instruction.
- The Data Memory Configuration is as follows:

	R PAGE Registers		IOC PAGE	
Addr	R PAGE0	R PAGE1	IOC PAGE0	IOC PAGE1
00	<b>INDA</b> Indirect addressing			
01	<b>TCCD</b> TCC data			
02	<b>PC</b> Program counter			
03	<b>STA</b> IOC Page, Status			
04	<b>RBSR</b> Register bank, RSR			
05	<b>P5IOD</b> Port 5 I/O data, Program page	<b>CDAD</b> Current DAC input data	<b>P5IOC</b> Port 5 I/O control, (P76, P77) open drain	<b>CDAC</b> Clear CDA, ASPCM rate and volume control
06	<b>P6IOD</b> Port 6 I/O data		<b>P6IOC</b> Port 6 I/O control	<i>(undefined, non-existent and set to "0" at all time)</i>

Addr	R PAGE Registers		IOC PAGE	
	R PAGE0	R PAGE1	IOC PAGE0	IOC PAGE1
07	<b>P7IOD</b> Port7 I/O data		<b>P7IOC</b> Port 7 I/O control	<b>VRAH</b> VROM Addr (8~15)
08	<b>P8IOD</b> Port 8 I/O date		<b>P8IOC</b> Port 8 I/O control	<b>VRAL</b> VROM Addr (0~7)
09	<b>P9IOD</b> Port 9 I/O data		<b>P9IOC</b> Port 9 I/O control	<b>VRD</b> VROM data
0A	<b>MCUC</b> CPU power saving, PLL, Main clock, VROM status, R page			<b>DEDC</b> DAC stop, ROM and DA switch
0B	<b>ASPC</b> ASPCM control			<b>CN1D</b> Counter 1 data
0C	<b>RAMA</b> Data RAM address			<b>CN2D</b> Counter 2 data
0D	<b>RAMD</b> Data RAM data			<b>P7PHC</b> Port 7 pull high
0E	<b>WUPC</b> Wake-up control, Port 8 high nib, switch			<b>CNPSC</b> CNT1, 2 Clk source and prescaler
0F	<b>INTF</b> Interrupt flag		<b>INTM</b> Interrupt mask	
10	16 bytes			
:	Common registers			
1F				
20	Bank 0~Bank 3			
:	Common registers			
3F	(32x8 for each bank)			

Figure 5-4 Data Memory Configuration

### 5.1.4 R3 (STA: IOC Page, Status Flags)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCPAGE	-	-	T	P	Z	DC	C
R/W-0	R-0	R-0	R	R	R/W	R/W	R/W

**Bit 7 (IOCPAGE):** Change IOC5 ~ IOCE to another page

0: IOC PAGE0

1: IOC PAGE1

**Bits 6 ~ 5:** Undefined bits, set to "0" at all time

**Bit 4 (T):** Time-out bit

Set to "1" with "SLEP" and "WDTC" commands or during power up, and reset to "0" by WDT time-out.

**Bit 3 (P):** Power down bit

Set to "1" during power on or by a "WDTC" command, and reset to "0" by a "SLEP" command.

Event	T	P	Remark
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
power up	1	1	
Low pulse on /RESET	x	x	X: Don't care

**Bit 2 (Z):** Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

**Bit 1 (DC):** Auxiliary carry flag

**Bit 0 (C):** Carry flag

### 5.1.5 R4 (RBSR: RAM Bank, RAM Select for Common Registers R20 ~ R3F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

**Bits 7 ~ 6 (RB1 ~ 0):** Bank select bits for Common Registers R20 ~ R3F

These select bits are used to determine which bank is activated among the four banks for 32 registers (R20 to R3F). Refer to Figure 5-3 *Control Register Configuration* for details.

**Bits 5 ~ 0 (RSR5 ~ 0):** Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in indirect addressing mode. For the Data Memory Configuration, refer to Figure 5-3.

### 5.1.6 R5 (P5IOD: Port 5 I/O Data, Program ROM Page Select)

*Page 0 (P5IOD: Port 5 I/O Data)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	PS3	PS2	PS1	PS0
R/W	R/W	R/W	R/W	R/W-0	R/W-0	R/W-0	R/W-0

**Bits 7 ~ 4 (P57 ~ P54):** 4-bit Port 5 (7 ~ 4) I/O data register

**Bits 3 ~ 0 (PS3 ~ 0):** Page selection bits

They should be set before JMP or CALL instruction.

Page select bits

PS3	PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3
:	:	:	:	:
1	1	1	0	Page 14
1	1	1	1	Page 15

User can use PAGE instruction to change page and maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. The program page is maintained by Elan's compiler. It will change user's program by inserting instructions within the program.

*Page 1 (CDAD: Current DAC Input Data Buffer)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CDAD7	CDAD6	CDAD5	CDAD4	CDAD3	CDAD2	CDAD1	CDAD0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bits 7 ~ 0 (CDAD7 ~ 0):** Current DAC input data buffer

### 5.1.7 R6 (P6IOD: Port 6 I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Bits 7 ~ 0 (P67 ~ P60):** 8-bit Port 6 (0~7) I/O data register

User can use the IOC register to define each bit as input or output.

### 5.1.8 R7 (P7IOD: Port 7 I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Bits 7 ~ 0 (P77 ~ P70):** 8-bit Port 7 (0~7) I/O data register

User can use the IOC register to define each bit as input or output.

### 5.1.9 R8 (P8IOD: Port 8 I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	P83	P82	P81	P80
R-0	R-0	R-0	R-0	R/W	R/W	R/W	R/W

**Bits 7 ~ 4:** Undefined bits, always "0"

**Bits 3 ~ 0 (P83 ~ P80):** 4-bit Port 8 (3~0) I/O data register

User can use the IOC register to define each bit as input or output.

### 5.1.10 R9 (P9IOD: Port 9 I/O Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	0	0	0	0	0	0
R/W	R/W	R-0	R-0	R-0	R-0	R-0	R-0

**Bits 7 ~ 6 (P97, P96):** 2-bit Port 9 (7~6) I/O data register

User can use the IOC register to define each bit as input or output.

**Bits 5 ~ 0:** Undefined bits, set to "0" at all time

### 5.1.11 RA (MCUC: CPU Power Saving, PLL, Main Clock Selection, R Page)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDLE	ENPLL	CLK2	CLK1	CLK0	0	STA_VR	RPAGE
R/W-0	R/W-0	R/W-0	R/W-0	RW-0	R-0	R-1	RW-0

**Bit 7 (IDLE):** Idle mode/Sleep mode select bit

**0:** Sleep mode

**1:** Idle mode

This bit will determine which mode to go after SLEP instruction.

These two modes can be awakened by TCC clock, Watchdog timer (WDT), Ports 97~96, or Ports 70~73, and run from "SLEP" next instruction.

Wakeup Signal	Sleep mode	Idle mode	Green mode	Normal mode
	RA(7,6) = (0,0) + SLEP	RA(7,6) = (1,0) + SLEP	RA(7,6) = (x,0) no SLEP	RA(7,6) = (x,1) no SLEP
TCC time out	x	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
WDT time out	Reset	Wake-up + Next instruction	Reset	Reset
Ports 96, 97	Reset	Wake-up + Next instruction	x	x
Ports 70 ~ 73	Reset	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt

P73 ~ P70's wakeup functions are controlled by IOCF (1, 2, 3) and ENI instructions.

CONT REGISTER Bit 7 defines whether P70's wakeup signal is a rising or falling edge.

Port 97, Port 96, Port 73, Port 72 and Port 71's wake-up patterns are falling edge trigger signals.

**Bit 6 (ENPLL):** PLL's power control bit is CPU mode control register

**0:** Disable PLL

**1:** Enable PLL

If PLL is enabled, CPU will operate at normal mode (high frequency). Otherwise, it will run at green mode (low frequency, 32768 Hz).

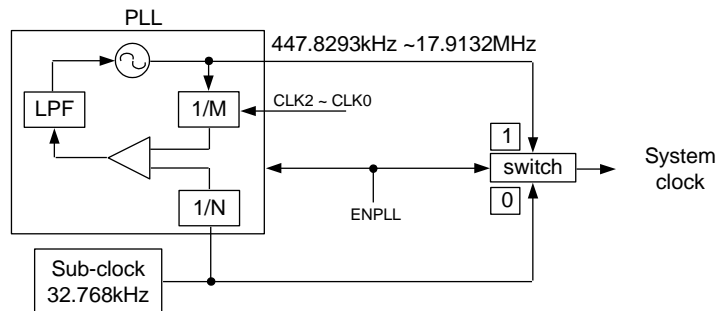


Figure 5-5 Correlation between 32768 Hz and Main clock

**Bits 5 ~ 3 (CLK2 ~ 0):** Main clock select bits.

User can choose different frequencies for the main clock through CLK1 and CLK2. All clock selections are listed below.

PLLEN	CLK2	CLK1	CLK0	Sub clock	Main clock	CPU clock
1	0	0	0	32768 Hz	447.829 kHz	447.829 kHz (Normal mode)
1	0	0	1	32768 Hz	895.658 kHz	895.658 kHz (Normal mode)
1	0	1	0	32768 Hz	1.791 MHz	1.791 MHz (Normal mode)
1	0	1	1	32768 Hz	3.582 MHz	3.582 MHz (Normal mode)
1	1	0	0	32768 Hz	7.165 MHz	7.165 MHz (Normal mode)
1	1	0	1	32768 Hz	10.747 MHz	10.747 MHz (Normal mode)
1	1	1	0	32768 Hz	14.331 MHz	14.331 MHz (Normal mode)
1	1	1	1	32768 Hz	17.913 MHz	17.913 MHz (Normal mode)
0	Don't care			32768 Hz	Don't care	32768 Hz (Green mode)

**Bit 2:** Undefined bit, set to “0” at all time

**Bit 1 (STA\_VR):** Status flag for voice ROM operation

**0:** Voice ROM busy

**1:** Voice ROM data ready

When this flag is “0”, the bus of the voice ROM is busy processing its data. When this flag is “1”, the bus of the Voice ROM is on standby and its data is ready for users to read.

**Bit 0 (RPAGE):** Change R PAGE 5 to another page

**0:** R5 PAGE0

**1:** R5 PAGE1

### 5.1.12 RB (ASPC: ASPCM Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PLAY	S/P	-	-	-	-
R-0	R-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0

**Bits 7 ~ 6:** Undefined bits, set to "0" at all time

**Bit 5 (PLAY):** voice-playing control

**0:** Disable voice-playing

**1:** Enable voice-playing

PLAY	S/P	Function	Description
1 → 0	0	Stop-playing	The playing address is reset to the beginning of the play. D/A data is reset.
	1	Pause-playing	The playing address is not reset.
0 → 1	0	Playing from stop	The playing address is reset to the beginning of the play. D/A data is reset. Then it begins to play.
	1	Playing from pause	The playing address is not reset and it plays again.

Note: While playing voice by setting (PLAY, S/P) = (1, 0) or (1, 1), if the play comes to an end (meet the stop code), the (PLAY, S/P) bits will automatically clear to (0, 0).

**Bit 4 (S/P):** Setting for voice stop-playing and voice pause-playing

**0:** Voice stop-playing

**1:** Voice pause-playing

**Bits 3 ~ 0:** Undefined bits, set to "0" at all time

### 5.1.13 RC (RAMA: Data RAM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATAA7	DATAA6	DATAA5	DATAA4	DATAA3	DATAA2	DATAA1	DATAA0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bits 7 ~ 0 (DATAA7 ~ 0):** Data RAM address

User can select Data RAM Address from 0 to 255.

### 5.1.14 RD (RAMD: Data RAM Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATAD7	DATAD6	DATAD5	DATAD4	DATAD3	DATAD2	DATAD1	DATAD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Bits 7 ~ 0 (DATAD7 ~ 0):** Data RAM data register.

User can see the IOCA register as to how to select Data RAM banks.

### 5.1.15 RE (WUPC: Wake-up Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	/WDTE	/WUP97	/WUP96	0	0	0	0
R-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0

**Bit 7:** 1 bit, set to “0” at all time

**Bit 6 (/WDTE):** Watchdog Timer enable control bit

0: Disable WDT

1: Enable WDT

**Bit 5 (/WUP97):** Port 9 Bit 7 wake-up control

0: Disable

1: Enable

**Bit 4 (/WUP96):** Port 9 Bit 6 wake-up control

0: Disable

1: Enable

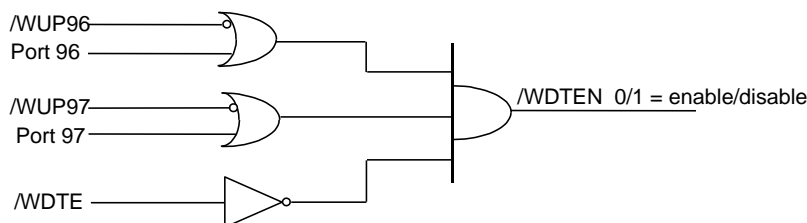


Figure 5-6 Wake up Function and Control Signal

**Bits 3 ~ 0:** Undefined bits, set to “0” at all time

### 5.1.16 RF (INTF: Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIF
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Note:** “1” means with interrupt request “0” means no interrupt occurs

**Bits 7 ~ 6:** Undefined bits, set to “0” at all time

**Bit 5 (CNT2):** 8 bit Counter 2 overflow interrupt flag.

It will be set when Counter 2 overflows.

**Bit 4 (CNT1):** 8 bit Counter 1 overflow interrupt flag.

It will be set when Counter 1 overflows.

**Bit 3 (INT2 / INT3):** External INT2 and INT3 pins interrupt flag. Set by a falling edge on the /INT2 and /INT3 pins, reset by software.

It can be used when Port 72 or Port 73 is set to input port.

**Bit 2 (INT1):** External INT1 pin interrupt flag. Set by a falling edge on /INT pin, reset by software.

It can be used when Port 71 is set to input port.

**Bit 1 (INT0):** External INT0 pin interrupt flag. Set by a falling edge on /INT pin, reset by software.

It can be used when Port 70 is set to input port.

**Bit 0 (TCIF):** TCC Timer Overflow Interrupt Flag. It will be set when TCC timer overflows, reset by software.

INT0 ~ INT3 interrupts are edge triggering (falling edge or rising edge) which can be set by CONT Bit 7 (INT\_EDGE). Also, see corresponding interrupt mask in IOCF register. User can read and clear.

RF can be cleared by instruction but cannot be set.

**NOTE**

*The result of reading RF is the "Logic AND" of RF and IOCF.*

### 5.1.17 R10 ~ R3F

R10 ~ R3F (Banks 0~3) are all general-purpose registers.

## 5.2 Special Function Registers

### 5.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

### 5.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	-	PAB	PSR2	PSR1	PSR0
R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

The CONT register is both readable and writable by instruction “CONTW” and “CONTR”.

**Bit 7 (INT\_EDGE):** interrupt edge type of P70

**0:** P70's interrupt sources are rising and falling edge signals.

**1:** P70's interrupt source is a falling edge signal.

**Bit 6 (INT):** Interrupt Enable flag

**0:** Masked by DISI or hardware interrupt

**1:** Enabled by ENI / RETI instructions

**Bit 5 (TS):** TCC signal source

**0:** Instruction clock

**1:** 16384 Hz

Instruction clock = MCU clock / 2. Refer to RA Bits 4 ~ 6 for PLL and Main clock selection. See Figure 5-5 for details.

**Bit 4:** Undefined bits, set to “0” at all time

**Bit 3 (PAB):** Prescaler Assignment Bit

**0:** TCC

**1:** WDT

**Bits 2 ~ 0 (PSR2 ~ PSR0):** TCC / WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

### 5.2.3 IOC5 (P5IOC, CDAC)

*Page 0 (P5IOC: Port 5 I/O Control, P7 (7, 6) Open Drain)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	IOC54	0	0	OP77	OP76
R/W-1	R/W-1	R/W-1	R/W-1	RW-0	RW-0	RW-0	RW-0

**Bits 7 ~ 4 (IOC57 ~ IOC54):** Port 5 (4 ~ 7) I/O direction control register

**0:** put the relative I/O pin as output

**1:** put the relative I/O pin into high impedance

**Bits 3 ~ 2:** Undefined bits, set to "0" at all time

**Bit 1 (OP77):** P77 open-drain control bit

**0:** Disable open-drain output

**1:** Enable open-drain output

**Bit 0 (OP76):** P76 open-drain control bit

**0:** Disable open-drain output

**1:** Enable open-drain output

Page 1 (CDAC: Clear CDA Data, Voice Synthesizer Sampling Rate and Volume Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLDA	RATE2	RATE1	RATE0	VOL3	VOL2	VOL1	VOL0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bit 7 (CLDA):** Current D/A data clear enable control

**0:** Disable

**1:** Enable

When this bit is set (enabled), the internal Current D/A data will be cleared and its output will go to ground level with the VOICE pin connecting a resistor to ground. After setting this bit, remember to clear (disable) it again otherwise it will keep outputting to ground level no matter if voice ROM is playing or not.

**Bits 6 ~ 4 (RATE2 ~ 0):** Voice synthesizer sampling rate control

RATE2 ~ 0	Sampling Rate
000	x
001	x
010	$32768 \text{ Hz} / 2 = 16384 \text{ Hz}$
011	$32768 \text{ Hz} / 3 = 10922.7 \text{ Hz}$
100	$32768 \text{ Hz} / 4 = 8192 \text{ Hz}$
101	$32768 \text{ Hz} / 5 = 6553.6 \text{ Hz}$
110	$32768 \text{ Hz} / 6 = 5461.3 \text{ Hz}$
111	$32768 \text{ Hz} / 7 = 4681.1 \text{ Hz}$

**Bits 3 ~ 0 (VOL3 ~ 0):** Voice synthesizer volume control

VOL3 ~ 0	Max. Voice Output Current (mA)
0000	0
0001	$5 \times 2 / 16 \text{ mA} = 0.625 \text{ mA}$
0010	$5 \times 3 / 16 \text{ mA} = 0.9375 \text{ mA}$
0011	$5 \times 4 / 16 \text{ mA} = 1.25 \text{ mA}$
0100	$5 \times 5 / 16 \text{ mA} = 1.5625 \text{ mA}$
0101	$5 \times 6 / 16 \text{ mA} = 1.875 \text{ mA}$
0110	$5 \times 7 / 16 \text{ mA} = 2.1875 \text{ mA}$
0111	$5 \times 8 / 16 \text{ mA} = 2.5 \text{ mA}$
1000	$5 \times 9 / 16 \text{ mA} = 2.8125 \text{ mA}$
1001	$5 \times 10 / 16 \text{ mA} = 3.125 \text{ mA}$

<b>VOL3 ~ 0</b>	<b>Max. Voice Output Current (mA)</b>
1010	$5 \times 11 / 16 \text{ mA} = 3.4375 \text{ mA}$
1011	$5 \times 12 / 16 \text{ mA} = 3.75 \text{ mA}$
1100	$5 \times 13 / 16 \text{ mA} = 4.0625 \text{ mA}$
1101	$5 \times 14 / 16 \text{ mA} = 4.375 \text{ mA}$
1110	$5 \times 15 / 16 \text{ mA} = 4.6875 \text{ mA}$
1111	5 mA

### 5.2.4 IOC6 (P6IOC)

Page 0 (P6IOC: Port 6 I/O Control)

<b>Bit 7</b>	<b>Bit 6</b>	<b>Bit 5</b>	<b>Bit 4</b>	<b>Bit 3</b>	<b>Bit 2</b>	<b>Bit 1</b>	<b>Bit 0</b>
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

**Bits 7 ~ 0 (IOC67 ~ IOC60):** Port 6 (7 ~ 0) I/O direction control register

**0:** put the relative I/O pin as output

**1:** put the relative I/O pin into high impedance

### 5.2.5 IOC7 (P7IOC, VRAH)

Page 0 (P7IOC: Port 7 I/O Control)

<b>Bit 7</b>	<b>Bit 6</b>	<b>Bit 5</b>	<b>Bit 4</b>	<b>Bit 3</b>	<b>Bit 2</b>	<b>Bit 1</b>	<b>Bit 0</b>
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

**Bits 7 ~ 0 (IOC77 ~ IOC70):** Port 7 (0~7) I/O direction control register

**0:** put the relative I/O pin as output

**1:** put the relative I/O pin into high impedance

Page 1 (VRAH: Voice ROM Address (8~15))

<b>Bit 7</b>	<b>Bit 6</b>	<b>Bit 5</b>	<b>Bit 4</b>	<b>Bit 3</b>	<b>Bit 2</b>	<b>Bit 1</b>	<b>Bit 0</b>
VRA15	VRA14	VRA13	VRA12	VRA11	VRA10	VRA9	VRA8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bits 7 ~ 0 (VRA15 ~ 8):** Voice ROM address register bit (15 ~ 8)

Voice ROM address can be accessed to a maximum of 40k-1.

## 5.2.6 IOC8 (P8IOC, VRAL)

Page 0 (P8IOC: Port 8 I/O Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	IOC83	IOC82	IOC81	IOC80
R-0	R-0	R-0	R-0	R/W-1	R/W-1	R/W-1	R/W-1

**Bits 7 ~ 4:** Undefined bits, set to “0” at all time

**Bits 3 ~ 0 (IOC83 ~ IOC80):** Port 8 (0~3) I/O direction control register

**0:** put the relative I/O pin as output

**1:** put the relative I/O pin into high impedance

Page 1 (VRAL: Voice ROM Address (0~7))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRA7	VRA6	VRA5	VRA4	VRA3	VRA2	VRA1	VRA0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bits 7 ~ 0 (VRA7 ~ 0):** voice ROM address register bit (7 ~ 0)

*Voice ROM address can be accessed to a maximum of 40k-1.*

## 5.2.7 IOC9 (P9IOC, VRD)

Page 0 (P9IOC: Port 9 I/O Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	0	0	0	0	0	0
R/W-1	R/W-1	R-0	R-0	R-0	R-0	R-0	R-0

**Bits 7 ~ 6 (IOC97 ~ IOC96):** Port T9 (7 ~ 6) I/O direction control register

**0:** put the relative I/O pin as output

**1:** put the relative I/O pin into high impedance

**Bits 5 ~ 0:** Undefined bits, set to “0” at all time

Page 1 (VRD: Voice ROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	VRD4	VRD3	VRD2	VRD1	VRD0
R-0	R-0	R-0	R/W	R/W	R/W	R/W	R/W

**Bits 7 ~ 5:** Undefined bits, set to “0” at all time

**Bits 4 ~ 0 (VRD4 ~ 0):** 8-bit voice ROM data register

### 5.2.8 IOCA (DAPC)

Page 1 (DAPC: DAC Power Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/DASTOP	0	0	0	VRDASW	0	0	0
R/W-0	R-0	R-0	R-0	R/W	R-0	R-0	R-0

**Bit 7 (DASTOP):** D/A stop conversion and power down

0: Disable and power down D/A

1: Enable and power on D/A

**Bits 6 ~ 4:** Undefined bits, set to "0" at all time

**Bit 3 (VRDASW):** Voice ROM & Current D/A access selection.

0: Access voice ROM memory, current D/A input are controlled by ASPCM hardware (ASPCM mode)

1: Access voice ROM memory, current D/A input can be directly accessed from their relative registers by software (S/W mode)

**Bits 2 ~ 0:** Undefined bits, set to "0" at all time

### 5.2.9 IOCB (CN1D)

Page 1 (CN1D: Counter 1 Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bits 7 ~ 0 (CN17 ~ CN10):** Counter1's buffer that user can read and write.

Counter 1 is an 8 bit up-counter preset and read out register.  
(Write = preset). After an interrupt, it will reload the preset value.

### 5.2.10 IOCC (CN2D)

Page 1 (CN2D: Counter 2 Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bits 7 ~ 0 (CN27 ~ CN20):** Counter 2's buffer that user can read and write.

Counter 2 is an 8 bit up-counter preset and read out register.  
(Write = preset). After an interrupt, it will reload the preset value.

### 5.2.11 IOCD (P7PHC)

Page 1 (P7PHC: Port 7 Pull high control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bits 7 ~ 0 (PH7 ~ 0):** Port 7 Pull high control bits

**0:** Disable internal pull-high

**1:** Enable internal pull-high

These control bits are used to enable the pull-high of Port 7 (0 ~ 7) pins.

### 5.2.12 IOCE (CNPSC)

Page 1 (CNPSC: Counter 1, 2 Clock Source and Prescaler)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	C2_PSC2	C2_PSC1	C2_PSC0	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bit 7 (CNT2S):** Counter 2 source

**0:** 32768Hz

**1:** Instruction clock which Instruction clock period = 2 x Main clock period

**Bits 6 ~ 4 (C2\_PSC2 ~ C2\_PSC0):** Counter 2 prescaler setting, described in the following table.

**Bit 3 (CNT1S):** Counter1 source

**0:** 32768Hz

**1:** Instruction clock which Instruction clock period = 2 x Main clock period

**Bits 0 ~ 2 (C1\_PSC2 ~ C1\_PSC0):** Counter 1 prescaler setting, described in the following table.

Reset = (0,0,0)

(C1_PSC2, C1_PSC1, C1_PSC0) (C2_PSC2, C2_PSC1, C2_PSC0)	Scaler Ratio
(0,0,0)	1:1
(0,0,1)	1:2
(0,1,0)	1:4
(0,1,1)	1:8
(1,0,0)	1:16
(1,0,1)	1:32
(1,1,0)	1:64
(1,1,1)	1:128

### 5.2.13 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CNT2	CNT1	INT2/INT3	INT1	INT0	TCIE
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**Bits 7 ~ 6:** Undefined bits, set to "0" at all time

**Bits 5 ~ 0:** Interrupt enable bit

**0:** Disable interrupt

**1:** Enable interrupt, Instruction clock period = 2 x Main clock period

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.

The IOCF Register is both readable and writable. They work with RF registers.

### 5.3 TCC / WDT and Prescaler

An 8-bit counter is available as prescaler for either TCC or WDT.

- An 8-bit counter is available for either TCC or WDT, determined by the status of Bit 3 (PAB) of the CONT register.
- See the prescaler ratio in the CONT register.
- Figures 5-7 depict the circuit diagram of TCC/WDT.
- Both TCC and the prescaler will be cleared by instructions which write to TCC each time.
- The prescaler will be cleared by the WDTC and SLEP instructions when assigned to WDT mode.
- The prescaler will not be cleared by SLEP instructions when assigned to TCC mode.

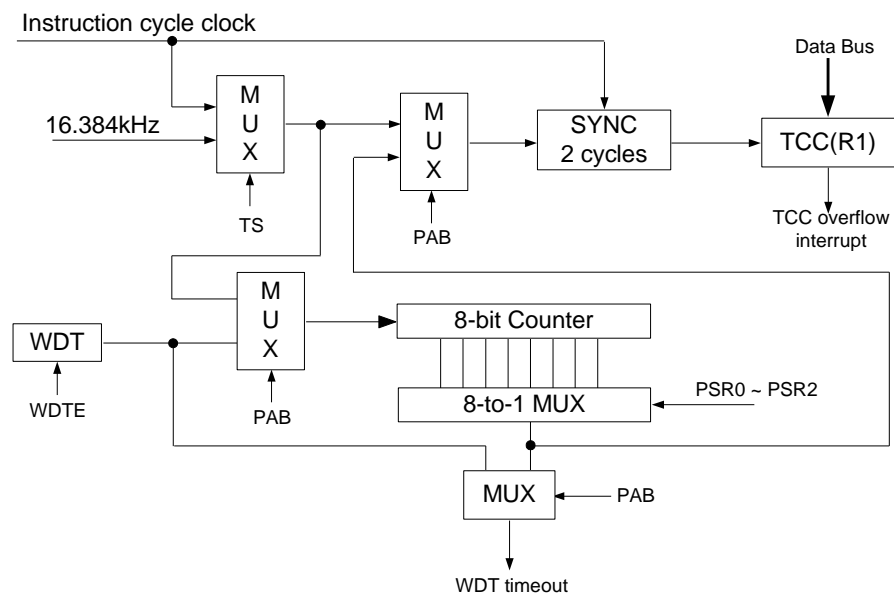


Figure 5-7 TCC and WDT Block Diagram

## 5.4 I/O Ports

The I/O registers, Port 5 ~ Port 9, are bidirectional tri-state I/O ports. Port 7 can be pulled-high internally by software control. In addition, P66 and P67 can also have open-drain outputs through software control. Wake-up functions are available from P96 and P97. Each I/O pin can be defined as an "input" or "output" pin by the I/O control registers (IOC5 ~ IOC9). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 9 are shown in Figure 5-8.

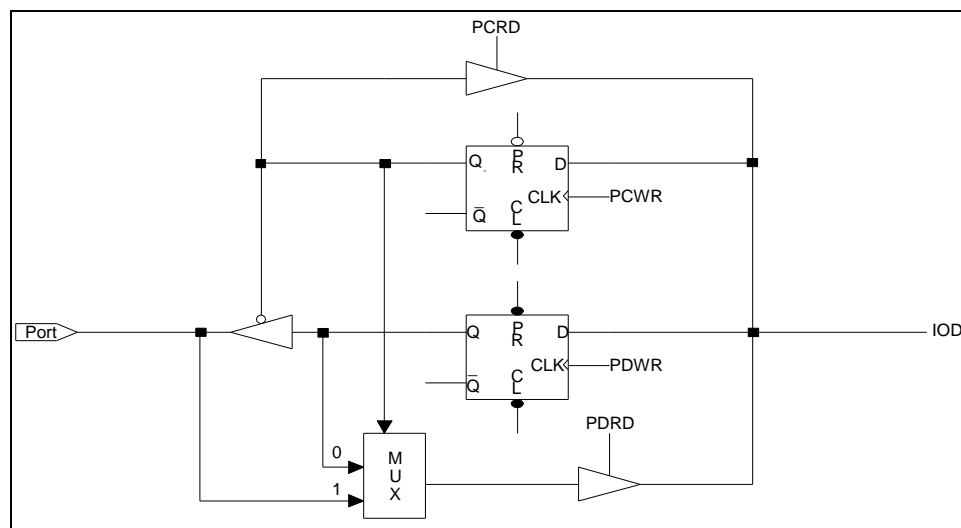


Figure 5-8 Circuit of I/O Port and I/O Control Register Circuit

## 5.5 Reset and Wake-up

A RESET can be caused by:

- (1) External /RESET pin
- (2) Power on reset or Power on voltage detector reset (/POVD reset)
- (3) WDT timeout (If enabled and in Green or Normal mode)

Note that only Power on reset or Power on voltage detector reset in Case (2) are enabled in the system by Code Option bit. If /POVDs are disabled, Power on reset is selected in Case (2). Refer to Figure 5-9.

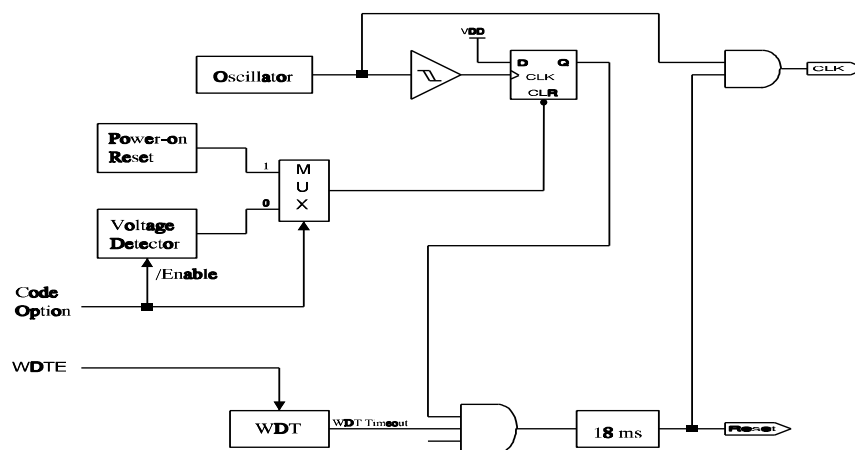


Figure 5-9 Block Diagram of Reset of controller

Once RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1".
- The other registers (Bit 7...Bit 0)



R5 Page 0 = "xxxx0000"	R5 Page1 = "00000000"	IOC5 Page 0 = "11110000"	IOC5 Page1 = "00000000"
R6 = Port		IOC6 Page 0 = "11111111"	
R7 = Port		IOC7 Page 0 = "11111111"	IOC7 Page1 = "00000000"
R8 = "0000xxxx"		IOC8 Page 0 = "00001111"	IOC8 Page1 = "00000000"
R9 = "xx000000"		IOC9 Page 0 = "11000000"	IOC9 Page1 = "000xxxxx"
RA = "00000010"			IOCA Page1 = "00000000"
RB = "0000x000"			IOCB Page1 = "00000000"
RC = "00000000"			IOCC Page1 = "00000000"
RD = "xxxxxxxxxx"			IOCD Page1 = "00000000"
RE = "00000000"			IOCE Page1 = "00000000"
RF = "00000000"		IOCF = "00000000"	

The controller can be awakened from Sleep mode (execution of "SLEP" instruction, named as Sleep mode) by (1) WDT time-out (if enabled) (2) external input at Port 9. After the CPU wakes-up, user should control the Watchdog in case of reset in Green mode or Normal mode. These two cases will set an RF flag.

## 5.6 Interrupt

The MCU has internal interrupts which are falling edge triggered, as follows: TCC timer overflow interrupt (internal), two 8-bit counters overflow interrupt.

If these interrupt sources change signal from high to low, the RF register will generate '1' flag to the corresponding register if IOCF register is enabled.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetched from Address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in the software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

There are four external interrupt pins including INT0, INT1, INT2, and INT3. And four internal counter interrupts available.

Signals of external interrupt INT0, INT1, INT2, and INT3 are from Port 7 Bit 0 to Bit 3. If IOCF is enabled, these signals will cause an interrupt, or these signals will be treated as general input data.

After reset, the next instruction will be fetched from Address 000H, the Instruction Interrupt is 001H and the Hardware Interrupt is 008H.

**TCC will go to Address 0x08 in Green mode or Normal mode after time out.  
These two cases will set the RF flag.**

## 5.7 Instruction Set

Instruction set has the following features:

- (1) Every bit of any register can be set, cleared, or tested directly.
- (2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. The symbol "k" represents an 8 or 10-bit constant or literal value.

Mnemonic	Operation	Status Affected
NOF	No Operation	None
DAA	Decimal Adjust A	C
CONTW	A → CONT	None
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
IOW R	A → IOCR	None
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC Enable Interrupt	None
CONTR	CONT → A	None
IOR R	IOCR → A	None
TBL	R2+A → R2 Bits 9,10 do not clear	Z, C, DC
MOV R, A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A, R	R-A → A	Z, C, DC
SUB R, A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A, R	A ∨ VR → A	Z
OR R, A	A ∨ VR → R	Z
AND A, R	A & R → A	Z
AND R, A	A & R → R	Z
XOR A, R	A ⊕ R → A	Z

Mnemonic	Operation	Status Affected
XOR R, A	$A \oplus R \rightarrow R$	Z
ADD A, R	$A + R \rightarrow A$	Z,C,DC
ADD R, A	$A + R \rightarrow R$	Z,C,DC
MOV A, R	$R \rightarrow A$	Z
MOV R, R	$R \rightarrow R$	Z
COMA R	$/R \rightarrow A$	Z
COM R	$/R \rightarrow R$	Z
INCA R	$R+1 \rightarrow A$	Z
INC R	$R+1 \rightarrow R$	Z
DJZA R	$R-1 \rightarrow A$ , skip if zero	None
DJZ R	$R-1 \rightarrow R$ , skip if zero	None
RRCA R	$R(n) \rightarrow A(n-1)$ $R(0) \rightarrow C$ , $C \rightarrow A(7)$	C
RRC R	$R(n) \rightarrow R(n-1)$ $R(0) \rightarrow C$ , $C \rightarrow R(7)$	C
RLCA R	$R(n) \rightarrow A(n+1)$ $R(7) \rightarrow C$ , $C \rightarrow A(0)$	C
RLC R	$R(n) \rightarrow R(n+1)$ $R(7) \rightarrow C$ , $C \rightarrow R(0)$	C
SWAPA R	$R(0-3) \rightarrow A(4-7)$ $R(4-7) \rightarrow A(0-3)$	None
SWAP R	$R(0-3) \leftrightarrow R(4-7)$	None
JZA R	$R+1 \rightarrow A$ , skip if zero	None
JZ R	$R+1 \rightarrow R$ , skip if zero	None
BC R, b	$0 \rightarrow R(b)$	None
BS R, b	$1 \rightarrow R(b)$	None
JBC R, b	if $R(b)=0$ , skip	None
JBS R, b	if $R(b)=1$ , skip	None
CALL k	$PC+1 \rightarrow [SP]$ , (Page, k) $\rightarrow PC$	None
JMP k	(Page, k) $\rightarrow PC$	None
MOV A, k	$k \rightarrow A$	None
OR A, k	$A \vee k \rightarrow A$	Z
AND A, k	$A \& k \rightarrow A$	Z
XOR A, k	$A \oplus k \rightarrow A$	Z
RETL k	$k \rightarrow A$ , [Top of Stack] $\rightarrow PC$	None
SUB A, k	$k-A \rightarrow A$	Z,C,DC
INT	$PC+1 \rightarrow [SP]$ , 001H $\rightarrow PC$	None
PAGE k	$K \rightarrow R5$	None
ADD A, k	$k+A \rightarrow A$	Z,C,DC

## 5.8 Code Option Register

The IC has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

12	11	10	9	8	7	6	5	4	3	2	1	0
												/POVD

**Bits 12 ~ 1:** Undefined bits, set to "0" at all time

**Bit 0 (/POVD):** Power on voltage detector reset.

0: Enable

1: Disable

The /POVD reset voltage when VDD = 3.3V is as follows.

/POVD	Reset Type	Sleep Mode Current
1	1.6V Power on reset	1 $\mu$ A
0	1.8V /POVD reset	6 $\mu$ A

Note: When /POVD is disabled, the CPU is reset by power on reset circuit. When /POVD is enabled, the CPU is reset by /POVD reset circuit.

## 6 Absolute Maximum Ratings

Items	Rating		
DC Supply Voltage	2.1V	to	3.6V
Input Voltage	$V_{SS} - 0.3V$	to	$V_{DD} + 0.5V$
Operating Temperature Range	- 40°C	to	85°C

**Note:** \*These parameters are theoretical values and have not been tested.

## 7 Electrical Characteristics

### 7.1 DC Characteristics

( $T_A = -40^{\circ}C \sim 85^{\circ}C$ ,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{SS} = 0V$ )

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IIL1	Input Leakage Current for input pins	$V_{IN} = V_{DD}, V_{SS}$	-	-	$\pm 1$	$\mu A$
IIL2	Input Leakage Current for bi-directional pins	$V_{IN} = V_{DD}, V_{SS}$	-	-	$\pm 1$	$\mu A$
VIH	Input High Voltage		2.5	-	-	V
VIL	Input Low Voltage			-	0.8	V
VIHT	Input High Threshold Voltage	/RESET, TCC, RDET1	2.0	-		V
VILT	Input Low Threshold Voltage	/RESET, TCC, RDET1	-	-	0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5	-	-	V
VILX	Clock Input Low Voltage	OSCI	-	-	1.5	V
IOH	Output High Drive Current	$V_{OH} = 2.72V @ V_{DD} = 3.0V$	-	7.5	-	mA
IOL	Output Low Sink Current (Port 6 / 7, P80 and P81)	$V_{OL} = 0.67V$	-	76.5	-	mA
	(Port 5 / 9, P82, and P83)		-	42	-	mA
IPH	Pull-high current	Pull-high active input pin at $V_{SS}$	-	-15	-20	$\mu A$
ISB1	Power down current (Sleep mode, POVD disable)	All input and I/O pin at $V_{DD}$ , output pin floating, WDT disabled	-	1	4	$\mu A$
	Power down current (Sleep mode, POVD enable)		-	5	15	$\mu A$
ISB2	Low clock current (Green mode, POVD disable)	CLK = 32768 Hz, All input and I/O pin at $V_{DD}$ , output pin floating, WDT disabled, other analog Circuits disabled	-	35	50	$\mu A$
	Low clock current (Green mode, POVD enable)		-	45	65	$\mu A$
ISB4	Low clock current (Green mode, POVD disable)	CLK = 32768 Hz, All input and I/O pin at $V_{DD}$ , output pin floating, WDT disabled, other analog Circuits disabled	-	55	75	$\mu A$
	Low clock current (Green mode, POVD enable)		-	65	90	$\mu A$
ICC	Operating supply current (CPU enable)	/RESET = High, CLK = 3.58MHz, Output pin floating, other analog circuits disabled	-	0.48	1.0	mA

**Note:** \*These parameters are theoretical values and have not been tested.

Current D/A ( $T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 5\%$ ,  $V_{SS} = 0\text{V}$ )

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ICC	Max. output current for Current D/A	IOC5 PAGE1 bit0 ~ 3 =1111	3	5	6	mA

## 7.2 AC Characteristics

$T_A = 25^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V}$ ,  $V_{SS} = 0\text{V}$

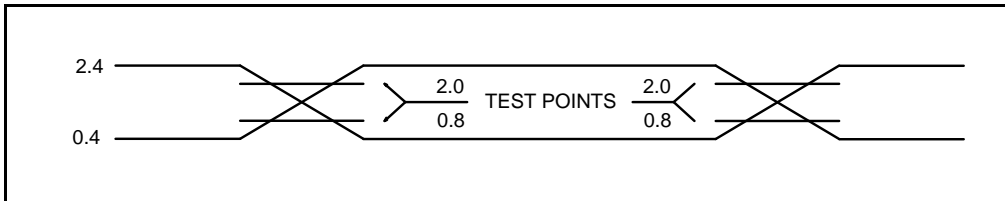
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time	32.768 Hz 3.5826MHz	-	60 550	-	$\mu\text{s}$ ns
Tdrh	Device delay hold time	-	-	18	-	ms
Ttcc	TCC input period	Note 1	(Tins + 20) / N	-	-	ns
Twdt	Watchdog timer period	$T_A = 25^{\circ}\text{C}$	-	18	-	ms
Tdiea	Delay from Phase 3 end to INSEND active	$C1=100\text{pF}$	-	-	30	ns
Tdiei	Delay from Phase 4 end to INSEND inactive	$C1=100\text{pF}$	-	-	30	ns
Tiew	INSEND pulse width	-	30	-	-	ns
Tdca	Delay from Phase 4 end to CA Bus valid	$C1=100\text{pF}$	-	-	30	ns
Tacc	ROM data access time	-	100	-	-	ns
Tcds	ROM data setup time	-	20	-	-	ns
Tcdh	ROM data hold time	-	20	-	-	ns
Tdca-1	Delay time of CA-1	$C1=100\text{pF}$	-	-	30	ns

**Note:** These parameters are theoretical values and have not been tested.

\*N = selected prescaler ratio

## 8 Timing Diagrams

### AC Test Input/Output Waveform



**Note:** AC Testing: Input are driven at 2.4V for Logic "1" and 0.4V for Logic "0"  
Timing measurements are made at 2.0V for Logic "1" and 0.8V for Logic "0"

Figure 8-1a AC Test Input/Output Waveform Timing Diagram

### Reset Timing (CLK = "0")

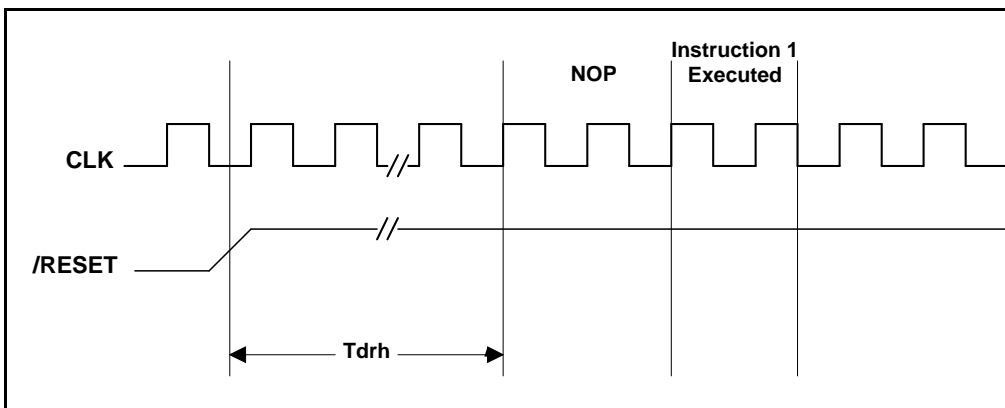


Figure 8-1b Reset Timing Diagram

### TCC Input Timing

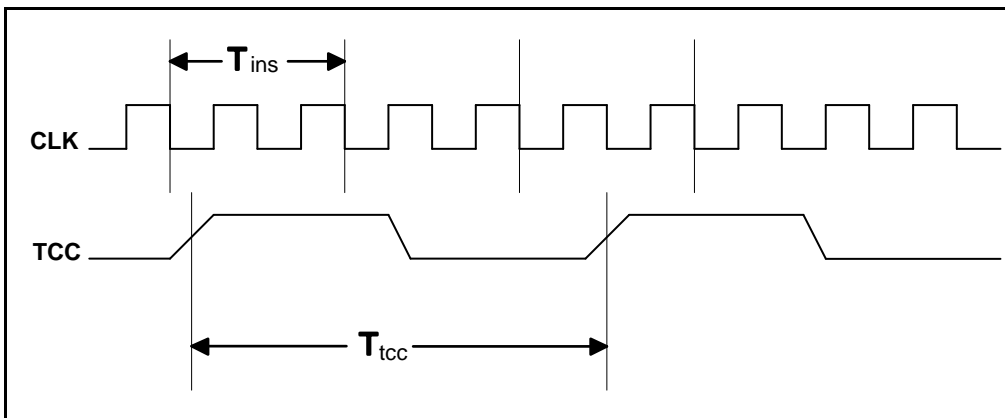


Figure 8-1c TCC Input Timing Diagram