EM78P5840N

8-Bit Microcontrollers

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2006/04/25
1.1	EM78P5841N, EM78P5842N renamed as EM78P5840N. Modified the General Description Section Modified the Features Section Modified the Pin Assignment Section Modified the Block Diagram Section Modified Figure 7-1 Program Counter Organization Modified the Code Option Register Modified Subsection 7.11.2 IRC Mode Modified Subsection 7.11.3 ERIC Mode Modified the Package Type for Green Product and rename Added Figure 7-8 Interrupt Backup Diagram Added Appendix F Quality Assurance and Reliability Deleted Appendix D.2 EM78P5840N Serial Package Type	2008/01/23
1.2	Modified the RESETEN bit for Code Option	2008/04/11
1.3	Modified Subsection 7.2.15 *Interrupt Status Register* Modified Subsection 7.3.2 *Control Register*	2009/08/18
1.4	Modified the names of the Code Option Register and the description in the Appendix.	2011/08/01

1 General Description

The EM78P5840N series are 8-bit RISC architecture microcontroller devices designed and developed with low-power, high-speed CMOS technology. Each of these devices has on-chip 4K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code as well as from unwanted external accesses. A number of one-time programmable option bits are also available to meet user's application requirements.

Functional flexibility of these integrated ICs is enhanced with their internal special features such as Watchdog Timer (WDT), program OTP-ROM, RAM, programmable real-time clock/counter, internal interrupt, power down mode, dual PWM (Pulse Width Modulation), 8-channel 10-bit A/D converter, and tri-state I/O.

NOTE

Refer to the Application Notes provided in the Appendix for important reminders before using the microcontroller described herein.

Convention on tables used to describe register attributes (bit number, bit name, type, etc.), are also provided in the Appendix.

2 Features

- CPU configuration
  - 4K×13 bits on-chip ROM
  - 144×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Less than 2.5 mA at 5V/3.58 MHz
  - Typically 25 μA, at 3V/32kHz (Green)
  - Typically 1 μA, during sleep mode
- I/O port configuration
  - 4 bidirectional I/O ports
  - 5 programmable pull-high I/O pins
  - External interrupt : P70, P71, P73
- Operating voltage range:
  - 2.2V~5.5V at 0°C~70°C (commercial)
  - 2.4V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (base on 2 clocks)
  - Crystal mode: DC ~ 14.3MHz, 3.6V; DC ~ 3.58 MHz, 2.2V
  - RC mode: DC ~ 14 MHz, 3.6V; DC ~ 2 MHz, 2.2V
  - Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C+85°C)	Voltage (2.2V~5.5V)	Process	Total
2 MHz	±5%	±5%	±4%	±14%
4 MHz	±5%	±5%	±4%	±14%

- The two main frequencies can be auto trimmed by ELAN Writer.
- Three operation modes using crystal oscillator (Main clock can be programmed to 3.58 MHz or 14.3 MHz) :
  - Two Normal mode frequency levels: 3.58 MHz and 14.3 MHz.
  - Input port interrupt function
  - Dual-clock operation (Internal PLL main clock, External 32.768kHz)

Mode	CPU Status	Main Clock	32.768kHz Clock Status
Sleep	Off	Off	Off
Green	On	Off	On
Normal	On	On	On

- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt.
  - 8-bit multi-channel Analog-to-Digital Converter with 10-bit resolution

Operating Voltage(V)(min)	3.5	3.0	2.5	2.5
Converter Rate (kHz, max)	74.5	37.4	18.7	9.3

  - Pulse Width Modulation (PWM): Three PWM with 10-bit resolution
  - One 8-bit counter interrupt
  - On-chip Watchdog Timer WDT)
  - Power-down (Sleep, Green) mode
- Five available interrupts
  - TCC overflow interrupt
  - One 8-bit counter interrupt
  - External interrupt
  - ADC completion interrupt
  - PWM period match completion
- Package Types
  - 18-pin DIP 300mil : EM78P5840ND18J/S
  - 18-pin SOP 300mil : EM78P5840NSO18J/S
  - 20-pin DIP 300mil : EM78P5840ND20J/S
  - 20-pin SOP 300mil : EM78P5840NSO20J/S
  - 24 pin DIP 600mil : EM78P5840ND24J/S
  - 24-pin skinny DIP 300mil : EM78P5840NK24J/S
  - 24 pin SOP 300mil : EM78P5840NSO24J/S

Note: *These are all Green Products which do not contain hazardous substances.*

3 Applications

General purpose I/O product applications

A/D applications

4 Pin Assignment

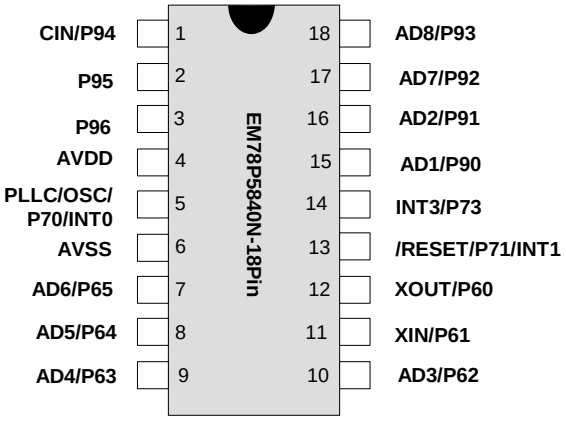


Figure 4-1 EM78P5840ND18/SO18

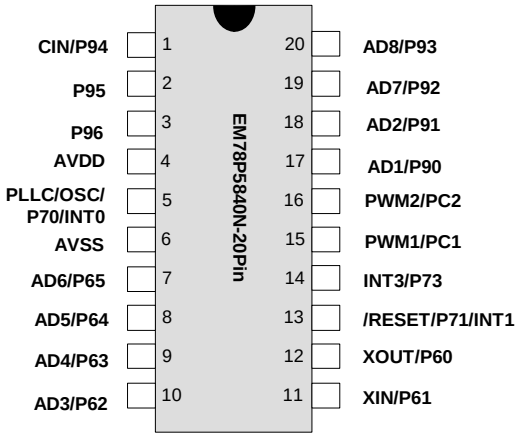


Figure 4-2 EM78P5840ND20/SO20

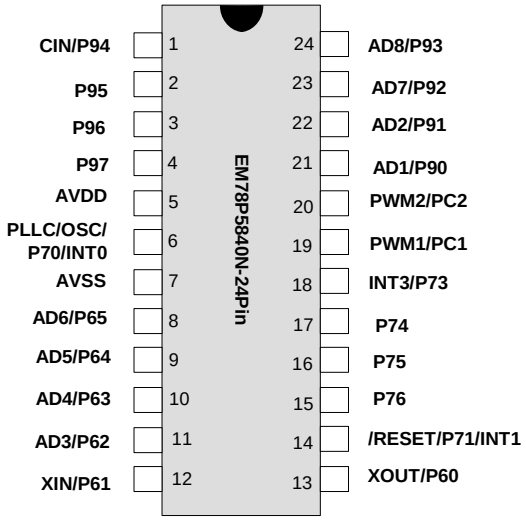


Figure 4-3 EM78P5840ND24/K24/SO24

5 Pin Description

5.1 EM78P5840ND18/SO18

Symbol	Pin No.	Type	Function
AVDD	4	–	Power supply
XIN	11	I	Input pin for the 32.768kHz oscillator
XOUT	12	O	Output pin for the 32.768kHz oscillator
PLLC	5	I	Phase lock loop capacitor. Connect a capacitor (0.047µF to 0.1µF) to ground
OSC	5	I	ERIC mode clock signal input. This pin is shared with PLLC.
CIN	1	I	Counter 1 external CLK input. This pin is shared with P94. Note that the frequency of the input CLK must be less than 1 MHz.
P60 ~ P61	12~11	I/O	General-purpose I/O pin These two pins can be used for ERIC and IRC modes.
P62 ~ P65	10~7	I/O	General-purpose I/O pin
P70	5	I/O	General-purpose I/O pin
P71	13	I	General-purpose I pin
P73	14	I/O	General-purpose I/O pin
P90 ~ P96	15~3	I/O	General-purpose I/O pin
INT0	5	I	External interrupt pin triggered by a falling or a rising edge. Defined by CONT <7>
INT1	13	I	External interrupt pin triggered by a falling edge.
INT3	14	I	External interrupt pin triggered by a falling edge.
AD1~ AD8	15, 16, 10~7, 17, 18	I	Analog-to-Digital Converter
/RESET	13	I	If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET/Vpp must not exceed Vdd during normal mode.
AVSS	6	–	Ground

5.2 EM78P5840ND20/SO20

Symbol	Pin No.	Type	Function
AVDD	4	–	Power supply
XIN	11	I	Input pin for the 32.768kHz oscillator
XOUT	12	O	Output pin for the 32.768kHz oscillator
PLLC	5	I	Phase lock loop capacitor. Connect a capacitor (0.047μF to 0.1μF) to ground
OSC	5	I	ERIC mode clock signal input. This pin is shared with PLLC.
CIN	1	I	Counter 1 external CLK input. This pin is shared with P94. Note that the frequency of the input CLK must be less than 1 MHz.
P60 ~ P61	12~11	I/O	General-purpose I/O pin These two pins can be used for ERIC and IRC modes.
P62 ~ P65	10~7	I/O	General-purpose I/O pin
P70	5	I/O	General-purpose I/O pin
P71	13	I	General-purpose I pin
P73	14	I/O	General-purpose I/O pin
P90 ~ P96	17~20 1~3	I/O	General-purpose I/O pin
PC1 ~ PC2	15, 16	I/O	General-purpose I/O pin
INT0	5	I	External interrupt pin triggered by a falling or a rising edge. Defined by CONT <7>
INT1	13	I	External interrupt pin triggered by a falling edge
PWM1~PWM2	15,16		Pulse width modulation output
AD1~ AD8	17,18, 10~7,19, 20	I	Analog-to-Digital Converter
/RESET	13	I	If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET/Vpp must not exceed Vdd during normal mode.
AVSS	6	–	Ground

5.3 EM78P5840ND24/K24/SO24

Symbol	Pin No.	Type	Function
AVDD	5	–	Power supply
XIN	12	I	Input pin for the 32.768kHz oscillator
XOUT	13	O	Output pin for the 32.768kHz oscillator
PLLC	6	I	Phase lock loop capacitor. Connect a capacitor (0.047μF to 0.1μF) to ground
OSC	6	I	ERIC mode clock signal input. This pin is shared with PLLC.
CIN	1	I	Counter 1 external CLK input. This pin is shared with P94. Note that the frequency of the input CLK must be less than 1 MHz.
P60 ~ P61	13 ~12	I/O	General-purpose I/O pin These two pins can be used for ERIC and IRC modes.
P62 ~ P65	11 ~ 8	I/O	General-purpose I/O pin
P70	6	I/O	General-purpose I/O pin
P71	14	I	General-purpose I pin
P73 ~ P76	18 ~ 15	I/O	General-purpose I/O pin
P90 ~ P97	21~24 1~4	I/O	General-purpose I/O pin
PC1 ~ PC2	19 ~ 20	I/O	General-purpose I/O pin
INT0	6	I	External interrupt pin triggered by a falling or a rising edge. Defined by CONT <7>
INT1	14	I	External interrupt pin triggered by a falling edge.
INT3	18	I	External interrupt pin triggered by a falling edge.
PWM1~PWM2	19 ~ 20		Pulse width modulation output
AD1~ AD8	21, 22 11~8 23, 24	I	Analog-to-Digital Converter
/RESET	14	I	If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET/Vpp must not exceed Vdd during normal mode.
AVSS	7	–	Ground

6 Block Diagram

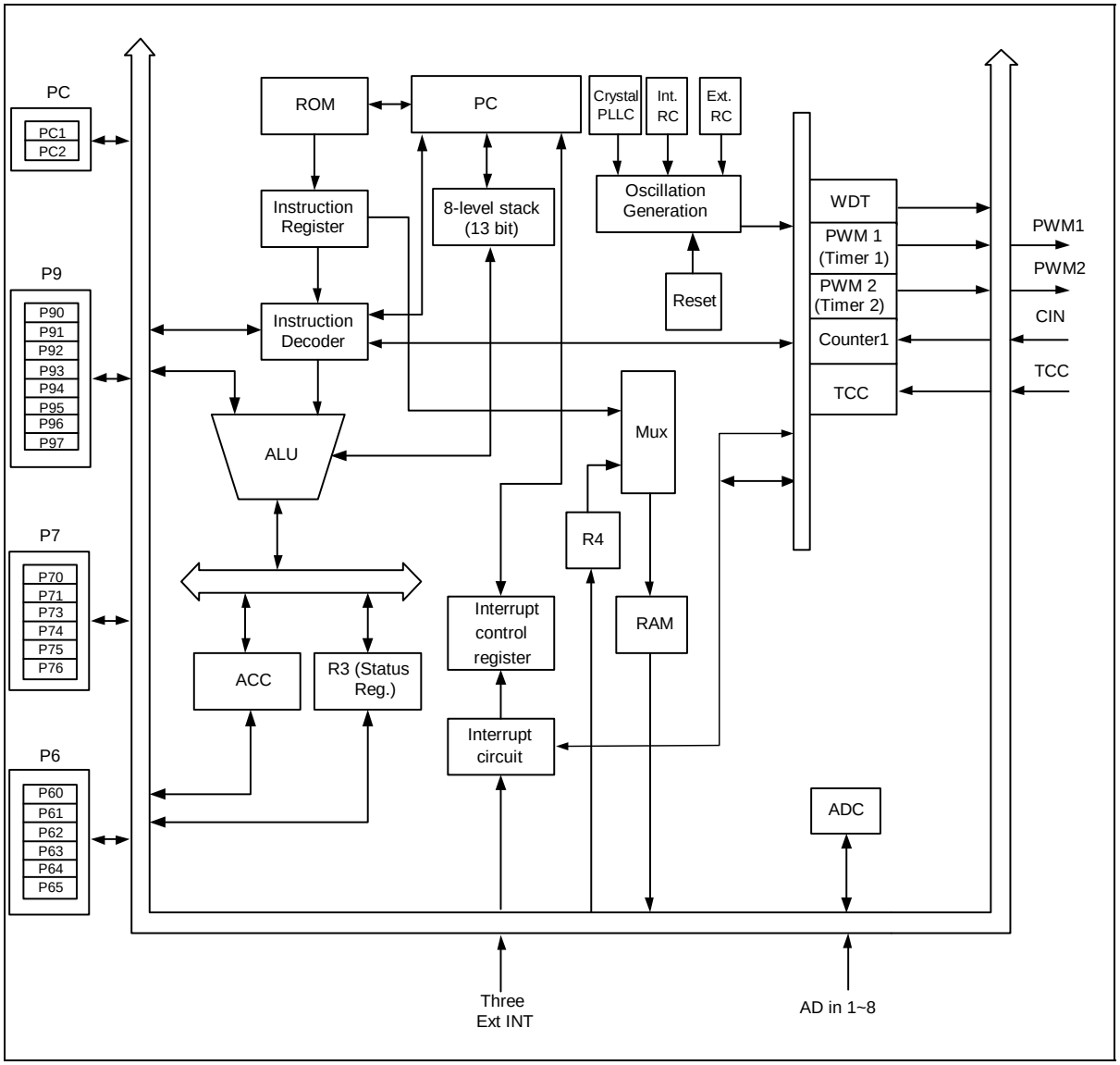


Figure 6 EM78P5840N Block Diagram

7 Functional Description

7.1 Register Configuration

7.1.1 R Page Register Configuration

R Page Registers				
Addr	**R Page 0**	**R Page 1**	**R Page 2**	**R Page 3**
00	Indirect addressing	Reserve	Reserve	Reserve
01	TCC	Reserve	Reserve	Reserve
02	PC	Reserve	Reserve	Reserve
03	Page, Status	Reserve	Reserve	Reserve
04	RAM bank, RSR	Reserve	Reserve	Reserve
05	Program ROM page	Reserve	Reserve	PWM Control
06	Port 6 I/O data	Reserve	Reserve	PWM1 Duty
07	Port 7 I/O data	ADC MSB output data	Reserve	PWM1 Control PWM1 Duty
08	Reserve	Reserve	Reserve	PWM1 Period
09	Port 9 I/O data	Reserve	Reserve	PWM2 Duty
0A	PLL, Main clock, WDTE	Reserve	Reserve	PWM2 Control PWM2 Duty
0B	Reserve	ADC output data buffer	Reserve	PWM2 Period
0C	Port C I/O data	Counter 1 data	Reserve	Reserve
0D	Reserve	Reserve	Reserve	Reserve
0E	Interrupt flag	Reserve	Reserve	Reserve
0F	Interrupt flag	Reserve	Reserve	Reserve
10 : 1F	16 bytes Common registers			
20 : 3F	Bank 0 Common registers 32x8 for each bank	Bank 1 Common registers 32x8 for each bank	Bank 2 Common registers 32x8 for each bank	Bank 3 Common registers 32x8 for each bank

Addresses 00~0F with Page 0~Page 3 are special registers. Addresses 10~1F are global with general purpose memory. Use the MOV instruction to set the MCU to read data from or write data to these registers directly. This will ignore the RAM bank select bits (RB1, RB0 in R4 Page 0). Addresses 20~3F are general purpose RAM, but the bank number must be indicated before accessing data.

7.1.2 IOC Page Register Configuration

IOC Page Registers		
Addr	**IOC Page 0**	**IOC Page 1**
00	Reserve	Reserve
01	Reserve	Reserve
02	Reserve	Reserve
03	Reserve	Reserve
04	Reserve	Reserve
05	Reserve	Reserve
06	Port 6 I/O control	Port 6 switches
07	Port 7 I/O control	Port 7 pull high
08	Reserve	Reserve
09	Port 9 I/O control	Reserve
0A	Reserve	Port 9 switches
0B	Reserve	ADC control
0C	Reserve	Reserve
0D	Reserve	Clock source (CN1) Prescaler (CN1)
0E	Interrupt mask	Reserve
0F	Interrupt mask	Reserve

The IOC registers are special registers. User can use the “IOW” instruction to write data and the “IOR” instruction to read data.

7.2 Register Operations

7.2.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov  A, @0x20   ; store an address at R4 for indirect addressing
Mov  0x04, A
Mov  A, @0xAA   ; write data 0xAA to R20 at Bank0 through R0
Mov  0x00, A
```

7.2.2 R1 (TCC)

The TCC data buffer is Increased by 16.384kHz or by the instruction clock cycle (controlled by the CONT register). It is written and read by the program as with any other register.

7.2.3 R2 (Program Counter)

The R2 structure is depicted in the Figure 7-1 below. The configuration structure generates 4K×13 external ROM addresses to the corresponding program instruction codes.

The "JMP" instruction allows direct loading of the low 10 program counter bits.

The "CALL" instruction loads the low 10 bits of the PC, PC+1, and then pushes the data onto the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2, A" allows the loading of an address from the A register to the PC, and the contents of the ninth and tenth bits are cleared to "0."

"ADD R2,A" allows a relative address to be added to the current PC, and the contents of the ninth and tenth bits are cleared to "0."

"TBL" allows a relative address to be added to the current PC, and the contents of the ninth and tenth bits don't change. The most significant bit (A10~A11) will be loaded with the contents of bits PS0~PS1 in the status register (R5 Page 0) upon execution of a "JMP", "CALL", "ADD R2, A", or "MOV R2, A" instruction.

If an interrupt is triggered, the program ROM will jump to Address 0x08 at Page 0. The CPU will automatically store the ACC, the status of R3, and R5 Page; and they will be restored after instruction RETI.

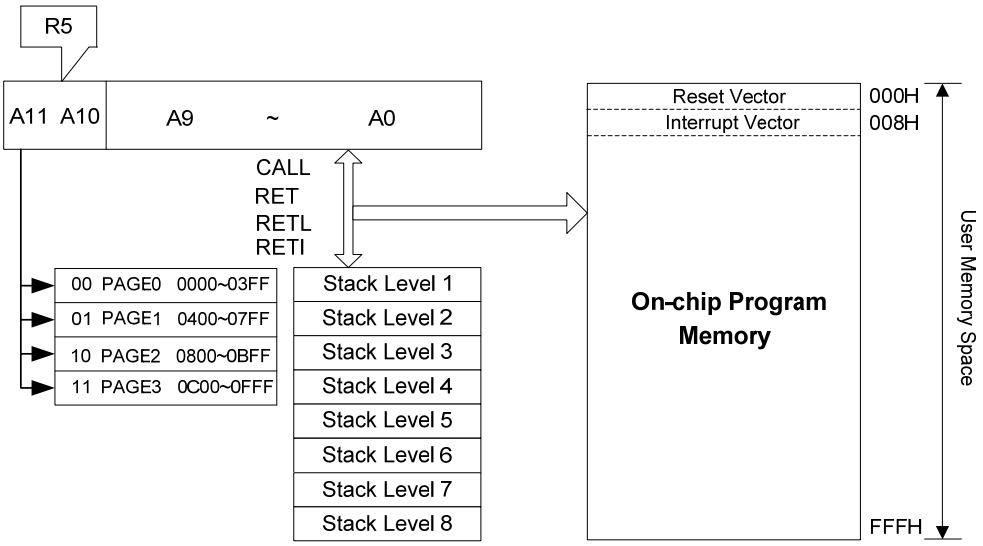


Figure 7-1 Program Counter Organization

7.2.4 R3 (Status, Page Select)

■ (Status Flag, Page Selection Bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RPAGE1	RPAGE0	IOCPAGE	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R	R	R/W	R/W	R/W

Bit 0 (C): Carry flag

Bit 1(DC): Auxiliary carry flag

Bit 2 (Z): Zero flag

Bit 3 (P): Power down bit

Set to “1” during power on or by a "WDTC" command and reset to “0” by a "SLEP" command.

Bit 4 (T): Time-out bit

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

Event	T	P	Remarks
WDT wakes up from sleep mode	0	0	
WDT times out (not in sleep mode)	0	1	
/RESET wakes up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	×	×	× = don't care

Bit 5 (IOCPAGE): Change IOC pages between Page 0 and Page 1

"**0**" : IOC Page 0

"**1**" : IOC Page 1

See Section 7.1.2 "*IOC Page Register Configuration"* for further details.

Bits 6~7 (RPAGE0 ~ RPAGE1): Change R pages between Page 0 ~ Page 3

(RPAGE1, RPAGE0)	R Page # Selected
(0, 0)	R Page 0
(0, 1)	R Page 1
(1, 0)	R Page 2
(1, 1)	R Page 3

Refer to Section 7.1.1 "*R Page Register Configuration"* for further details.

7.2.5 R4 (RAM Select for Common Registers R20 ~ R3F)

■ **(RAM Select Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 5 (RSR0 ~ RSR5): Indirect addressing for common Registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1): Bank select bits for common Registers R20 ~ R3F

These select bits are used to determine which bank is activated among the four banks for the 32 registers (R20 to R3F).

Refer to Section 7.1.1 "*R Page Register Configuration*" for further details.

7.2.6 R5 (Program Page Select, PWM Control)

■ **Page 0 (Port 5 I/O Data Register, Program Page Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	0	0	PS1	PS0
-	-	-	-	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 1 (PS0 ~ PS1): Program page selection bits

PS1	PS0	Program Memory Page (Address)
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

The PAGE instruction can be used to maintain the program page.

Bit 2 ~ Bit 3 (Undefined): These two bits must be set to "0." Otherwise, the MCU will access an incorrect program code.

Bit 4 ~ Bit 7 (Undefined): not used

■ **Page 3 (PWMCON)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 1 (T1P0 ~ T1P1): TMR1 clock prescaler option bits

T1P1	T1P0	Prescaler
0	0	1:2 (Default)
0	1	1:8
1	0	1:32
1	1	1:64

Bit 2 ~ Bit 3 (T2P0 ~ T2P1): TMR2 clock prescaler option bits

T2P1	T2P0	Prescaler
0	0	1:2 (Default)
0	1	1:8
1	0	1:32
1	1	1:64

Bit 4 (T1EN): TMR1 enable bit

"**0**" : TMR1 is off (default value)

"**1**" : TMR1 is on

Bit 5 (T2EN): TMR2 enable bit

"**0**" : TMR2 is off (default value)

"**1**" : TMR2 is on

Bit 6 (PWM1E): PWM1 enable bit

"**0**" : PWM1 is off (default value), and the corresponding pin carries out the PC1 function

"**1**" : PWM1 is on, and the corresponding pin will be automatically set as output pin

Bit 7 (PWM2E): PWM2 enable bit

"**0**" : PWM2 is off (default value), and the corresponding pin carries out the PC2 function

"**1**" : PWM2 is on, and the corresponding pin will be automatically set as output pin

7.2.7 R6 (Port 6 I/O Data, PWM Control)

■ **Page 0 (Port 6 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P65	P64	P63	P62	P61	P60
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 1 (P60 ~ P61): Ports 60 ~ 61 are used in IRC and ERIC modes. In these modes, Ports 60 ~ 61 are defined as General Purpose I/O. In Crystal mode, Ports 60 ~ 61 are defined as crystal input (XIN and XOUT) pins.

Bit 2 ~ Bit 6 (P62 ~ P65): 4-bit Port 6 I/O data register. The IOC register can be used to set each bit as input or output.

Bit 6 ~ Bit 7 (undefined): These bits are not used

■ **Page 3 (DT1L: The Least Significant Byte (Bits 0 ~ 7) of PWM1 Duty Cycle)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1[7]	PWM1[6]	PWM1[5]	PWM1[4]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

A specified value keeps the output of PWM1 to remain at high until such value matches the value of TMR1.

7.2.8 R7 (Port 7 I/O Data, ADC, PWM Duty Cycle)

■ **Page 0 (Port 7 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	P76	P75	P74	P73	-	P71	P70
-	R/W	R/W	R/W	R/W	-	R	R/W

Bit 0 (P70): Port 70 is a multi-function pin. In Crystal mode, set PLLEN in code option to define Port 70 as a general purpose I/O or PLLC. Do not enable the PLL function if Port 70 is defined as an I/O. In IRC or ERIC mode, this pin (Port 70) is defined as general purpose I/O and PLLEN will be ignored. P70 is Port 70 I/O data register and the IOC7 register can be used to set each bit either as input or output.

Bit 1 (P71): Port 71 is shared with the /RESET pin. Set the code option for RESETEN and define Port 71 as an input pin or /RESET pin. This register is a read-only bit. P71 does not does not have an internal pull high function. If you want to use the interrupt at P71, external pull-high is necessary.

Bit 2 and Bit 7 (Undefined): These bits are not used.

Bit 3 ~ Bit 6 (P73 ~ P76): 4-bit Port 7 I/O data register. The IOC register can be used to set each bit either as input or output.

■ **Page 1 (ADC Resolution Select Bit and ADC MSB Output Data)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	AD9	AD8	-	ADRES	0	0
-	-	R	R	-	R/W-0	R-0	R-0

Bit 0 ~ Bit 1 (undefined): These two bits are not used. However, these bits must be cleared to "0" to avoid possible error.

Bit 2 (ADRES): Resolution selection for ADC

"**0**" : ADC is 8-bit resolution. When 8-bit resolution is selected, the most significant (MSB) 8-bit data output of the internal 10-bit ADC will be latched and mapped to RB PAGE1 only (see Section 7.2.12). Hence, R7 PAGE1 Bits 4 ~5 are not implemented.

"**1**" : ADC is 10-bit resolution. When 10-bit resolution is selected, the 10-bit data output of the internal 10-bit ADC will be mapped to RB PAGE1 (see Section 7.2.12), plus R7 PAGE1 Bits 4 ~5 to meet the 10 bits requirement.

Bit 3 (Undefined): This bit is not used.

Bit 4 ~ Bit 5 (AD8 ~ AD9): The most significant 2 bits of the 10-bit ADC conversion output data. Combine these two bits with the RB PAGE1 into a complete 10-bit ADC conversion output data.

Bit 6 ~ Bit 7 (Undefined): These bits are not used.

■ **Page 3 (DT1H: Most Significant Byte (Bit 0 ~ Bit 1) of PWM1 Duty Cycle)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	PWM1[9]	PWM1[8]
R-0	R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0

Bit 0 ~ Bit 1 (PWM1[8] ~ PWM1[9]): Most Significant two bits of PWM1 Duty Cycle

Bit 2 ~ Bit 7 (Undefined): These bits are not used. However, these bits must be cleared to "0" to avoid possible error.

7.2.9 R8 (PWM1 Period)

■ **Page 3 (PRD1: PWM1 Period)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

The contents of this register is PWM1 time base period. The PWM1 frequency is the inverse of the time base period.

7.2.10 R9 (Port 9 I/O Data, DT2L)

■ **Page 0 (Port 9 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P90 ~ P97): 8-bit Port 9 (0~7) I/O data register. The IOC register can be used to set each bit either as input or output.

■ **Page 3 (DT2L: Least Significant Byte (Bit 0 ~ Bit 7) of PWM2 Duty Cycle)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2[7]	PWM2[6]	PWM2[5]	PWM2[4]	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

A specified value keeps the PWM2 output to remain high until it matches with the value of TMR2.

7.2.11 RA (PLL, Main Clock Selection, Watchdog Timer, DT2H)

■ **Page 0 (PLL Enable Bit, Main Clock Selection Bits, Watchdog Timer Enable Bit)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PLLEN	CLK2	CLK1	CLK0	-	-	WDTEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	-	-	R/W-0

Bit 0 (WDTEN): Watchdog control bit

"**0**" : Disable watchdog

"**1**" : Enable watchdog

The WDTC instruction can be used to clear the watchdog counter. The watchdog counter is a free-running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in Sleep mode). During normal operation or Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during Green mode or Normal mode. Without the presacler, the WDT time-out period is approximately 18 ms.

Bit 1 ~ Bit 2 (Undefined): These bits are not used.

Bit 3 ~ Bit 5 (CLK0 ~ CLK2): Main clock select bits in Crystal mode. These three bits are NOT used in IRC and ERIC mode.

■ **In Crystal Mode:**

Different frequencies for the main clock can be chosen with the CLK0, CLK1 and CLK2 bits. All available clock selections are listed below**:**

PLLEN	CLK2	CLK1	CLK0	Sub Clock	Main Clock	CPU Clock
1	0	0	0	32.768kHz	3.582 MHz	3.582 MHz (Normal mode)
1	0	0	1	32.768kHz	3.582 MHz	3.582 MHz (Normal mode)
1	0	1	0	32.768kHz	3.582 MHz	3.582 MHz (Normal mode)
1	0	1	1	32.768kHz	3.582 MHz	3.582 MHz (Normal mode)
1	1	0	0	32.768kHz	14.3 MHz	14.3 MHz (Normal mode)
1	1	0	1	32.768kHz	14.3 MHz	14.3 MHz (Normal mode)
1	1	1	0	32.768kHz	14.3 MHz	14.3 MHz (Normal mode)
1	1	1	1	32.768kHz	14.3 MHz	14.3 MHz (Normal mode)
0	don't care	don't care	don't care	32.768kHz	don't care	32.768kHz (Green mode)

Bit 6 (PLLEN): PLL's power control bit is the CPU mode control register. This bit is only used in Crystal mode. In RC mode, this bit will be ignored.

"**0**" : Disable PLL

"**1**" : Enable PLL

If PLL is enabled, the CPU will operate in Normal mode (high frequency). Otherwise, it will run in Green mode (low frequency, 32768 Hz).

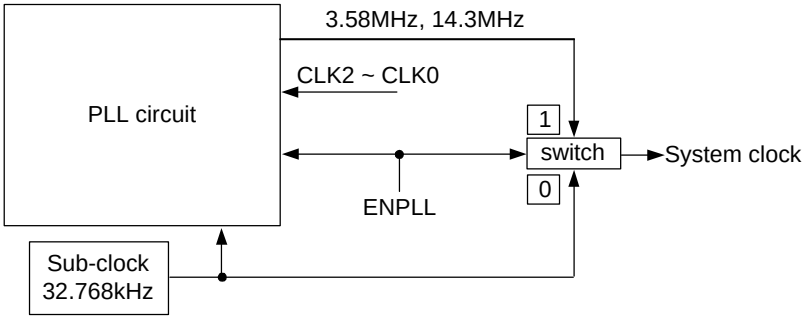


Figure 7-2 Correlation between 32.768kHz and PLL

Bit 7 (Undefined): This bit is not used. However, always keep this bit at "0" to preclude possible error.

When Bit 7and Bit 6 are set to “0” and are included in the SLEP instruction, the following table shows the status after wake up and the wake-up sources.

Wake-up Signal	Sleep Mode
-	RA(7,6)=(0,0) + SLEP
TCC time out IOCF Bit 0 =1	No effect
Counter 1 time out IOCF Bit 1=1	No effect
WDT time out	Reset and jump to Address 0
Port 7 (0, 1, 3)*	Reset and Jump to Address 0

* Port 70 wake-up function is controlled by IOCF Bit 3. It is a falling edge or rising edge trigger (controlled by CONT register Bit 7).

Port 71 wake-up function is controlled by IOCF Bit 4. It is a falling edge trigger.

Port 73 wake-up function is controlled by IOCF Bit 7. It is a falling edge trigger.

■ **Page 3 DT2H: Most Significant Bit (Bit 1 ~ Bit 0) of PWM2 Duty Cycle**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PWM2[9]	PWM2[8]
-	-	-	-	-	-	R/W-0	R/W-0

Bit 0 ~ Bit 1 (PWM2[8] ~ PWM2[9]): Most Significant bit of PWM2 Duty Cycle
A specified value keeps the PWM2 output to remain high until it matches with the value of TMR2.

Bit 2 ~ Bit 7 (Undefined): These bits are not used.

7.2.12 RB (ADC Input Data Buffer)

■ **Page 1 (ADC Output Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (AD0 ~ AD7): The last significant 8 bits of the 10-bit or the 8-bit resolution ADC conversion output data. Combine these 8 bits with the R7 PAGE1 Bit 4 ~ Bit 5 (see Section 7.2.8) to have a complete 10-bit ADC conversion output data in 10-bit resolution mode.

■ **Page 3 (PRD2: PWM2 Period)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (PRD2[0] ~ PRD2[7]): All the contents of this register are PWM2 time-base period. The PWM2 frequency is the inverse of the period.

7.2.13 RC (Port C I/O Data, Counter 1 Data)

■ **Page 0 (Port 9 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PC2	PC1	-
-	-	-	-	-	R/W	R/W	-

Bit 0 (undefined): This bit is not used.

Bit 1 ~ Bit 2 (PC1 ~ PC2): Port C1, Port C2 I/O data register

The IOC register can be used to define each bit either as input or output.

Bit 3 ~ Bit 7 (Undefined): These bits are not used.

■ **Page 1 (Counter 1 Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN10 ~ CN17): Counter 1 buffer that's readable and writable. Counter 1 is an 8-bit up-counter with 8-bit prescaler that allows the device to preset (write → preset) and read the counter by using RC PAGE1. After an interrupt, the preset value will be reloaded.

Examples of Write and Read Instructions:

```
MOV  0x0C, A   ; write the data at accumulator to Counter 1 (preset)
MOV  A, 0x0C   ; read & move the data at Counter 1 to accumulator
```

7.2.14 RE (Interrupt Flag)

■ **Page 0 (Interrupt Flag)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2	0	ADI	PWM1	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (Undefined): Not used. However, these four bits must be cleared to "0" to prevent possible error.

Bit 4 (PWM1): One PWM1 (Pulse Width Modulation Channel 1) period upon reaching the interrupt flag.

Bit 5 (ADI): ADC interrupt flag after each sampling

Bit 6 (undefined): This bit must be cleared to "0." Otherwise, errors may occur.

Bit 7 (PWM2): PWM2 (Pulse Width Modulation Channel 2) interrupt flag

Set when a selected period is reached, reset by software.

7.2.15 RF (Interrupt Status)

■ **Interrupt Status Register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT3	-	-	INT1	INT0	-	CNT1	TCIF
R/W-0	-	-	R/W-0	R/W-0	-	R/W-0	R/W-0

Bit 0 (TCIF): TCC timer overflow interrupt flag. Set when TCC timer overflows.

"**0**" : No Interrupt request. Hence no interrupt occurs.

"**1**" : With Interrupt request

Bit 1 (CNT1): Counter 1 timer overflow interrupt flag. Set when Counter 1 timer overflows.

"**0**" : No Interrupt request. Hence no interrupt occurs.

"**1**" : With Interrupt request

Bit 2 (Undefined): This bit is not used.

Bit 3 (INT0): By setting Port 70 to general IO, INT0 will become Port 70 pin's interrupt flag. If Port 70 has a falling edge/rising edge (controlled by the CONT register) trigger signal, the CPU will set this bit. If the pin is set to PLLC or OSCI, no interrupt will occur at Port 70 and INT0 register will be ignored.

"**0**" : No Interrupt request. Hence no interrupt occurs.

"**1**" : With Interrupt request

Bit 4 (INT1): By setting Port 71 to general I/O, INT1 will become Port 71 pin's interrupt flag. External pull-high circuit is needed to trigger an interrupt at Port 71. If Port 71 has a falling edge trigger signal, the CPU will set this bit. If the pin is set to /RESET, no interrupt will occur at Port 71 and INT1 register will be ignored.

"**0**" : No Interrupt request. Hence no interrupt occurs.

"**1**" : With Interrupt request

Bit 5 ~ Bit 6 (Undefined): These bits are not used.

Bit 7 (INT3): External Port 73 pin interrupt flag. If Port 73 has a falling edge trigger signal (see table below), the CPU will set this bit.

"**0**" : No Interrupt request. Hence no interrupt occurs.

"**1**" : With Interrupt request

NOTE

IOCF is the interrupt mask register which can be read and cleared.

The following shows the trigger edge signals.

Signal	Trigger
TCC	Time out
Counter 1	Time out
INT0	Falling / Rising edge
INT1	Falling edge
INT3	Falling edge

7.2.16 R10~R3F (General Purpose Register)

- **R10~ R1F**
- **R20~R3F (Banks 0 ~ 3)**

These are all general purpose registers.

7.3 Special Function Registers

7.3.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

7.3.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P70EG	INT	TS	RETBK	PAB	PSR2	PSR1	PSR0
R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Note: *The CONT register is readable (CONTR) and writable (CONTW).*

Bit 0 ~ Bit 2 (PSR0 ~ PSR2): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Ratio	WDT Ratio
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB): Prescaler assigned bit

"**0**" : TCC

"**1**" : WDT

Bit 4 (RETBK): Return the backed-up control value for the interrupt routine

"**0**" : Disable

"**1**" : Enable

When this bit is set to “1”, the CPU will automatically store the ACC, R3 status, and R5 PAGE after an interrupt is triggered. This bit will be restored after the RETI instruction. When this bit is set to “0”, user needs to store the ACC, R3 status, and R5 PAGE in the program.

Bit 5 (TS): TCC signal source

"**0**" : Internal instruction clock cycle

"**1**" : IRC output

Bit 6 (INT): INT enable flag

"**0**" : Interrupt masked by DISI or hardware interrupt

"**1**" : Interrupt enabled by ENI/RETI instructions

Bit 7 (P70EG): If Port 70 is set to INT0 input, P70EG can select the interrupt toggle type.

"**0**" : P70 's interrupt source is a rising edge signal

"**1**" : P70 's interrupt source is a falling edge signal

■ TCC and WDT

An 8-bit counter is available as the prescaler for the TCC or WDT. The prescaler is available for either TCC or WDT at a time. Availability of the 8-bit counter for TCC or WDT is contingent on the status of Bit 3 (PAB) of the CONT register as shown above.

See the prescaler ratio for TCC/WDT in the table above. Figure 7-3 depicts the block diagram of TCC/WDT.

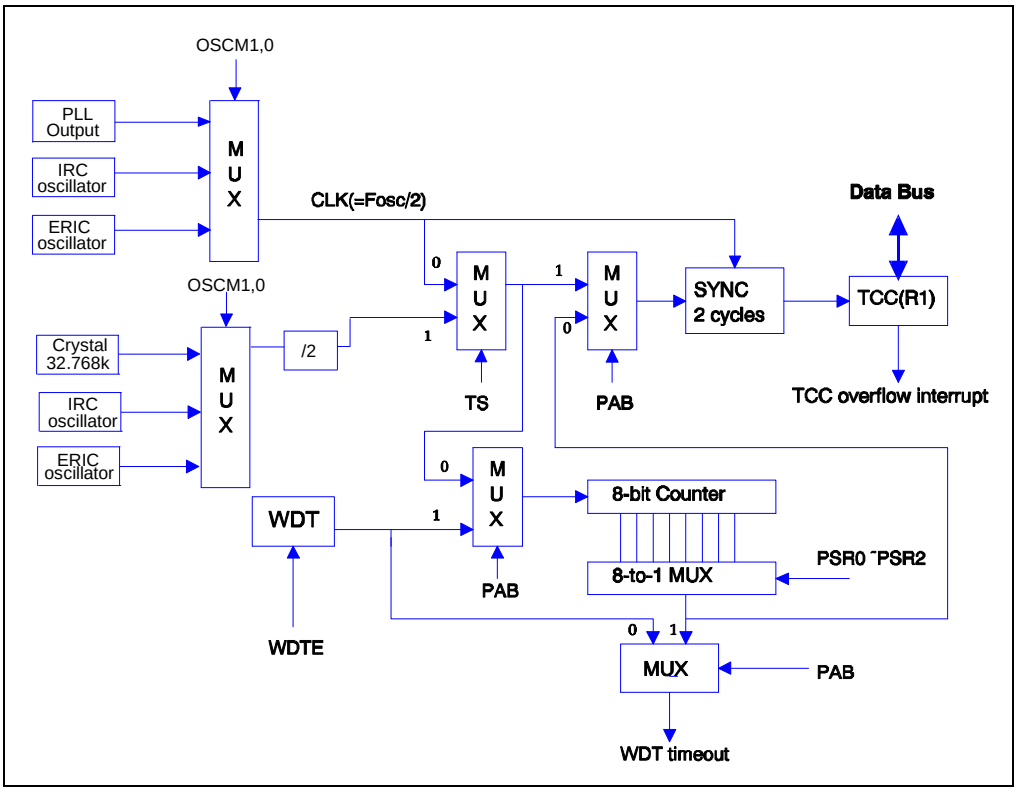


Figure 7-3 TCC/WDT Block Diagram

7.3.3 IOC6 (Port 6 I/O Control, P6 Pin Switch Control)

■ **Page 0 (Port 6 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
-	-	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 1 (IOC60 ~ IOC61): In IRC or ERIC mode, Port 60 and Port 61 are I/O direction control registers. In Crystal mode, these two bits are unused.

Bit 2 ~ Bit 5 (IOC62 ~ IOC65): Port 62 ~ Port 65 I/O direction control register

"**0**" : Set the corresponding I/O pin as output

"**1**" : Set the corresponding I/O pin to high impedance

Bit 6 ~ Bit 7 (Undefined): These bits are not used. However, these two bits must be cleared to "0." Otherwise, the MCU power consumption will increase.

NOTE

The default value of these bits are "1." Clear them to "0" when initializing the MCU.

■ **Page 1 (Port 6 Pins Switch Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	0	P65S	P64S	P63S	P62S	P91S	P90S
-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (P90S): Select normal I/O Port 90 pin or ADC Channel 1 input AD1 pin

"**0**" : P90 (I/O Port 90) pin is selected

"**1**" : AD1 (ADC Channel 1 input) pin is selected

Bit 1 (P91S): Select normal I/O Port 91 pin or Channel 2 input AD2 pin of ADC

"**0**" : P91 (I/O Port 91) pin is selected

"**1**" : AD2 (ADC Channel 2 input) pin is selected

Bit 2 (P62S): Select normal I/O Port 62 pin or Channel 3 input AD3 pin of ADC

"**0**" : P62 (I/O Port 62) pin is selected

"**1**" : AD3 (ADC Channel 3 input) pin is selected

Bit 3 (P63S): Select normal I/O Port 63 pin or Channel 4 input AD4 pin of ADC

"**0**" : P63 (I/O Port 63) pin is selected

"**1**" : AD4 (ADC Channel 4 input) pin is selected

Bit 4 (P64S): Select normal I/O Port 64 pin or Channel 5 input AD5 pin of ADC

"**0**" : P64 (I/O Port 64) pin is selected

"**1**" : AD5 (ADC Channel 5 input) pin is selected

Bit 5 (P65S): Select normal I/O Port 65 pin or Channel 6 input AD6 pin of ADC

"**0**" : P65 (I/O Port 65) pin is selected

"**1**" : AD5 (ADC Channel 6 input) pin is selected

Bit 6 (Undefined): This bit is not used. However, it must be cleared to "0" to prevent possible error from occuring.

Bit 7 (Undefined): This bit is not used

NOTE

1. ADC Channel 1 and Channel 2 are shared with Port 90 and Port 91.
2. ADC Channel 3 and Channel 6 are shared with Port 62 and Port 65.

7.3.4 IOC7 (Port 7 I/O Control, Port 7 Pull-high Control)

■ **Page 0 (Port 7 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	IOC76	IOC75	IOC74	IOC73	0	0	IOC70
-	R/W-1	R/W-1	R/W-1	R/W-1	-	-	R/W-1

Bit 0 (IOC70): Port 70 pin is defined as general purpose I/O, PLLC, or OSC through code option setting. In IRC mode or Crystal mode (only at code option PLLEN =0), Port 70 pin is a general purpose I/O, while IOC70 is I/O direction control register of Port 70 pin.

"**0**" : Set the corresponding I/O pin as output

"**1**" : Set the corresponding I/O pin to high impedance

Bit 1 (Undefined): This bit is not used. However, by setting RESETEN = 1 by Code Option, Port 71 pin will become an input-only pin.

Bit 2 (Undefined): This bit is not used but must be cleared to "0." Otherwise, the MCU power consumption will increase.

NOTE

The default value of this bit is "1." Clear to "0" when initializing the MCU.

Bit 3 ~ Bit 6 (IOC73~IOC76): Port 7 I/O direction control register

"**0**" : Set the corresponding I/O pin as output

"**1**" : Set the corresponding I/O pin to high impedance

Bit 7 (Undefined): This bit is not used but must be cleared to "0." Otherwise, the MCU power consumption will increase.

> **NOTE**
> *The default value of this bit is "1." Clear to "0" when initializing the MCU.*

■ **Page 1 (Port 7 Pull-high Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PH76	PH75	PH74	PH73	0	0	PH70
-	R/W-0	R/W-0	R/W-0	R/W-0	-	-	R/W-0

Bit 0 (PH70): Port 70 pull-high control register. This bit only exists when you set Port 70 as a general purpose I/O.

"**0**" : disable pull-high function

"**1**" : enable pull-high function

Bits 1 ~ 2 and Bit 7 (Undefined): These bits are not used but must be cleared to "0." Otherwise, the MCU power consumption will increase.

Bit 3 ~ Bit 6 (PH73 ~ PH76): Port 7 pull-high control register

"**0**" : disable pull-high function

"**1**" : enable pull-high function

7.3.5 IOC9 (Port 9 I/O Control, Port 9 Switches)

■ **Page 0 (Port 9 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97): Port 9 (0~7) I/O direction control register

"**0**" : Set the corresponding I/O pin as output

"**1**" : Set the corresponding I/O pin to high impedance

7.3.6 IOCA (Port 9 PMS Switch Control)

■ **Page 1 (Port 9 Pin Switch Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	0	-	-	0	-	AD8S	AD7S
-	R/W	-	-	R/W	-	R/W-0	R/W-0

Bit 0 (AD7S): Select normal I/O Port 92 pin or ADC Channel 7 input AD7 pin

"**0**" : P92 (I/O Port 92) pin is selected

"**1**" : AD7 (ADC Channel 7 input) pin is selected

Bit 1 (AD8S) : Select normal I/O Port 93 pin or ADC Channel 8 input AD8 pin

"**0**" : P93 (I/O Port 93) pin is selected

"**1**" : AD8 (ADC Channel 8 input) pin is selected

Bit 2 (Undefined): This bit is not used

Bit 3 (Undefined): This bit is not used. However, it must be cleared to "0." Otherwise, the MCU power consumption will increase.

Bit 4 ~ Bit 5 (Undefined): These bits are not used.

Bit 6 (Undefined): This bit is not used. However, this bit must be cleared to "0." Otherwise, the MCU power consumption will increase.

Bit 7 (Undefined): This bit is not used.

7.3.7 IOCB (ADC Control)

■ **Page 1 (ADC Control Bits)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN2	IN1	IN0	ADCLK1	ADCLK0	ADPWR	0	ADST
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	-	R/W-0

Bit 0 (ADST): Start sampling at the AD converter

By setting this bit to "1", the AD will start to sample data. This bit will be cleared by hardware automatically after each sampling.

Bit 1 (Undefined): This bit is not used. However, it must be cleared to "0" to preclude possible error.

Bit 2 (ADPWR): AD converter power control

"**0**" : disable

"**1**" : enable

Bit 3 ~ Bit 4 (ADCLK0 ~ ADCLK1): AD circuit's sampling clock source.

In Crystal mode:

ADCLK1	ADCLK0	Sampling Rate	Operating Voltage
0	0	74.6K	≥ 3.5V
0	1	37.4K	≥ 3.0V
1	0	18.7K	≥ 2.5V
1	1	9.3K	≥ 2.5V

In IRC or ERIC mode:

In these modes, the AD converter rate is set by the oscillator. The formula for the input frequency and the AD converter rate is:

$$\textbf{\textit{AD Coverter Rate}} = \frac{Oscillator / 4}{\left(2^{ADCLK}\right) / 12}$$

For example, if input CLK = 4 MHz

ADCLK1	ADCLK0	Sampling Rate	Operation Voltage
0	0	83.3K	≥ 3.5V
0	1	41.7K	≥ 3.0V
1	0	20.8K	≥ 2.5V
1	1	10.4K	≥ 2.5V

Note: *The AD converter (ADC) rate must not be over 50kHz. Otherwise, the ADC resolution will decrease.*

This is a CMOS multi-channel 10-bit successive approximation of the A/D converter. Its features are as follows**:**

- 74.6kHz maximum conversion speed (Crystal mode) at 5V
- Adjustable full scale input
- Internal (VDD) reference voltage
- Eight analog inputs multiplexed into one AD converter
- Power-down mode for power saving
- Complete AD conversion interrupt
- Interrupt register, AD control, and status register, and AD data register

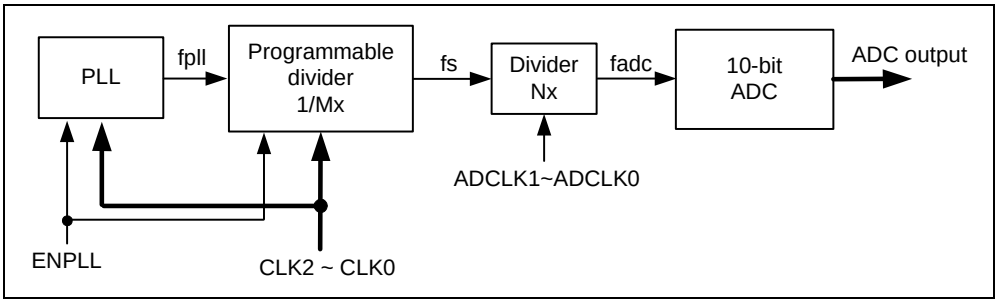


Figure 7-4 ADC Voltage Control Logic

Bit 5 ~ Bit 7 (IN0~ IN2) : Input channel selection of the AD converter. These two bits can choose one of the following three AD inputs.

IN2	IN1	IN0	Input	Pin
0	0	0	AD1	P90
0	0	1	AD2	P91
0	1	0	AD3	P62
0	1	1	AD4	P63
1	0	0	AD5	P64
1	0	1	AD6	P65
1	1	0	AD7	P92
1	1	1	AD8	P93

NOTE

Before switching to the AD channel, the corresponding pin must be set as an AD input.

7.3.8 IOCC (Port C I/O Control, ADC Control)

■ **Page 0 (Port C I/O Control)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	IOCC2	IOCC1	0
-	-	-	-	-	R/W-1	R/W-1	-

Bit 0 (Undefined): This bit is not used. However, it must be cleared to "0." Otherwise, the MCU power consumption will increase.

Bit 1 ~ Bit 2 (IOCC1 ~ IOCC2): Port C (1~2) I/O direction control register

"**0**" : Set the corresponding I/O pin as output

"**1**" : Set the corresponding I/O pin to high impedance

Bit 3 ~ Bit 7 (Undefined): These bits are not used. However, they must be cleared to "0." Otherwise, the MCU power consumption will increase.

NOTE

The default value of Bit 0 and Bits 3~7 is "1." Clear to "0" when initializing the MCU.

7.3.9 IOCD (Tone 1 Control, Clock Source, CN1 Prescaler)

■ **Page 1 (Clock Source and Counter 1 Prescaler)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNTI/ES	-	-	-	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	-	-	-	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C1_PSC0 ~ C1_PSC2): Counter 1 prescaler ratio

C1_PSC2	C1_PSC1	C1_PSC0	Counter 1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S): Counter 1 clock source. This bit will be unchanged in RC mode (RC mode CLK is always equal to the oscillator's frequency).

"**0**" : 16.384kHz

"**1**" : System clock

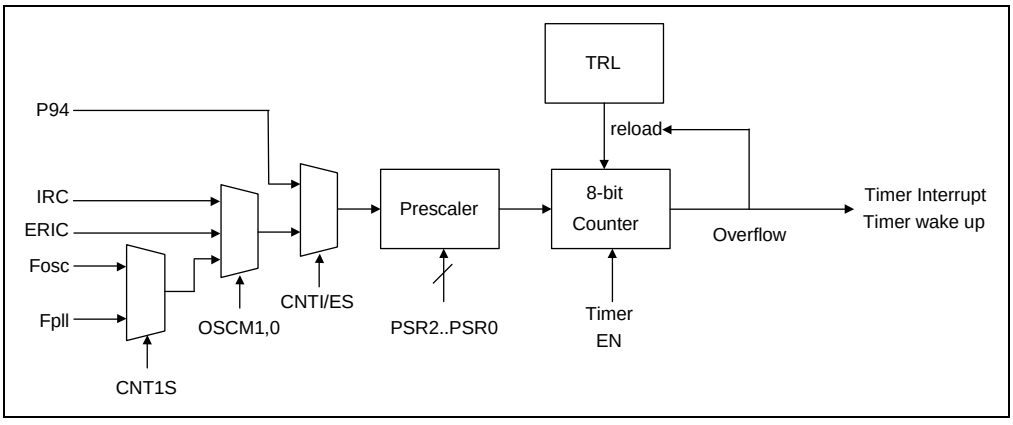


Figure 7-5 Timer CLK Source Diagram

Bit 4 ~ Bit 6 (Undefined): These bits are not used.

Bit 7 (CNTI/ES): Counter source select

"**0**" : Timer counter CLK is sourced from the system CLK or Crystal output, and P94 is set as a general purpose I/O

"**1**" : P94 is defined as input, and the Timer counter CLK is sourced from P94's falling edge

7.3.10 IOCE (Interrupt Mask)

■ **Page 0 (Interrupt Mask)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2	0	ADI	PWM1	-	-	-	-
R/W-0	-	R/W-0	R/W-0	-	-	-	-

Bit 0 ~ Bit 3 (Undefined): These bits are not used.

Bit 4 (PWM1) : One PWM1 one period for each interrupt mask.

Bit 5 (ADI) : ADC conversion complete interrupt mask

"**0**" : Disable interrupt

"**1**" : Enable interrupt

There are four registers for the AD converter. Use one bit of the interrupt control register (IOCE Page 0 Bit 5) to signal an interrupt when the AD conversion is completed. The status and control register of AD (IOCB Page 1 and RE Page 0 Bit 5) indicate the A/D conversion status or AD control. The AD data register (RB PAGE1) stores the result of the AD conversion.

The ADI bit can be enabled or disabled in the IOCE PAGE 0 register to signal the completion of the A/D conversion. The ADI flag is then enabled or disabled in the RE register when AD conversion is completed. The ADI flag indicates the end of an AD conversion. The AD converter sets the interrupt flag (ADI) in the RE Page 0 register when a conversion is completed. The interrupt can be disabled by setting the ADI bit in IOCE Page 0 Bit 5 to “0.”

The AD converter has eight analog input channels (AD1 ~ AD8) multiplexed into one sample and hold to AD module. The reference voltage can be driven from the internal power. The AD converter itself is a 10-bit successive approximation type and produces the last significant 8-bit result in the RB Page 1 and the most significant 2 bits to R7 Page 1 Bit 4, Bit 5. A conversion is initiated by setting the control bit ADST in IOCB Page 1 Bit 0.. Prior to conversion, the appropriate channel must be selected by setting IN0 ~ IN2 bits in the RE register. Enough time must be allowed to sample data. Every AD data conversion needs 12-clock cycle time. The minimum conversion time required is 13 µs (73K sample rate). The ADST Bit in IOCB Page 1 Bit 0 must be set to begin a conversion.

It will be automatically reset in the hardware when a conversion is completed. At the end of the conversion, the Start bit is cleared and the the AD interrupt is activated if ADI in IOCE Page 0 Bit 5 = 1. ADI will be set when the conversion is completed. It can be reset by software.

If ADI = 0 in IOCE Page 0 Bit 5 and AD starts data conversion by setting ADST(IOCB Page 1 Bit 0) = 1, then AD will continue the conversion non-stop and the hardware will not reset the ADST bit. In this condition, ADI is deactivated. After ADI in IOCE Page 0 Bit 5 is set, ADI in RE Page 0 Bit 5 will be activated again.

To minimize the operating current, all biasing circuits in the A/D module that consume DC current, are powered down when the ADPWR bit in IOCB Page 1 Bit 2 register is ”0”. When ADPWR bit is ”1,” the A/D converter module is operating.

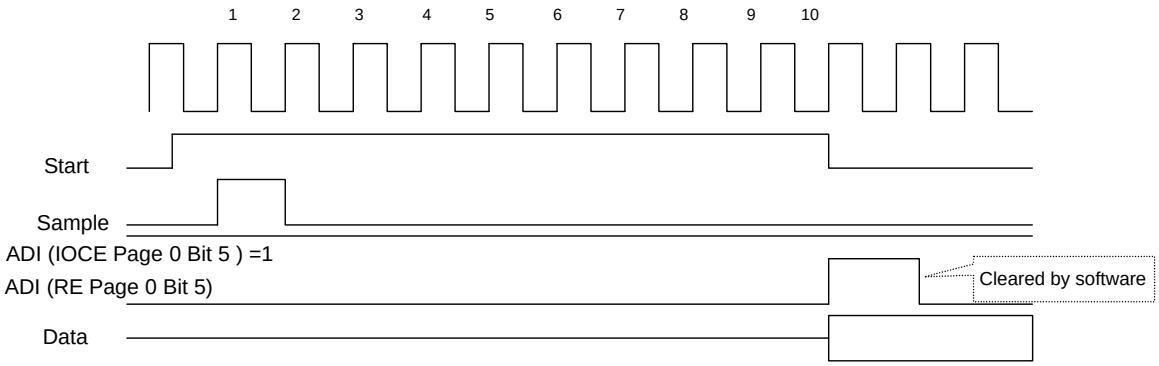


Figure 7-6 A/D Converter Timing

Bit 6 (Undefined): This bit is not used. However, you must clear this bit to “0” to avoid any possible error.

Bit 7 (PWM2) : PWM2 interrupt enable bit

"**0**" : Disable interrupt

"**1**" : Enable interrupt

7.3.11 IOCF (Interrupt Mask)

■ **Page 0 (Interrupt Mask Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT3	0	0	INT1	INT0	0	CNT1	TCIF
R/W-0	-	-	R/W-0	R/W-0	-	R/W-0	R/W-0

Bit 0 ~ Bit 1 (TCIF ~ CNT1): Interrupt enable bits

"**0**" : Disable interrupt

"**1**" : Enable interrupt

Bit 2 (Undefined): This bit is not used. However, this bit must be cleared to “0” to avoid unpredicted interrupts to occur.

Bit 3 ~ Bit 4 (INT0 ~ INT1): Interrupt enable bits

"**0**" : Disable interrupt

"**1**" : Enable interrupt

Bit 5 ~ Bit 6 (Undefined): These bits are not used. However, these bits must be cleared to "0" to avoid unpredicted interrupts to occur.

Bit 7 (INT3): Interrupt enable bit

"**0**" : Disable interrupt

"**1**" : Enable interrupt

The following table shows the interrupt sources and the resulting status after an interrupt.

Interrupt Signal		Sleep Mode	Green Mode	Normal Mode
TCC time out IOCF Bit 0=1 And "ENI"	ENI	RESET and Jump to Address 0	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
	DISI	No function	No function	No function
Counter 1 time out IOCF Bit 1=1 And "ENI"		No function	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
Port 70[1] Only at IRC mode or Crystal mode (at PLLEN = 0)		RESET and Jump to Address 0	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
Port 71[2] Only at RESETEN = 1		RESET and Jump to Address 0	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
Port 73[3] IOCF Bit 3 Bit 7 =1 And "ENI"		RESET and Jump to Address 0	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page0)
ADI[4] IOCE Bit 5 = 1 And "ENI		No function	No function	Interrupt (Jump to Address 8 at Page 0)
PWM1 IOCE Bit 4 = 1 And "ENI		No function	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)

[1] *Port 70 interrupt function is controlled by IOCF Bit 3. It is a falling edge or rising edge trigger (controlled by CONT register Bit 7).*

[2] *Port 71 interrupt function is controlled by IOCF Bit 4. It is a falling edge trigger.*

[3] *Port 73 interrupt function is controlled by IOCF Bit 7. It is a falling edge trigger.*

[4] *ADI interrupt source function is controlled by RE Page 0 Bit 5. It is a rising edge trigger after an ADC sampling is completed.*

7.4 Instruction Set

The Instruction set has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Convention:

"R" = *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*
Bits 6 and 7 in R4 determine the selected register bank.

"b" = *Bit field designator that selects the value for the bit located in register "R" and which affects the operation.*

"k" = *8 or 10-bit constant or literal value*

Binary Instruction	Hex	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A →R2 Bits 9,10, do not clear	Z, C, DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1

Binary Instruction	Hex	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC	1
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1
0 0100 11rr rrrr	04rr	COM R	/R → R	Z	1[1]
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z	1[1]
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z	1
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skipped
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skipped
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skipped
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skipped
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None	1
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None	1
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skipped
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skipped
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None	1
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z	1
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC	1
1 1110 0000 0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1 1110 100k kkkk	1E8k	PAGE k	K–>R5(4:0)	None	1
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC	1[1]

[1] *One Instruction cycle = Two main CLK*

7.5 Code Option Register

Word 0											
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2 ~ Bit 0**
Mnemonic	C3	C2	C1	C0	RESETEN	PLLEN	OSC1	OSC0	RCM	-	Protect
1	High	High	High	High	P71	PLLC	High	High	4MHz	-	Disable
0	Low	Low	Low	Low	/RESET	P70	Low	Low	2MHz	-	Enable

Bits 12, 11, 10, and Bit 9 (C3, C2, C1, C0): Calibrator of internal RC mode

C3, C2, C1, and C0 must be set to "1" only (auto-calibration).

Bit 8 (RESETEN): /RESET/71 pin select bit

0 : P71 set to /RESET pin

1 : P71 is general purpose input pin (default)

Bit 7 (PLLEN): PLLC/P70 pin select bit.

Bit 6 ~ Bit 5 (OSC1 ~ OSC0): Oscillator Modes Select bits.

Mode	OSC1	OSC0	PLLEN
IRC (Internal RC oscillator mode); PLLC/OSC/P70/INT0 act as P70	0	0	×
ERIC (External R, Internal C oscillator mode) ; PLLC/OSC/P70/INT0 act as OSC. User must cascade the resistor to AVDD	0	1	×
Crystal (Crystal oscillator mode) ; PLLC/OSC/P70/INT0 act as P70	1	×	0
Crystal (Crystal oscillator mode) ; PLLC/OSC/P70/INT0 act as PLLC. PLLC output, user must cascade the capacitor to AVSS **(default)**	1	×	1

Bit 4 (RCM): IRC mode select bit

0 : 2 MHz

1 : 4 MHz

Bit 3: Not used, but need to be cleared to "0" all the time to avoid possible error.

Bit 2 ~ Bit 0 (Protect 2 ~ Protect 0): Protect bits

Protect 2 ~ Protect 0 are protect bits. Protect types are as follows:

Protect 2	Protect 1	Protect 0	Protect
0	0	0	Enable
1	1	1	Disable

7.6 I/O Port

7.6.1 I/O Structure

The I/O registers are bidirectional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O data registers and I/O control registers are both readable and writable. The I/O ports and control registers circuits are illustrated below.

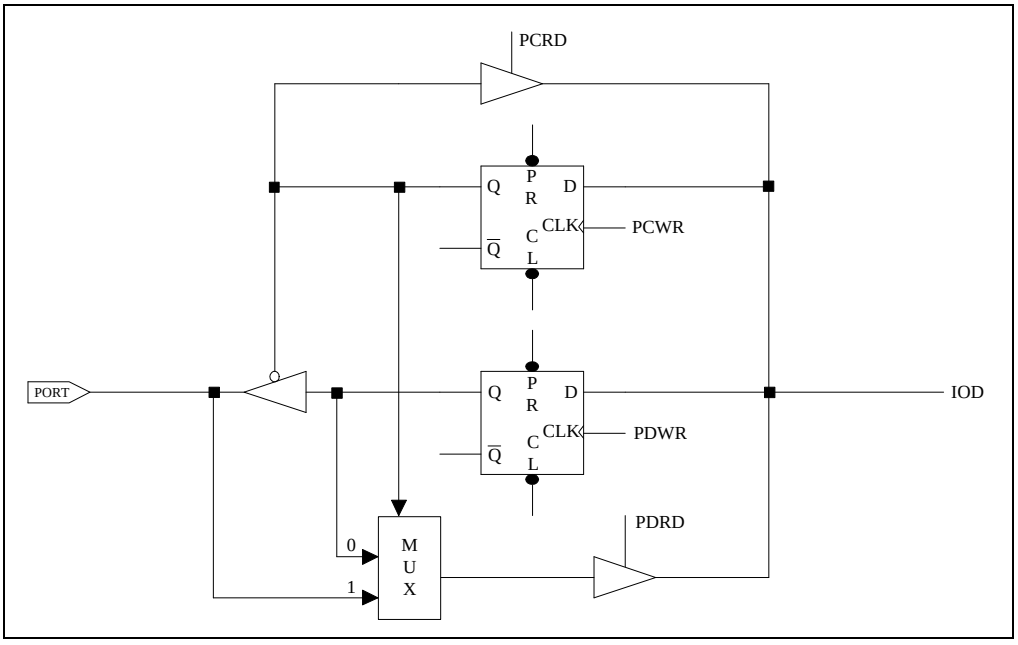


Figure 7-7a I/O Port and I/O Control Register Circuit

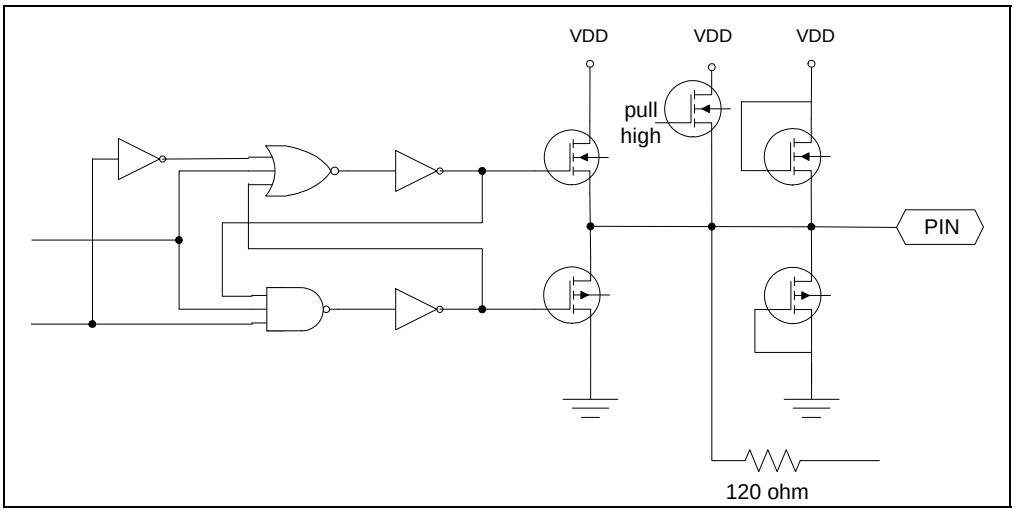


Figure 7-7b EM785840N/41N/42N Input/output Ports Circuit

7.6.2 I/O Description

■ **Port 6**

Pin	P65	P64	P63	P62	P61	P60
Register	R65, Page 0	R64, Page 0	R63, Page 0	R62, Page 0	R61, Page 0	R60, Page 0
I/O	I/O	I/O	I/O	I/O	I/O	I/O
I/O Control	IOC65, Page 0	IOC64, Page 0	IOC63, Page 0	IOC62, Page 0	IOC61, Page 0	IOC60, Page 0
Pin-shared with	AD6	AD5	AD3	AD3	Xin	Xout

Port 60 ~ Port 61: Used in IRC and ERIC mode

In these two modes, Port 60 and Port 61 are defined as general purpose I/O.

In Crystal mode, Port 60 and Port 61 are defined as crystal input (Xin and Xout) pins and R60, R61 bits are undefined.

Port 62 ~ Port 65: Port 6 (2~5) I/O pins

The IOC register can be used to define each pin as input or output.

IOC60 ~ IOC61: Unused registers in Crystal mode

In IRC or ERIC mode, these bits are I/O direction control register.

■ **Port 7**

Pin	P76	P75	P74	P73	P71	P70
Register	R76, Page 0	R75, Page 0	R74, Page 0	R73, Page 0	R71, Page 0	R70, Page 0
I/O	I/O	I/O	I/O	I/O	Input only	I/O
I/O control	IOC76, Page 0	IOC75, Page 0	IOC74, Page 0	IOC73, Page 0	×	IOC70, Page 0
Pull-high	IOC76, Page 1	IOC75, Page 1	IOC74, Page 1	IOC73, Page 1	×	IOC70, Page 1
Pin-shared with	-	-	-	INT3	Reset/INT0	PLLC/ERIC /INT0

Port 70: Multi-function pin

In Crystal mode, by setting PLLEN in code option, Port 70 will be set as general purpose I/O or PLLC.

NOTE

Do not enable the PLL function if Port 70 is defined as I/O.

In IRC or ERIC mode, this pin is defined as Port 70, and PLLEN will be ignored. R70, Page 0 is a Port 70 I/O data register. The IOC register can be used to define each bit as input or output.

Port 71: is shared with /RESET pin.

By setting RESETEN in code option, Port 71 is defined as input pin or /RESET pin. This is an input only pin. P71 does not support internal pull-high function. If you want to use P71 interrupt, external pull-high is necessary.

Port 73 ~ Port 76: Port 7 I/O pins

The IOC register can be used to define each bit either as input or output.

IOC70, Page 1: is Port 70 pull-high control register.

This bit only exist when Port 70 is set as general purpose I/O.

■ **Port 9**

Pin	P97	P96	P95	P94	P93	P92	P91	P90
Register	R97, Page 0	R96, Page 0	R95, Page 0	R94, Page 0	R93, Page 0	R92, Page 0	R91, Page 0	R90, Page 0
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
I/O Control	IOC96, Page 0	IOC96, Page 0	IOC95, Page 0	IOC94, Page 0	IOC93, Page 0	IOC92, Page 0	IOC91, Page 0	IOC90, Page 0
Shared with	-	-	-	CIN	AD1	AD1	AD1	AD1

P90 ~ P97: Port 9 I/O pins

The IOC register can be used to define each bit as input or output.

■ **Port C**

Pin	PC2	PC1
Register	RC1, Page0	RC1, Page0
	I/O	I/O
I/O control	IOCC2, Page0	IOCC1, Page0
Shared with	PWM2	PWM1

PC1~PC2: Port C I/O pins

The IOC register can be used to define each bit as input or output.

7.7 Reset

A Reset is initiated by one of the following conditions:

- Power-on reset
- WDT timeout (if enabled and in Green or Normal mode)
- The Reset pin is pulled low (at RESETEN = 0)

Once a Reset occurs, the following functions are immediatley performed:

- The oscillator continues to run, or will be started (if not already running)
- The Program Counter (R2) is set to all "0"
- When powered on, the upper three bits of R3 and the upper two bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.

7.8 Wake-up

The controller provides a Sleep mode function to conserve power consumption by –

Sleep mode, RA(7) = 0 + "SLEP" instruction

In Sleep mode, the controller turns off all the CPU and crystal. Other power control circuits can also be turned off, i.e., key tone control or PLL control (which has an enable register) by software.

Wake-up is triggered from Sleep mode through one of the following conditions:

- WDT Time-out
- External interrupt
- /RESET pull low

All of the above will reset the controller and run the program at Address 0. The result is the same as that with power-on reset.

The following table lists the wake-up sources and the resulting status after wake-up:

Wake-up Signal	Sleep Mode
-	RA (7, 6)=(0, 0) + SLEP
TCC Time-out IOCF Bit 0=1	No function
Counter 1 Time out IOCF Bit 1=1	No function
WDT Time out	Reset and Jump to Address 0
Port 7 (0, 1, 3)*	Reset and Jump to Address 0

***Port 70** *wake-up function is controlled by IOCF Bit 3. It is a falling edge or rising edge trigger (controlled by CONT Register Bit 7).*

Port 71 *wake-up function is controlled by IOCF Bit 4. It is a falling edge trigger.*

Port 73 *wake-up function is controlled by IOCF Bit 7. It is a falling edge trigger.*

7.9 Interrupt

RF is the interrupt status register that records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) is generated, it will prompt the next instruction to be fetched from Address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared through software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

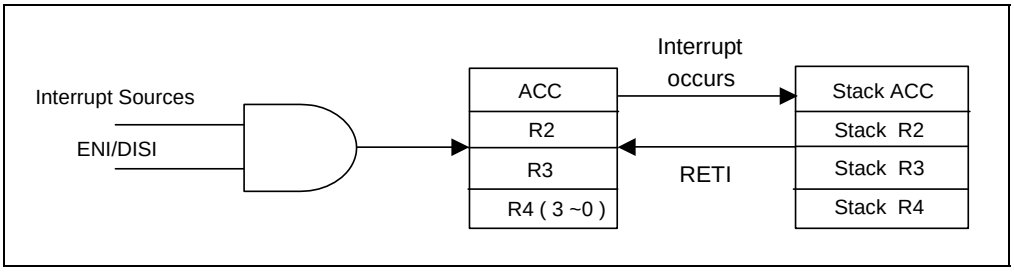


Figure 7-8 Interrupt Backup Diagram

7.10 PWM (Pulse Width Modulation)

7.10.1 Overview

In PWM mode, both PWM1 and PWM2 pins produce up to 10-bit resolution PWM output (see Figure 7-9a below for its functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output in high. The baud rate of the PWM is the inverse of the period. Figure 6-8b below illustrates the relationships between a period and a duty cycle.

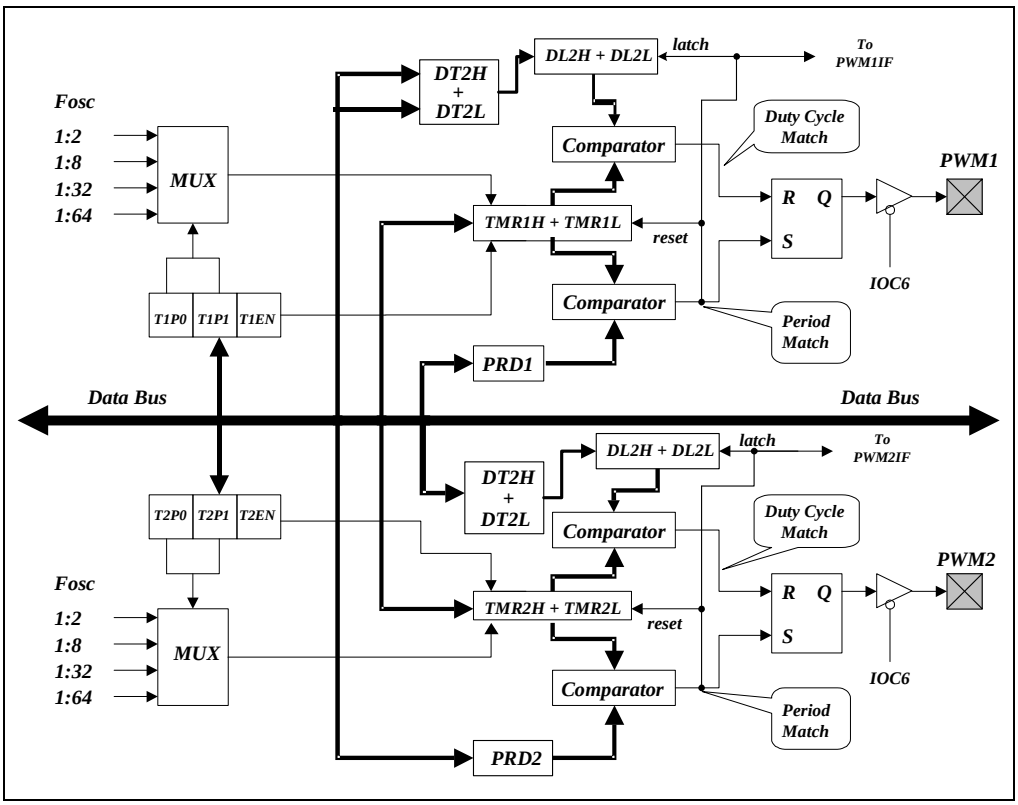


Figure 7-9a Dual PWM Functional Block Diagram

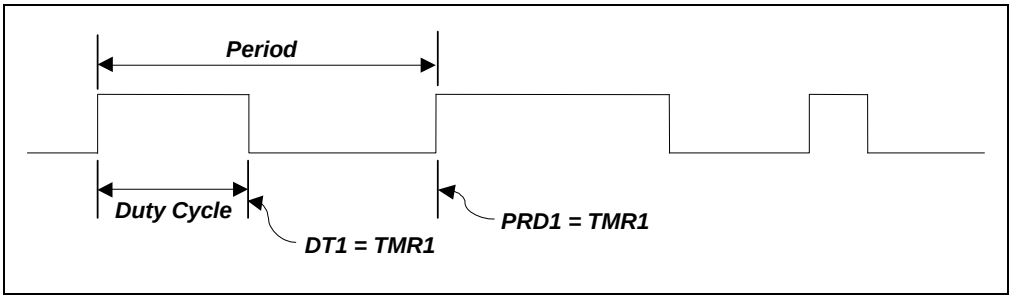


Figure 7-9b PWM Output Timing

7.10.2 Relative Register Description

■ **R5, Page 3 (PWMCON)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

Bit 0 ~ Bit 1 (T1P0 ~ T1P1): TMR1 clock prescaler option bits

T1P1	T1P0	Prescaler
0	0	1:2 (Default)
0	1	1:8
1	0	1:32
1	1	1:64

Bit 2 ~ Bit 3 (T2P0 ~ T2P1): TMR2 clock prescaler option bits

T1P1	T1P0	Prescaler
0	0	1:2 (Default)
0	1	1:8
1	0	1:32
1	1	1:64

Bit 4 (T1EN): TMR1 enable bit

"**0**" : TMR1 is off (default value)

"**1**" : TMR1 is on

Bit 5 (T2EN): TMR2 enable bit

"**0**" : TMR2 is off (default value)

"**1**" : TMR2 is on

Bit 6 (PWM1E): PWM1 enable bit

"**0**" : WM1 is off (default value), and its related pin carries out the PC1 function

"**1**" : PWM1 is on, and its related pin is automatically set as output

Bit 7 (PWM2E): PWM2 enable bit

"**0**" : PWM2 is off (default value), and its related pin carries out the PC2 function

"**1**" : PWM2 is on, and its related pin is automatically set as output

■ **R6 and R7, Page 3 (DT1: Duty Cycle of PWM1)**

R71	R70	R67	R66	R65	R64	R63	R62	R61	R60
PWM1[9]	PWM1[8]	PWM1[7]	PWM1[6]	PWM1[5]	PWM1[4]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]

A specified value keeps the PWM1 output to remain high until the value matches with TMR1.

■ **R9 and RA, Page 3 (DT2: PWM2 Duty Cycle)**

RA1	RA0	R97	R96	R95	R94	R93	R92	R91	R90
PWM2[9]	PWM2[8]	PWM2[7]	PWM2[6]	PWM2[5]	PWM2[4]	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]

A specified value keeps the PWM2 output to remain high until the value matches with TMR2.

■ **R8, Page 3 (PRD1: PWM1 Period)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]

This register contains the PWM1 time-base period. The PWM1 frequency is the inverse of the time-base period.

■ **RB, Page 3 (PRD2: PWM2 Period)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]

This register contains the PWM2 time-base period. The PWM2 frequency is the inverse of the time-base period.

7.10.3 Increment Timer Counter (TMRX: TMR1H/TMR1L or TMR2H/TMR2L)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written to, and cleared at any reset conditions. If enabled, the rates can be reduced to conserve power by setting the T1EN bit to “0”.

7.10.4 PWM Period (PRDX: PRD1 or PRD2)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following operations are performed on the next increment cycle:

- TMRX is cleared
- The PWMX pin is set to “1”
- The PWM duty cycle is latched from DT1/DT2 to DTL1/DTL2

NOTE
The PWM output will not be set if the duty cycle is 0.

- The PWMXIF pin is set to 1

The following formula is used to calculate the PWM period:

$$\textbf{\textit{Period}} = (PRDX + 1) \times 4 \times \left(\frac{1}{F_{OSC}} \right) \times \textit{(TMRX} \times \textit{Prescale value)}$$

Where Fosc is the system clock.

7.10.5 PWM Duty Cycle (DTX: DT1H/ DT1L; DTL: DL1H/DL1L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded any time. However, it cannot be latched into DTL until the current value of DLX is equal to TMRX.

The following formula is used to calculate the PWM duty cycle:

$$\textbf{\textit{Duty Cycle}} = (DTX) \times \left(\frac{1}{F_{OSC}} \right) \times \textit{(TMRX} \times \textit{Prescale value)}$$

7.10.6 PWM Programming Procedure/Steps

Follow these steps in loading PRDX with the PWM period:

1) Load DTX with the PWM duty cycle

2) Enable interrupt function by writing to IOCF PAFE0, if required

3) Set the PWMX pin as output by writing a desired value to IOCC Page 0

Load a desired value to R5 Page 3 with the TMRX prescaler value and enable both PWMX and TMRX.

7.10.7 Timer (TMRX)

The TMRX, consisting of Timer 1 (TMR1) and Timer 2 (TMR2), are 10-bit clock counters with programmable prescalers. This is designed for the PWM module to be set as baud rate clock generators. TMRX can be read, written to, and cleared at any reset condition.

The following figure shows the TMRX block diagram.

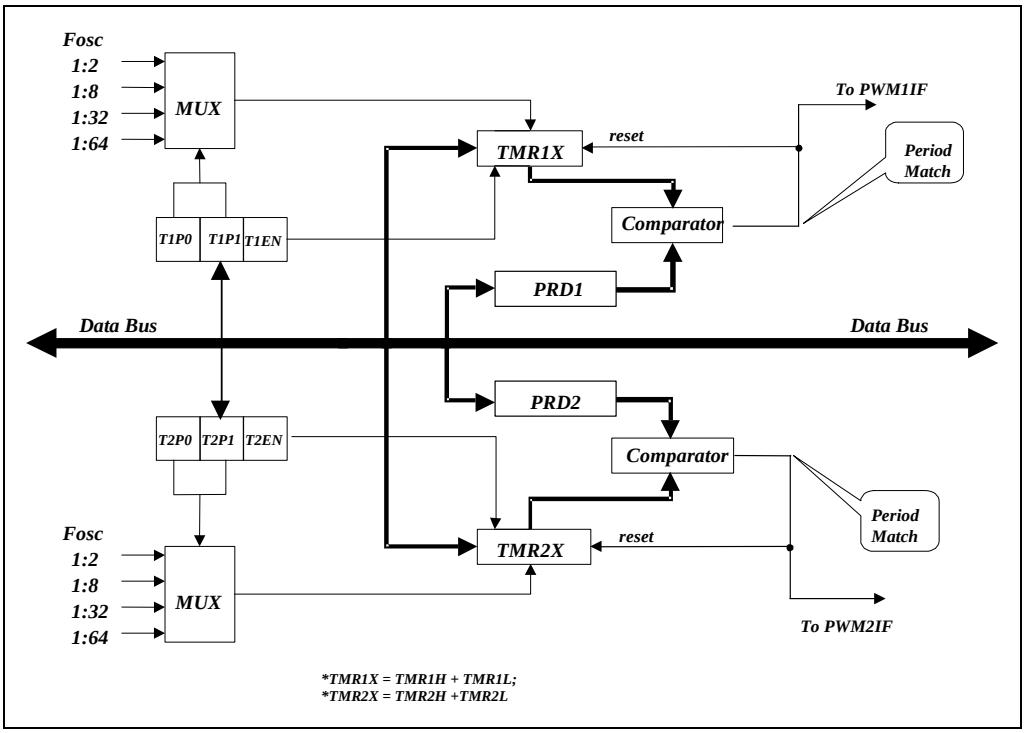


Figure 7-10 TMRX Block Diagram

Where**:**

Fosc: Input clock

Prescaler (T1P0~T1P1 and 21P0~T2P1): Options of 1:2, 1:8, 1:32, and 1:64 are defined by TMRX. It is cleared when any type of reset occurs.

TMR1X and TMR2X: Timer X register. TMRX is incremented until it matches with the value of PRDX, and then it is reset to "0". TMRX cannot be read.

PRD1 and PRDX: PWM period register

When defining TMRX, refer to the operation of its related registers as indicated in the prescaler register. Make sure that the PWMX bits are disabled if their related TMRXs are enabled. That is, Bit 6 of the PWMCON register must be set to "0."

■ **Related Control Registers (R5 Page 3) of TMR1 and TMR2**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

Perform the Timer programming procedures as follows:

1) Load PRDX with the Timer period
2) Enable the interrupt function by setting IOCF Page 0, if required
3) Load a desired value to PWMCON with the TMRX prescaler value, enable TMRX, and then, disable PWMX.

7.11 Oscillator

The EM78P5840N can be operated in three different oscillator modes; i.e., Crystal mode, IRC mode, and ERIC mode. The modes can be selected by setting the code option accordingly. The following subsections describe in details the three oscillator modes.

7.11.1 Crystal Mode

To operate in Crystal mode, one crystal and two capacitors are needed for the external circuit. In this mode, the EM78P5840N can run in three active modes, i.e., Normal mode, Green mode, and Sleep mode. The advantages of Crystal mode opeation are low power consumption (in Green mode) and a more accurate main CLK. The following figure shows the Crystal mode application circuit. Pin XIN and Pin XOUT can be directly connected to a crystal to generate an oscillation. By clearing the code option "PLLEN" to "0," Port 70 will switch and operate as a general I/O (the PLL function must be disabled to prevent activating the Normal mode). The /RESET pin will switch to Port 71 if "RESETEN" is cleared to "0."

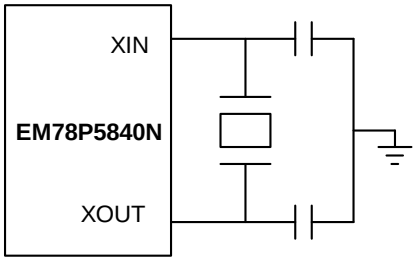


Figure 7-11a Crystal Mode Application Circuit

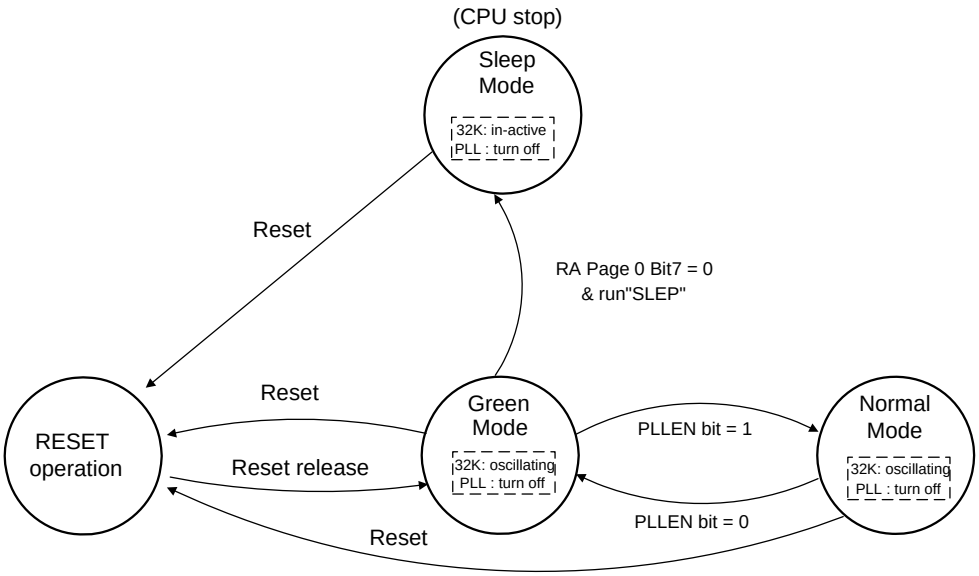


Figure 7-11b Correlation between Normal, Green, and Sleep Modes in Crystal Mode

7.11.2 IRC Mode

For some applications where timing is not critical or where accurate oscillator frequencies are not required, using the RC oscillator offers a cost effective oscillator configuration. The EM78P5840N provides an internal RC mode with default frequency values of 4M and 2 MHz. In IRC mode, the PLLC, XIN, XOUT, and /RESET pins can be defined as general purpose I/Os. The IRC oscillation frequency can vary with VDD, temperature and process variations.

■ **Internal RC Drift Rate (Ta=25°C, VDD=3.9V±5%, VSS=0V)**

Internal RC Frequency	Drift Rate			
	Temperature (-40°C ~+85°C)	Voltage (2.3V~5.5V)	Process	Total
4 MHz	±5%	±5%	±4%	±14%
2 MHz	±5%	±5%	±4%	±14%

Note: *Theoretical values are for reference only. Actual values may vary depending on the actual process.*

In IRC mode, Port 60, Port 61, and Port 70 are defined as bidirectional I/O. By clearing RESETEN in the code option to "0," the /RESET pin can also be set as input pin (Port 71). In IRC mode, only two active modes are available, i.e., Normal and Sleep modes. See Figure 7-11b for more details.

7.11.3 ERIC Mode

In ERIC mode the device has an internal capacitor and an external resistor (connected to VDD). The internal capacitor functions as a temperature compensator. In order to obtain a more accurate frequency, a precise resistor is recommended.

Note that the oscillation frequency of the RC oscillator can vary with VDD, temperatore and process variations. Moreover, the package type and the PCB layout can also affect the system frequency.

ERIC oscillation frequency is based on an external resistor. In this case, the system CLK will always be greater than 2M. That is to say, the system CLK can only be adjusted to between 2M and 6M. The following table shows the relation between the system oscillating CLK and the external resistor values.

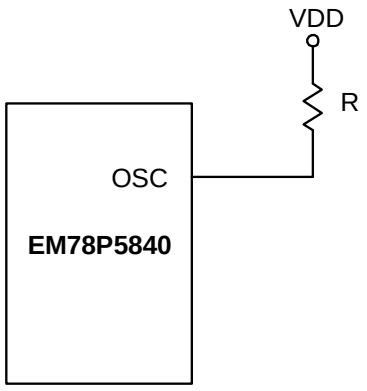


Figure 7-12a ERIC Mode Application Circuit

The relation between the system oscillating CLK and the external resistor values:

Frequency (Hz)	External Resistor (Ω)	Operating Voltage (VDD)
6M	34K	3.0V ~5.5V
5M	41K	2.8V ~5.5V
4M	51K	2.5V ~5.5V
3.58M	57K	2.2V ~5.5V
2.1M	97K	2.2V ~5.5V

Note: [1]: *Measured based on DIP packages.*

[2]: *The values are for design reference only.*

[3]: *The frequency drift is ± 30%.*

In ERIC mode, only two active modes can be achieved, i.e., Normal and Sleep modes. See the following figure (Figure 6-11b) for more details.

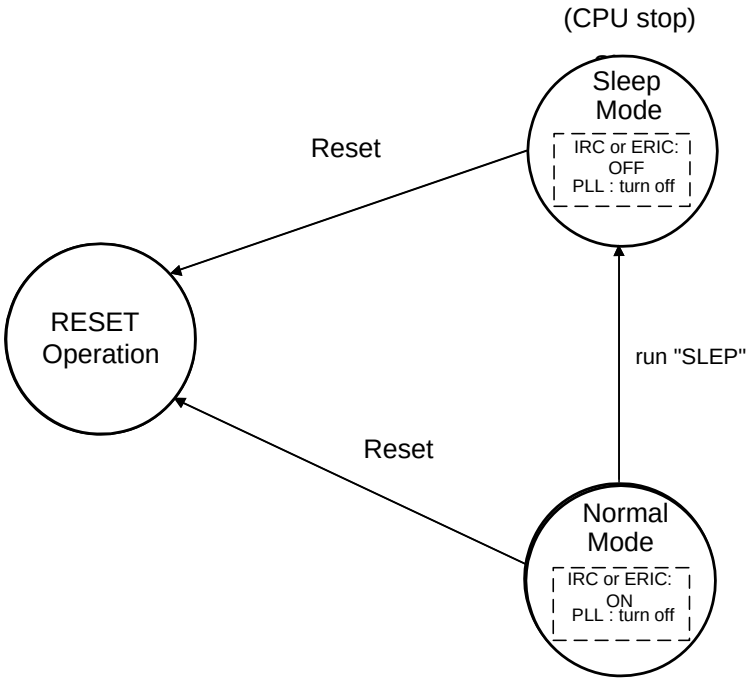


Figure 7-12b Relation between Normal and Sleep Modes in IRC and ERIC Modes

7.12 Power-on Considerations

Any microcontroller is not guaranteed to function properly before the power supply stabilizes at its steady state. The EM78P5840N power-on reset voltage ranges from 1.6V ~ 2.0V. Depending on user's application, VDD must drop to below 1.6V and remains OFF for 10 µs before power can be switched on again. This will reset the EM78P5840N and allows it to work normally. The extra external reset circuit can work well if VDD can rise at a very fast speed (50ms or less). However, in most cases where critical applications are involved and due to unstable power on conditions, extra external devices are required to deal with the power-up concerns.

7.13 External Power-on Reset Circuit

By setting the code option "RESETEN" to "0", the /RESET pin is selected. The following figure shows how an external RC produces a reset pulse. The pulse width should be kept long enough for VDD to reach minimum operating voltage. The Diode D acts as a short circuit during power down. The Capacitor C will discharge rapidly and fully.

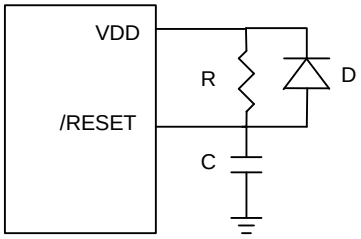


Figure 7-13a External Power-on Reset Circuit 1

The POR reset voltage varies depending on the actual temperature or process variations. For some applications, a constant reset voltage is important. The following figure shows an example circuit that supports an adjusted reset voltage. By adjusting R41 and R46, POR reset voltage will be a constant (Vpor) and the potential voltage on the /RESET pin will drop to "0" when the VDD drops to below Vpor. The graph in Figure 7-12c shows the relation between VDD and Vpor. When R41=3.9MΩ and R46=910KΩ, /RESET will remain at "0" if VDD is below 2.24V, and is reactivated after VDD goes above 2.1V (see Figure 7-13c).

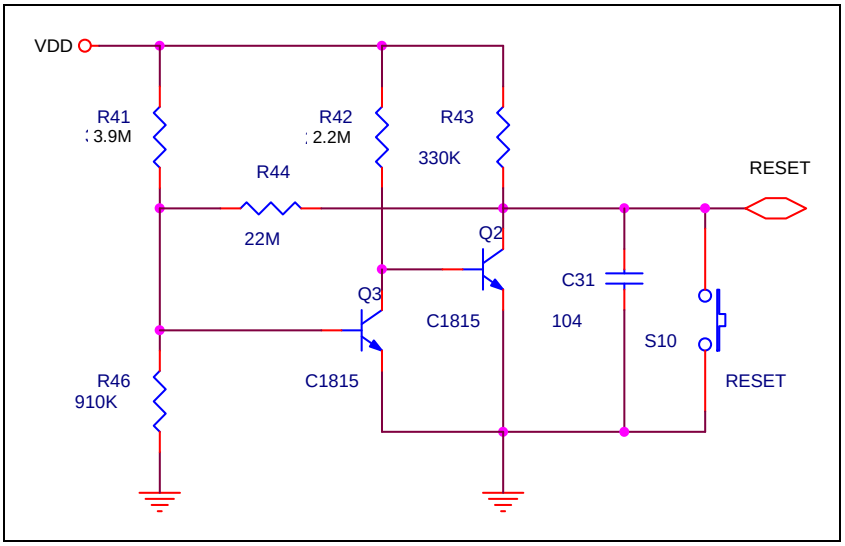


Figure 7-13b External Power-on Reset Circuit 2

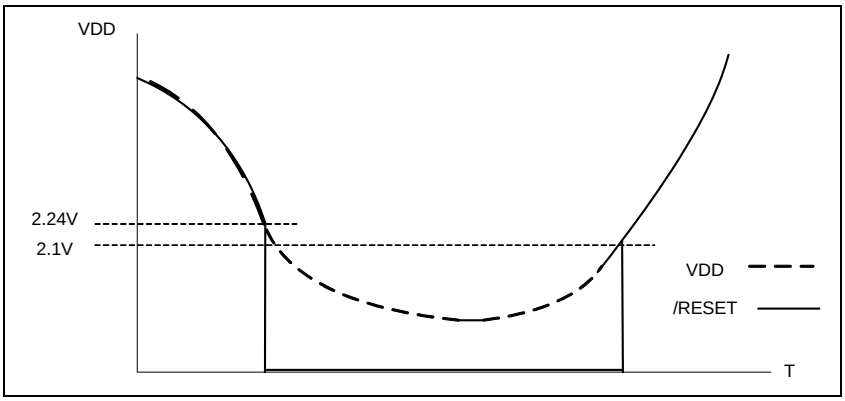


Figure 7-13c Relation between VDD and Vpor

8 Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	–0.3 To 6	V
Input Voltage	Vin	–0.5 to VDD +0.5	V
Operating Temperature Range	Ta	0 to 70	°C

9 DC Electrical Characteristics

Ta = 25°C, AVDD=VDD=5V ± 5%, VSS=0V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current for Input pins	IIL1	VIN = VDD, VSS	-	-	±1	μA
Input leakage current for bidirectional pins	IIL2	VIN = VDD, VSS	-	-	±1	μA
Input high voltage (except P71)	VIH	-	2.5	-	-	V
Input low voltage (except P71)	VIL	-	-	-	0.8	V
P71 Input high voltage	VIH	-	2.0	-	-	V
P71 Input low voltage	VIL	-	-	-	0.8	V
Input high threshold voltage	VIHT	/RESET, TCC	2.0	-	-	V
Input low threshold voltage	VILT	/RESET, TCC	-	-	0.8	V
Clock input high voltage	VIHX	OSCI	3.5	-	-	V
Clock input low voltage	VILX	OSCI	-	-	1.5	V
Output high voltage for Port C1~Port C2	VOH1	IOH = -6mA	2.4	-	-	V
Output high voltage for Port 60~Port 67; Port 7	VOH2	IOH = -10mA	2.4	-	-	V
Output high voltage for Port 9	VOH3	IOH = -15mA	2.4	-	-	V
Output low voltage for Port C1~Port C2	VOL1	IOH = 6mA	-	-	0.4	V
Output low voltage for Port 60~Port 67; Port 7	VOL2	IOH = 10mA	-	-	0.4	V
Output low voltage for Port 9	VOL3	IOH = 15mA	-	-	0.4	V
Pull-high current	IPH	Pull-high active input pin at VSS	-	–10	–15	μA
Power down current (Sleep mode)	ISB1	All input and I/O pins at VDD, Output pin floating, WDT disabled	-	1	4	μA
Low clock current (Green mode)	ISB2	CLK=32.768kHz, All analog circuits disabled, All input and I/O pins at VDD, Output pin floating, WDT disabled	-	25	35	μA
Operating supply current (Normal mode)	ICC1	/RESET=High, CLK=3.582 MHz All analog circuits disabled, Output pin floating	-	1.5	2.5	mA

9.1 Device Characteristic Graphics

The graphs below were derived based on a limited number of samples and they are provided for reference only. Hence, the device characteristics shown herein cannot be guaranteed as fully accurate. In these graphs, the data exceeding the specified operating range are shown for information purposes only. The device will operate properly only within the specified range.

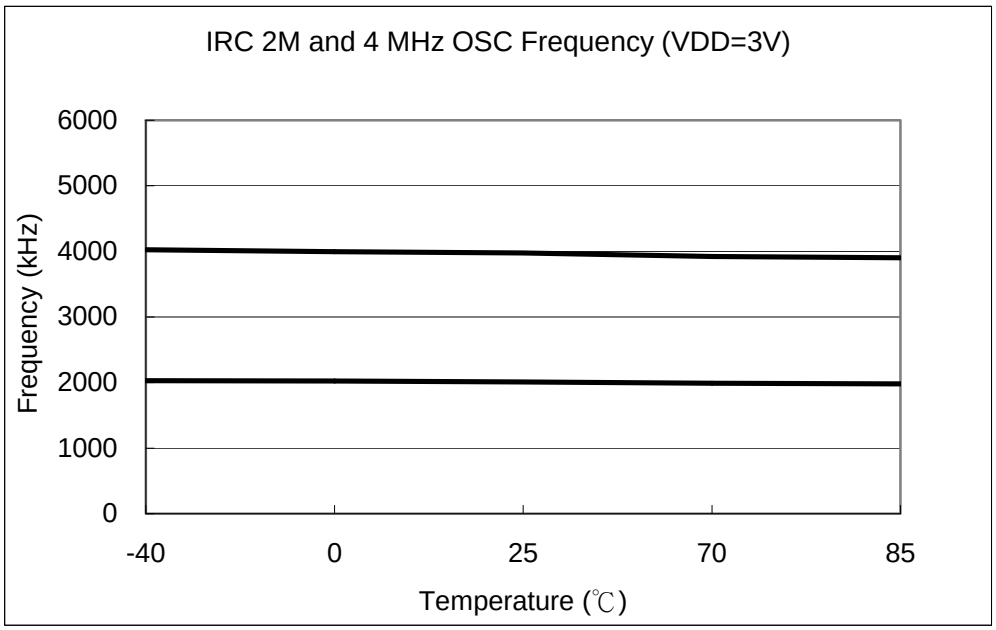


Fig. 9-1 Internal RC OSC Frequency vs. Temperature, VDD=3V

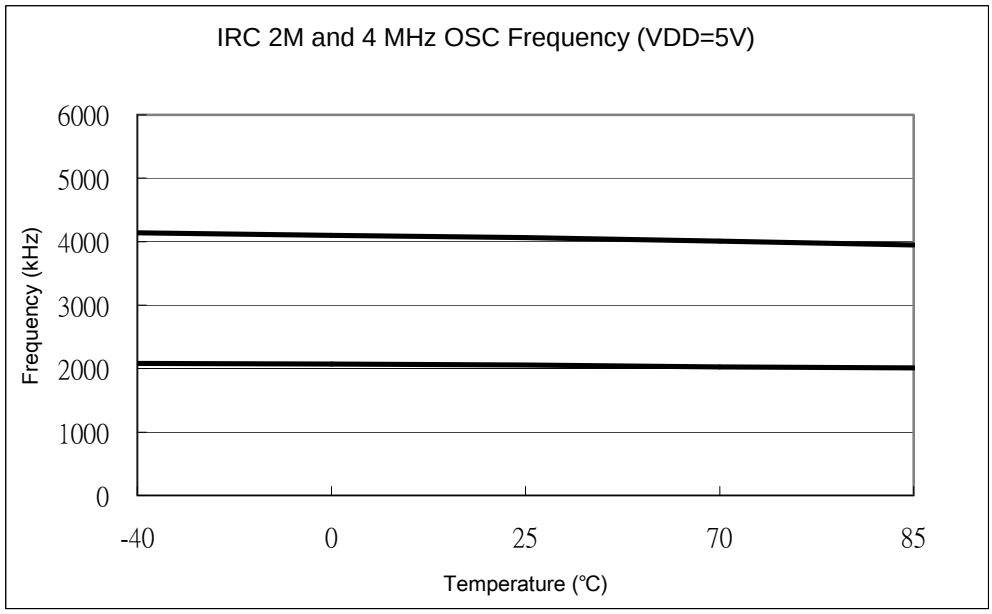


Fig. 9-2 Internal RC OSC Frequency vs. Temperature, VDD=5V

10 AC Electrical Characteristics

■ CPU Instruction Timing (Ta = 25°C, AVDD=VDD=5V, VSS=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk	-	45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.582 MHz	-	60 550	-	μs ns
Device delay hold time	Tdrh	-	-	16	-	ms
TCC input period	Ttcc	*	(Tins+20)/N	-	-	ns
Watchdog timer period	Twdt	Ta = 25°C	16-30%	16	16+30%	ms

**N* = selected prescaler ratio*

■ ADC Characteristics (VDD = 5V, Ta = +25°C, for Internal Reference Voltage)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Upper bound offset voltage	Vofh	-	-	44	52.8	mV
Lower bound offset voltage	Vofl	-	-	32	38.4	mV

These parameters are theoretical values and have not been tested. See Section 9.2, *The Characteristics of EM78P5840N 10-bit ADC* for further details.

■ Timing Characteristics (AVDD=VDD=5V,Ta=+25°C)

Description		Symbol	Min.	Typ.	Max.	Unit
Oscillator Timing Characteristics						
Crystal start up	32.768kHz	Tosc	400	-	1500	ms
	3.579 MHz PLL	-	-	5	10	μs
Timing Characteristics of Reset						
The minimum width of the reset low pulse		Trst	3	-	-	μs
The delay between reset and the start of the program		Tdrs	-	18	-	ms

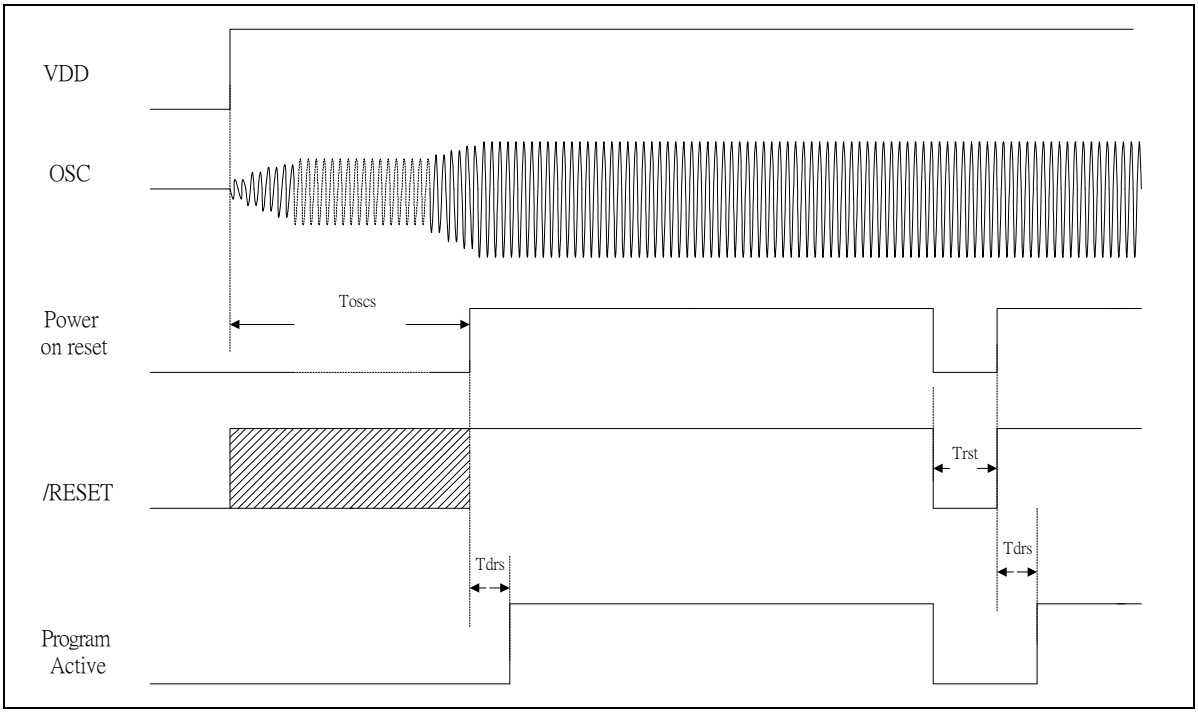
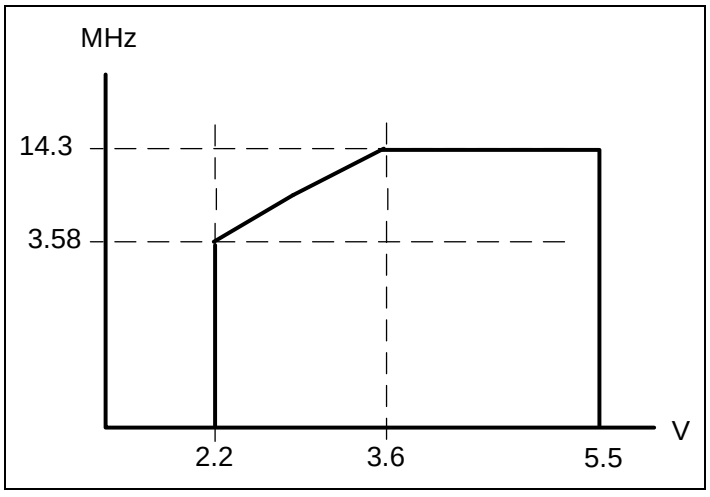


Figure 10-1 Relation between OSC Stable Time and Power-on Reset

10.1 Operating Voltage vs Main CLK

Y axis: main CLK



X axis: min VDD

Figure 10-2 Relation between Operating Voltage and the Main CLK

10.2 10-Bit ADC Characteristics

The EM78P5840N has a built-in 10-bit resolution, multi-channel ADC function. In an ideal situation, if ADC's reference voltage is 5V, the ADC's LSB is 5V/1024. However, due to some physical or circuit characteristics, the convertion result may be adversely affected. An example is shown in the next figure. The offset voltage reduces the AD's converter range. If the AD's input voltage is less than VOFL, the ADC will output a "0." On the other hand, if the input voltage is larger than (VDD-VOFH), the ADC will output 1023. That is , the AD converter range will be replaced by (VDD-VOFH+LSB-VOFL+LSB).

If VRB = VOFL – LSB and

VRT = VDD-VOFH+LSB, then LSB is:

$$LSB = \frac{(VRT - VRB)}{1024}$$

$$LSB = \frac{\left(VDD - (VOFH + VOFL) \right)}{1022}$$

NOTE

During actual operation, carefully observe the resulting effect of the AD offset voltage. When the converter range is VRT ~ VRB, the AD converter's result will be more precised.

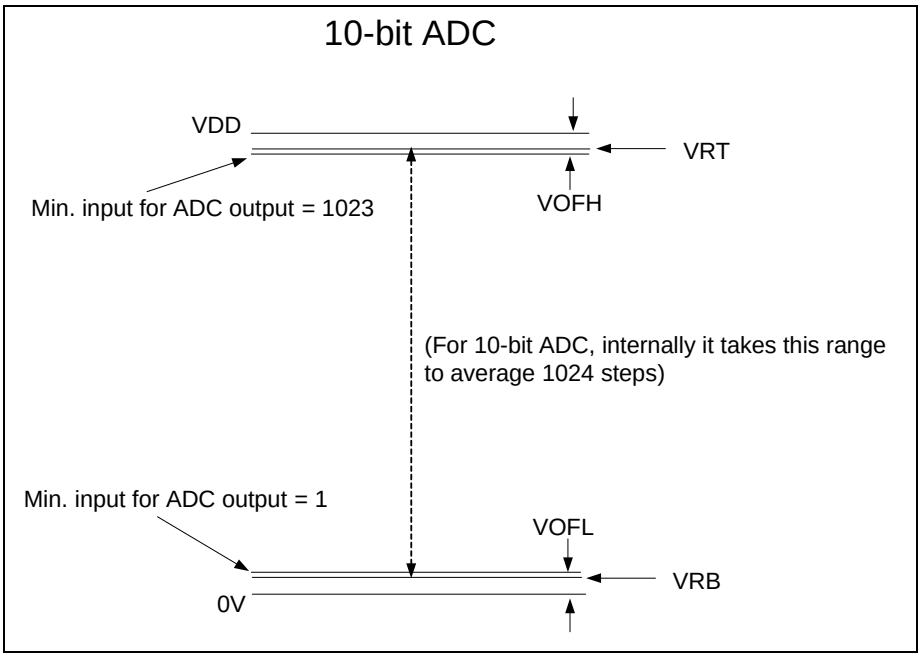
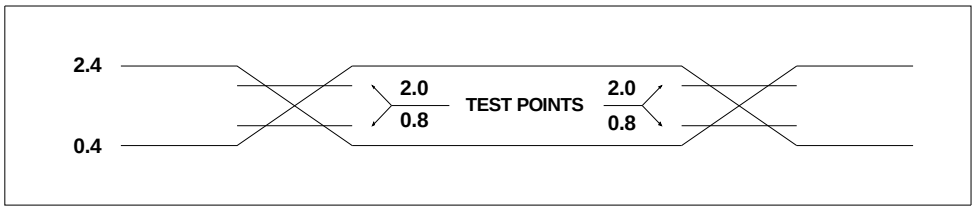


Figure 10-3 Relation between ADC and Offset Voltage

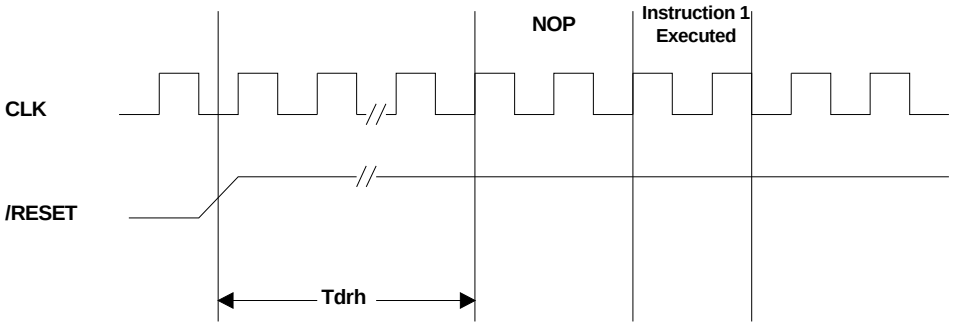
11 Timing Diagrams

AC Test Input/Output Waveform



AC Testing : Input is driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")

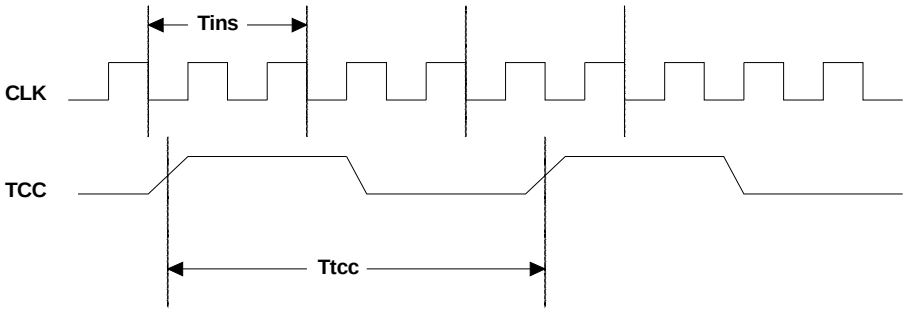


Figure 11 AC Timing Diagrams

12 OTP ROM Burning Pins

One time programmable ROM burning pins:

OTP Pin Name	Mask ROM Pin Name
VDD	AVDD
VPP	/RESET
DINCK	P65
ACLK	P64
PGMB	P63
OEB	P62
DATA	P73
GND	AVSS

APPENDIX

A Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P5840ND18J/S	DIP	18 pins	300 mil
EM78P5840NSO18J/S	SOP	18 pins	300 mil
EM78P5840ND20J/S	DIP	20 pins	300 mil
EM78P5840NSO20J/S	SOP	20 pins	300 mil
EM78P5840ND24J/S	DIP	24 pins	600 mil
EM78P5840NK24J/S	Skinny DIP	24 pins	300 mil
EM78P5840NSO20J/S	SOP	24 pins	300 mil

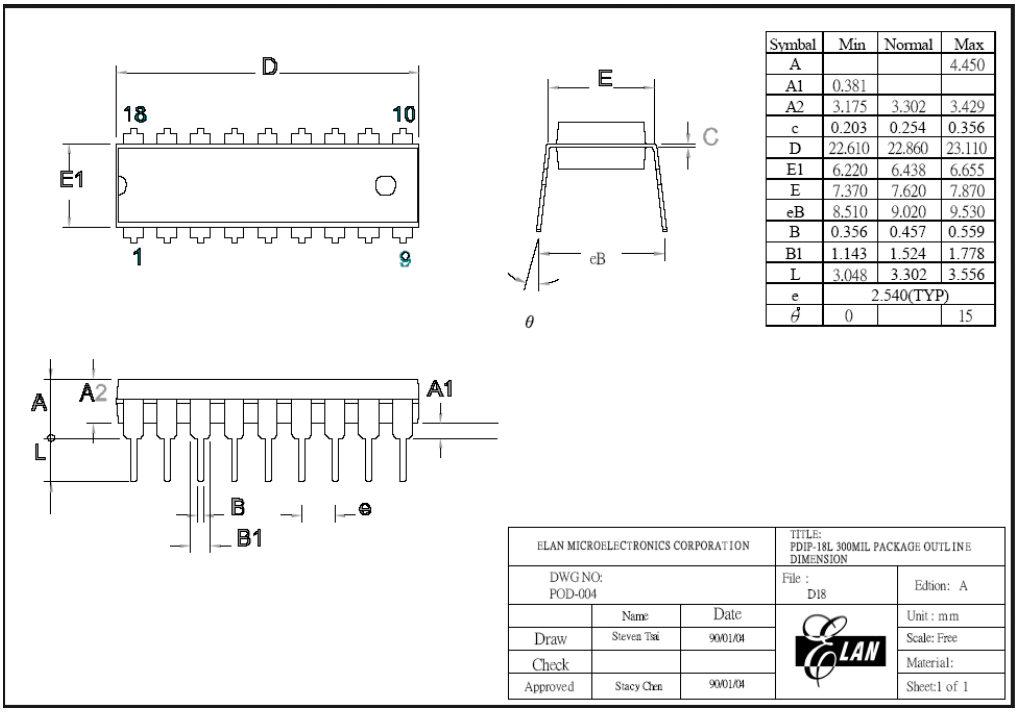
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78P5840NJ/S
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point(°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	> 50%

B Package Information

B.1 EM78P5840ND18

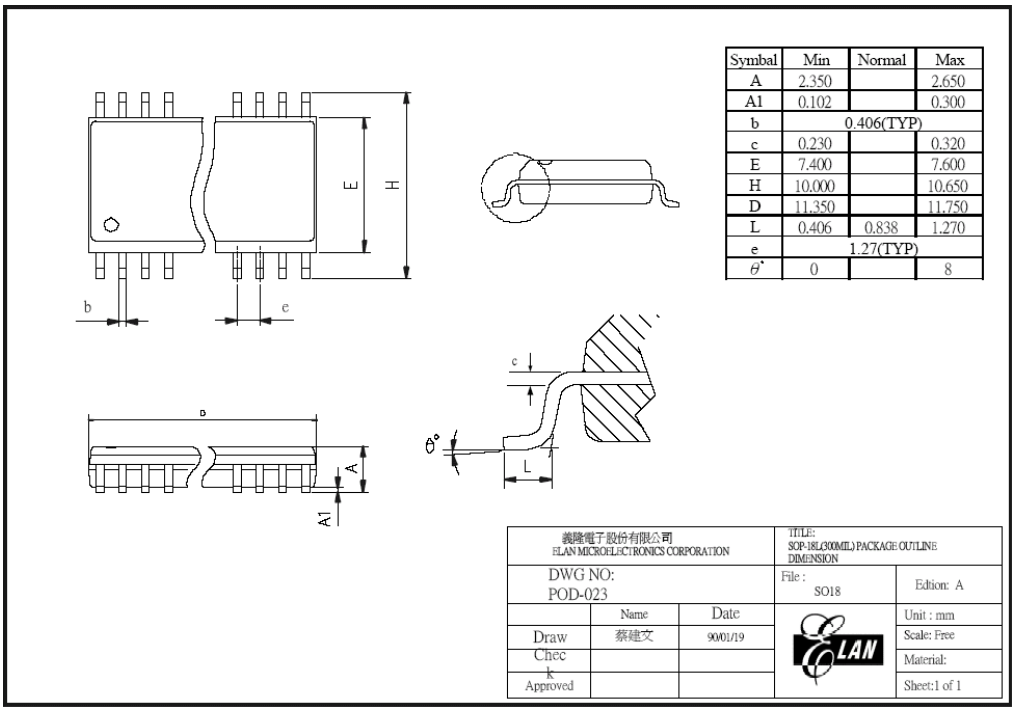


Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

ELAN MICROELECTRONICS CORPORATION			TITLE: PDIP-18L 300MIL PACKAGE OUTLINE DIMENSION	
DWG NO: POD-004			File : D18	Edtion: A
	Name	Date		Unit : mm
Draw	Steven Tsai	90/01/04		Scale: Free
Check				Material:
Approved	Stacy Chen	90/01/04		Sheet:1 of 1

Figure B-1 EM78P5840N 18-pin DIP Package Type

B.2 EM78P5840NSO18

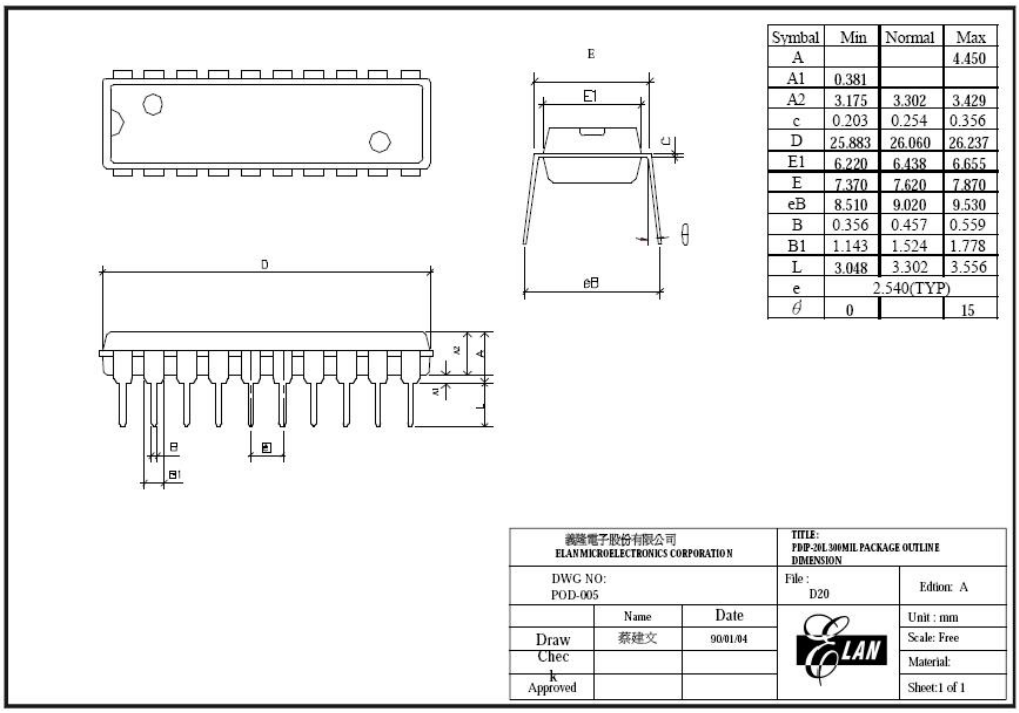


Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e	1.27(TYP)		
θ°	0		8

義隆電子股份有限公司 ELAN MICROELECTRONICS CORPORATION			TITLE: SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION	
DWG NO: POD-023			File : SO18	Edition: A
	Name	Date		Unit : mm
Draw	蔡建文	90/01/19		Scale: Free
Chec k				Material:
Approved				Sheet:1 of 1

Figure B-2 EM78P5840N 18-pin SOP Package Type

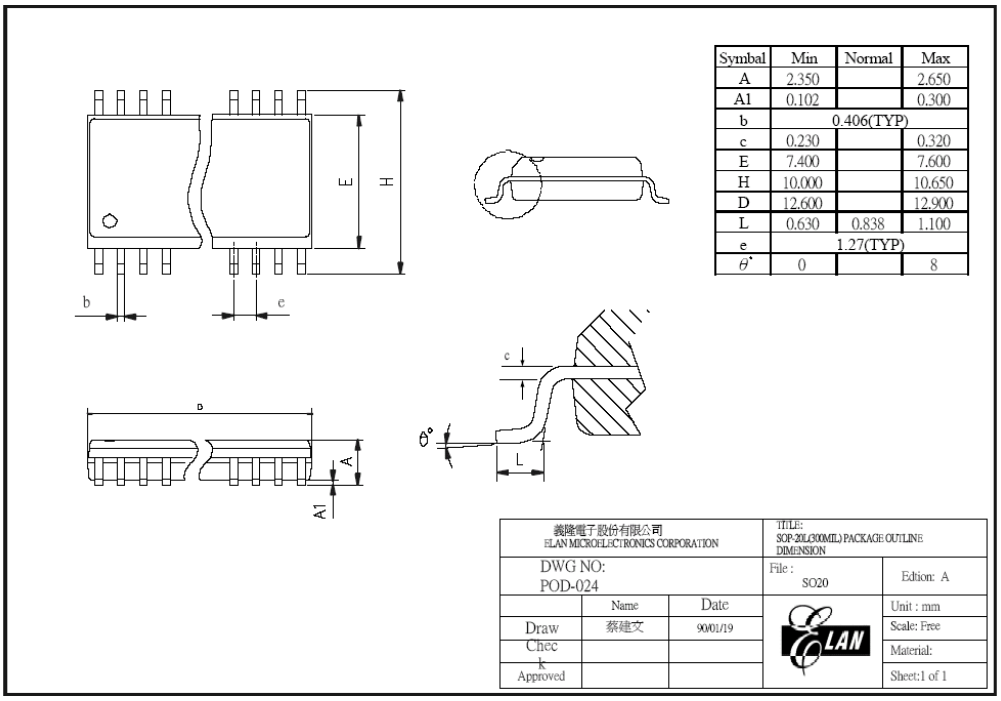
B.3 EM78P5840ND20



Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

Figure B-3 EM78P5840N 20-pin DIP Package Type

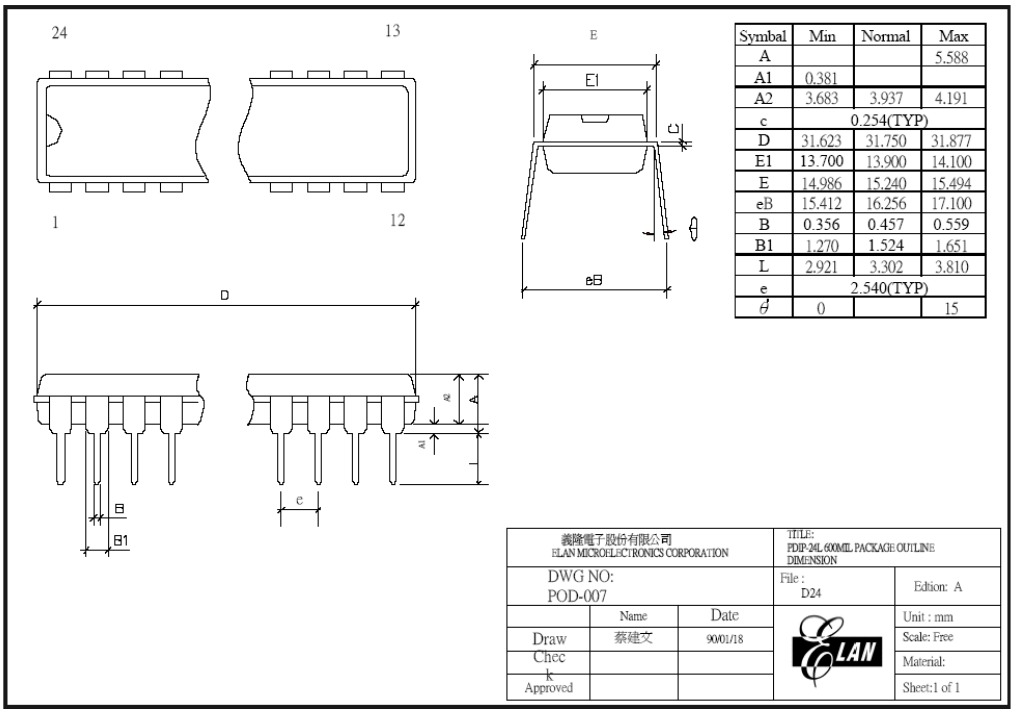
B.4 EM78P5840NSO20



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e		1.27(TYP)	
θ°	0		8

Figure B-4 EM78P5840N 20-pin SOP Package Type

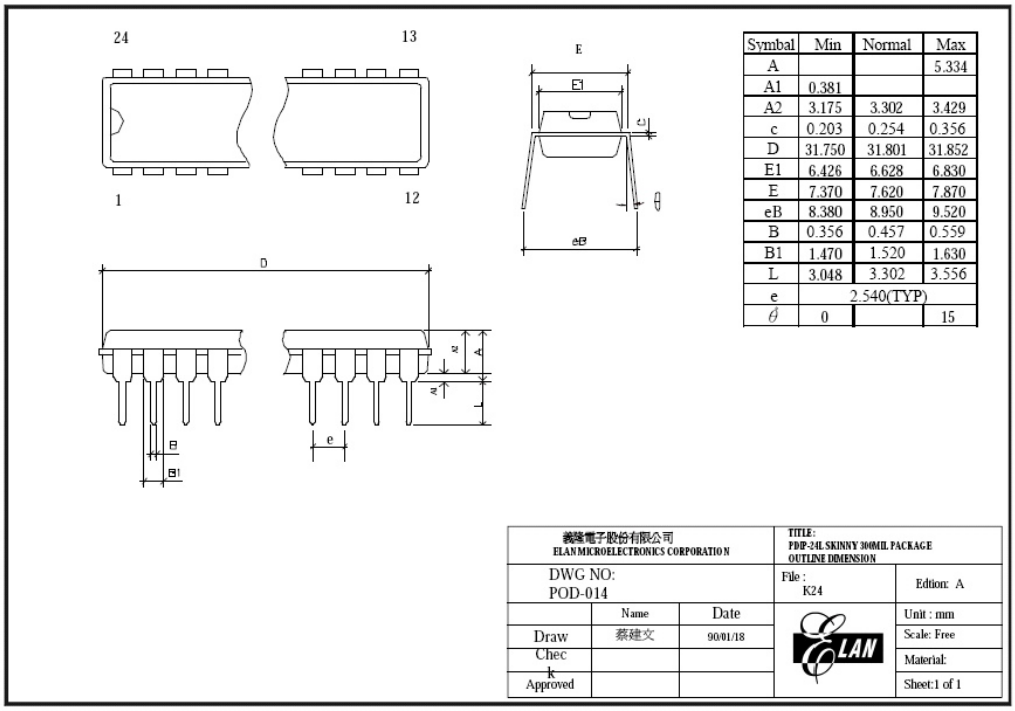
B.5 EM78P5840ND24



Symbal	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.683	3.937	4.191
c		0.254(TYP)	
D	31.623	31.750	31.877
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.356	0.457	0.559
B1	1.270	1.524	1.651
L	2.921	3.302	3.810
e		2.540(TYP)	
θ	0		15

Figure B-5 EM78P5840N 24-pin DIP Package Type

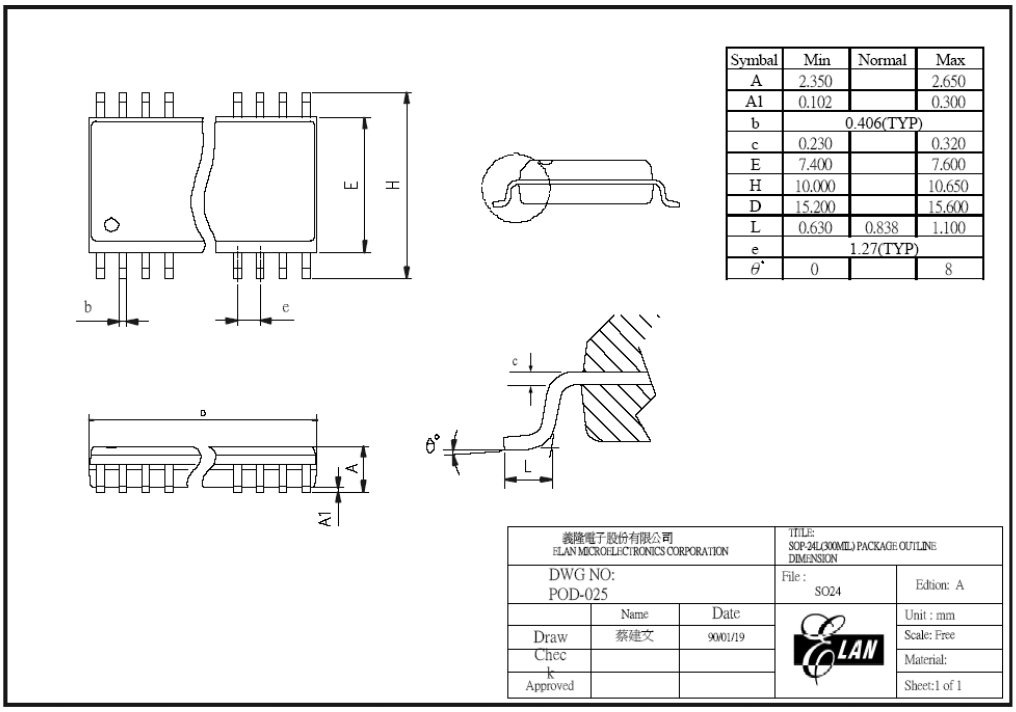
B.6 EM78P5840NK24



Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	31.750	31.801	31.852
E1	6.426	6.628	6.830
E	7.370	7.620	7.870
eB	8.380	8.950	9.520
B	0.356	0.457	0.559
B1	1.470	1.520	1.630
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

Figure B-6 EM78P5840N 24-pin Skinny DIP Package Type

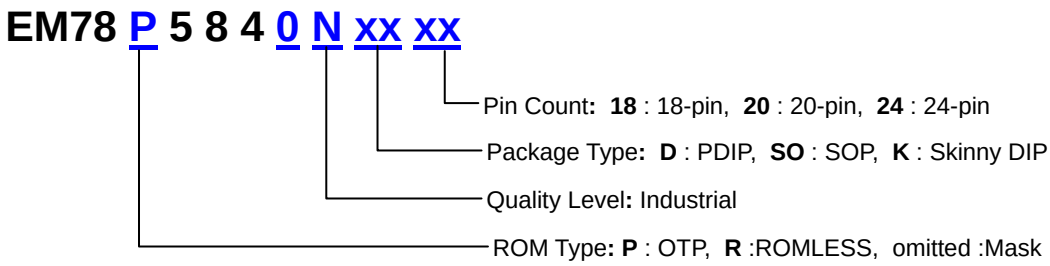
B.7 EM78P5840NSO24



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

Figure B-7 EM78P5840N 24-pin SOP Package Type

C Numbering System



D EM78P5840N Series

D.1 EM78P5840N Series Category

ROMLESS	OTP	Mask
ICE5840	EM78P5840N	EM785840N

D.1.1 Difference between ICE5840, EM78P5840N and EM785840N

Item	ICE5840	EM78P5840N Series	EM785840N Series
CID RAM	1024 byte	NA	NA
CID RAM Address Auto +1	✓	NA	NA
CNT1*	8-bit counter	8-bit counter	8 or 16 (shared with CNT2) bit counter
CNT2**	×	×	✓*
Stack	12	8	8

**CNT1 can be shared with CNT2 to generate a 16-bit counter under EM785840N.*

***CNT2 is NOT supported in ICE5840 and EM78P5840N.*

D.1.2 Difference between EM78P5840Nxx18, EM78P5840Nxx20, and EM78P5840Nxx24

Pin Count	18	20	24
PWM	×	2 channels	2 channels
AD Channel	8	8	8
IO (max.)	16	18	22

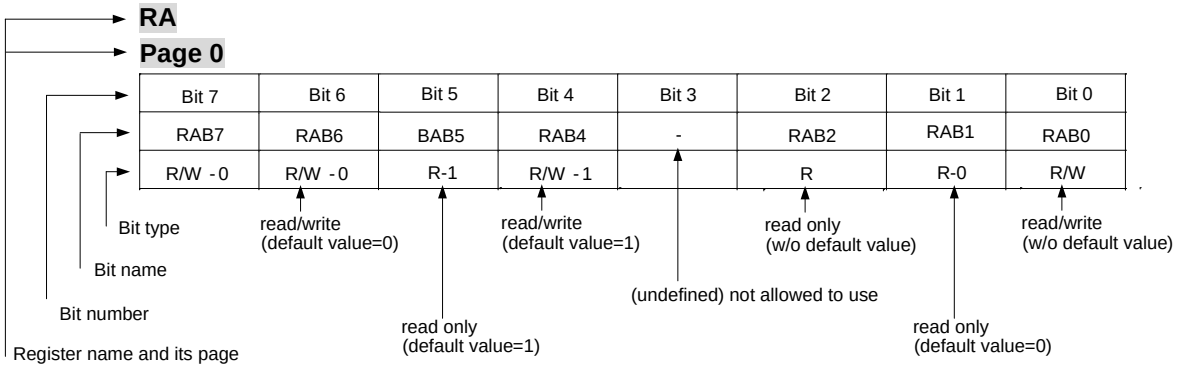
E Application Notes

1. There are some undefined or not existing bits in the registers. User needs to be cautious in dealing with those bits while programming and should not use them as data to execute logic or math operations, since those bits have no relative functions and have never been tested. Different symbols are used to distinguish them.

   "**0**" or "**1**" → value always equal to 0 or value always equal to 1, (not existent, read only)

   "**-**" → value unknown, (not existent) undefined bits are not allowed for use.

2. You will notice that most of the register bit number, name, type, etc., are shown in table format in this specification. The following are the conventions used to describe the entry in each row and column in the table.



3. Do NOT switch the MCU operation mode from Normal mode to Sleep mode directly. Before going into Idle or Sleep mode, switch the MCU to Green mode first.
4. While switching the main clock (regardless whether from high freq to low freq or vice versa), adding six instruction delay (NOP) is required.
5. The offset voltage will affect the ADC result. See Figure 10-3 in Section 10-2 for details.
6. Do NOT connect unnecessary circuits on the OTP burner pins during the burning process of the OTP ROM.
7. For low pin count package, some pins do not appear on the package, but they exist on dies. Do NOT keep these unused pins floating. Set these pins output to high or low.

F Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15mins)~150°C (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350mm^3 ----225±5°C) (Pkg thickness ≤ 2.5mm or Pkg volume ≤ 350mm^3 ----240±5°C)	
Temperature cycle test	-65°C (15mins)~150°C (15mins), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%, TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥ ｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ ｜± 300V｜	

F.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.