eKTF5616/08

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Version	Revision Description	Date
1.0	Initial Release Version	2017/05/22
1.1	Delete Internal RC frequency 4MHz information	2017/07/27
1.2	1. Modify I2C function pin description 2. Modify DC Electrical Characteristics & Add IOH3/IOL3 information 3. Modify feature information 4. Add APPENDIX : D Quality Assurance and Reliability	2018/04/20
1.3	Add eKTF5616SS20A package type	2019/09/10
1.4	Add eKTF5616AQN24 package type	2022/01/20

User Application Note

1. OCDS simulation 12MHz need select other frequency first, then set Bank0 RE bit1~0(RCM1~RCM0) change to 12MHz
2. When P50//RESET is /RESET pin, P50 must set input.

1 General Description

The eKTF5616/08 is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It has a built-in 4K×16-bit programmable ROM and is equipped with touch sensors. The capacitive touch key sensor uses plastic or glass substrate as cover.

The system controller converts fingertip position data into button presses, depending on finger location and human interface context. The eKTF5616/08 OCD can be used to develop user program for this microcontroller and several other ELAN Flash type ICs.

2 Features

- CPU configuration
  - Supports 4K×16 bits program ROM
  - (48+512) bytes general purpose register.
  - **128** bytes in-system programmable EEPROM
  - 16-level stacks for subroutine nesting
  - 3 programmable Level Volt Reset
    LVR: 4.2V, 3.6V, 2.5V
  - 1 sets of 16 programmable Level Voltage Detector
    LVD: 4.7V, 4.5V, 4.3V, 4.1V, 3.9V, 3.7V, 3.5V, 3.3V, 3.1V, 2.9V, 2.8V, 2.6V, 2.5V, 2.4V, 2.3V, 2.2V
  - Four CPU operation modes (Normal, Green, Idle, Sleep)
  - Typically 1 uA, during sleep mode
- I/O port configuration
  - 4 bidirectional I/O ports: P5 ~ P8
  - 4 programmable pin change wake-up ports: P5~P8
  - 4 programmable pull-down I/O ports: P5~P8
  - 4 programmable pull-high I/O ports: P5~P8
  - 4 programmable open-drain I/O ports: P5~P8
  - 4 programmable high-sink/drive I/O ports: P5~P8
  - High-drive 30mA(typically)
  - High-sink 80mA(typically)
- Operating voltage range:
  - 2.1V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (base on two clocks):

Main oscillator:

- IRC mode:
  DC ~ 16 MHz at 3V; DC ~ 8 MHz at 2.1V

Internal RC Frequency	Drift Rate				
	Temperature(-40℃ ~+85℃) + Voltage(2.1V~5.5V)		Process (UWTR:±1% NUWTR: ±0.5%)	Total	
	VDD	Internal Vref.		VDD	Internal Vref.
8MHz	±9.5%	±2%	±1%	±10.5%	±3%
12MHz	±9.5%	±2%	±1%	±10.5%	±3%
16MHz	±9.5%	±2%	±1%	±10.5%	±3%

*Internal Vref. : UWTR total ±3%, NUWTR total ±2.5%

Sub oscillator:

- IRC mode: 16K/32K

- Peripheral configuration
  - 8-bit real time clock (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Two Pulse Width Modulation (PWMA, PWMB) with 16-bit resolution shared with Timers A and B
  - One 8-bit timer TC1 with six modes: Timer/Counter/Capture/Window/Buzzer/PWM/ PDO (Programmable Divider Output) modes.
  - Touch key function 16 traces for 2 groups
  - 8-channel Analog-to-Digital converter with 12bit resolution + 1 internal reference for Vref & 1/2VDD(power detector)
  - Serial transmitter/receiver interface (SPI): 3-wire synchronous communication
  - I^2C function with 7/10 bits address and 8 bits data transmit/receive mode
  - Universal asynchronous receiver/transmitter (UART) available
  - Power down (Sleep) mode
  - Idle with scan mode
- 18 available interrupts: (2 external, 19 internal)
  - External interrupt: P54, P55
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - PWMA, PWMB period match completion
  - TC1 interrupt
  - I^2C transfer/receive/stop interrupt
  - SPI interrupt
  - UART TX, RX , RX error interrupt
  - LVD interrupt
  - System hold interrupt
  - ADC completion interrupt
  - TK Scan interrupt
- Single instruction cycle commands
- Package Type:
  - 28 SOP(300mil) : eKTF5616SO28
  - 20 SOP(300mil) : eKTF5616SO20
  - 16 SOP(150mil) : eKTF5608SO16A
  - 24 QFN(4*4*0.8mm) : eKTF5616QN24
  - 24 QFN(4*4*0.8mm) : eKTF5616AQN24
  - 20 SSOP(150mil) : eKTF5616SS20A

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Assignment

3.1 Package: SOP 28

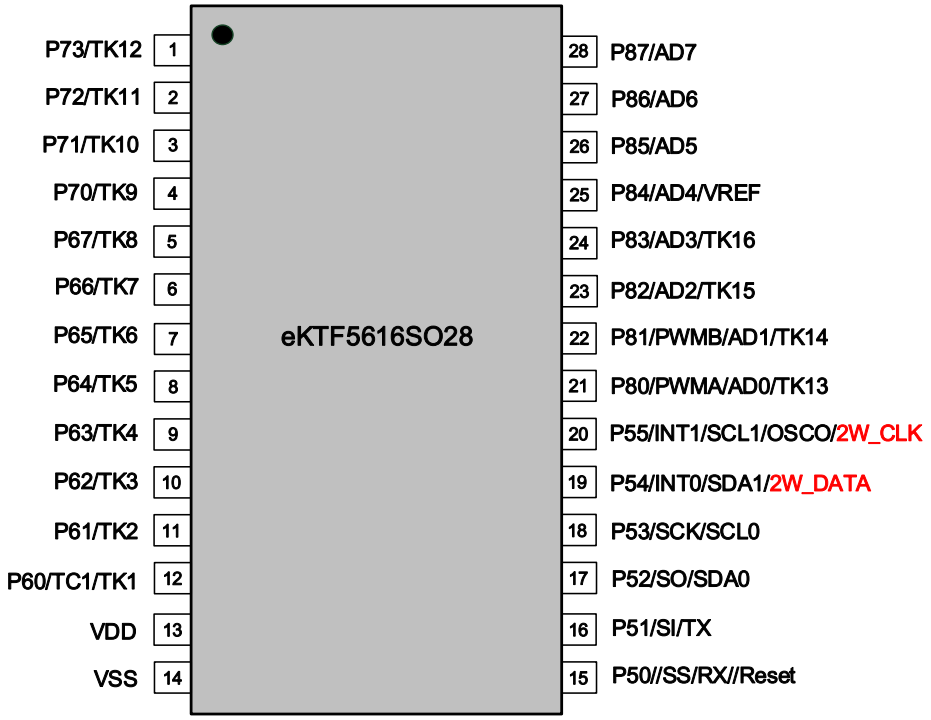


Figure 3-1 SOP-28 Pin Assignment

3.2 Package: SOP 20

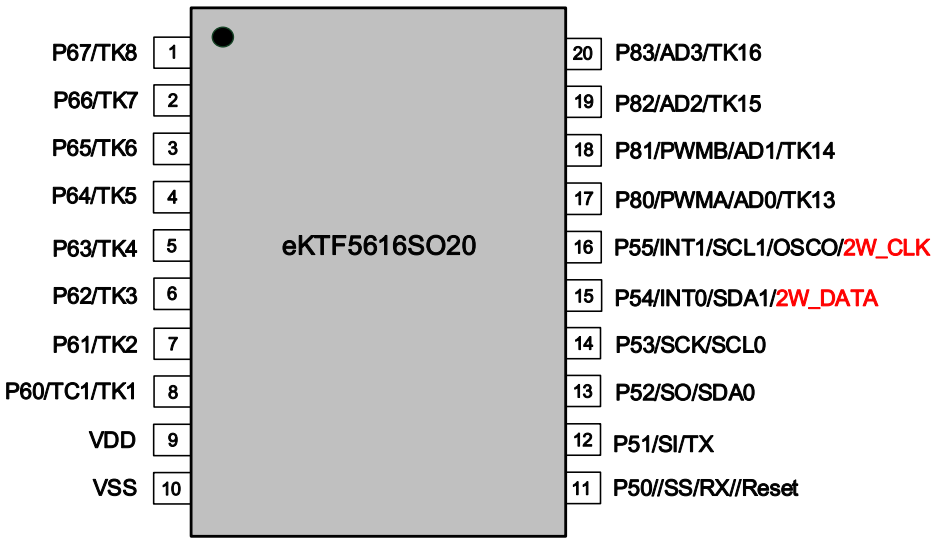


Figure 3-2 SOP-20 Pin Assignment

3.3 Package: QFN 24

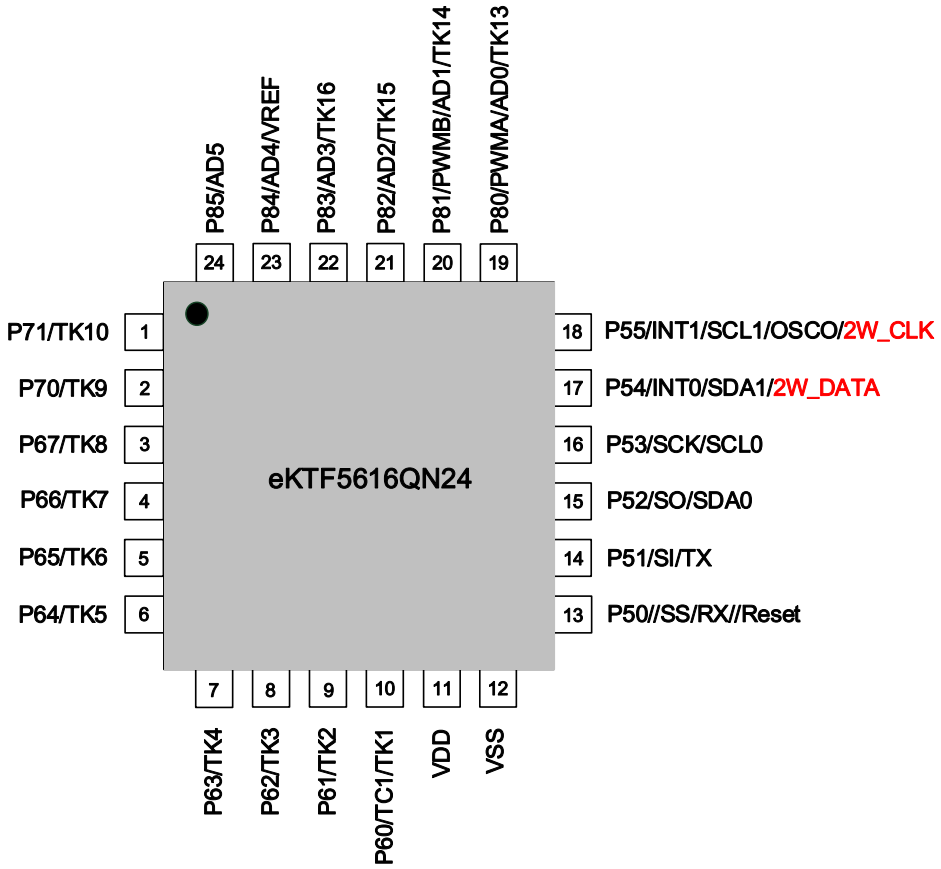


Figure 3-3 QFN-24 Pin Assignment

3.4 Package: SOP 16

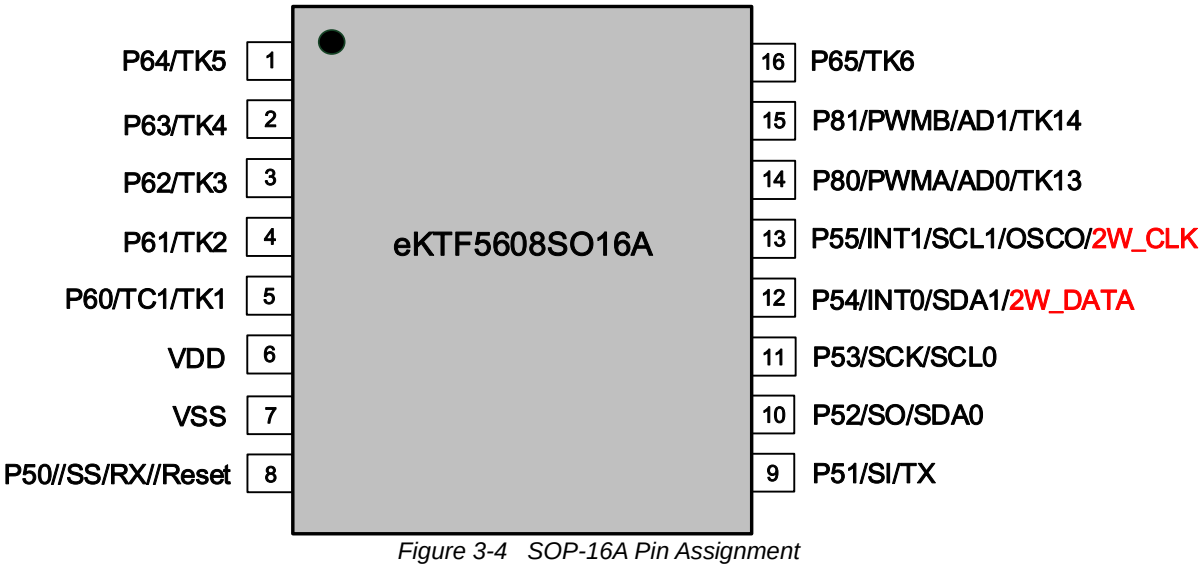


Figure 3-4 SOP-16A Pin Assignment

3.5 Package: SSOP 20

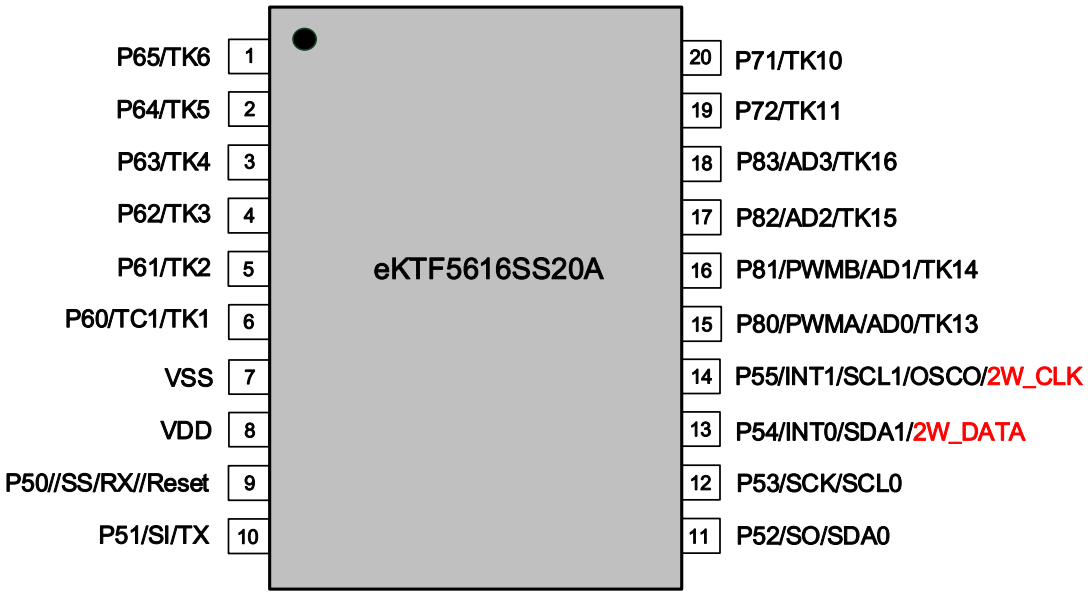


Figure 3-5 SSOP-20A Pin Assignment

3.6 Package: AQFN 24

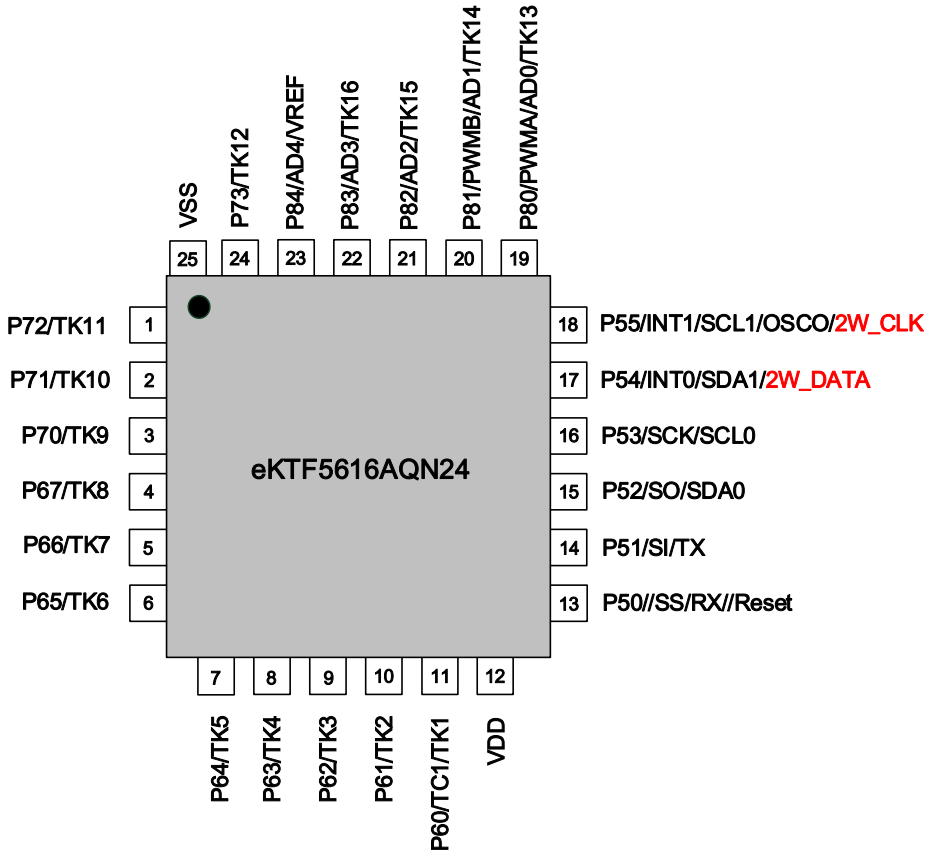


Figure 3-6 AQFN-24 Pin Assignment

4 Pin Description

Name	Function	Input Type	Output Type	Description
VDD	VDD	Power	–	Kernel Power
VSS	VSS	Power	–	Kernel Ground
P50//SS/RX//RESET	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	/SS	ST	–	SPI slave mode enable
	RX	ST	–	UART data receive input (RX)
	/RESET	ST	–	Internal pull-high reset pin *** When P50//RESET is /RESET pin, P50 must set input.**
P51/SI/TX	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	SI	ST	–	SPI serial data input
	TX	–	CMOS	UART data transmit output (TX)
P52/SO/SDA0	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	SO	–	CMOS	SPI serial data output
	SDA0	ST	CMOS	I^2C serial data line. It is open-drain
P53/SCK/SCL0	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	SCK	ST	CMOS	SPI serial clock input/output
	SCL0	ST	CMOS	I^2C serial clock line. It is open-drain
P54/INT0/SDA1/ 2W_DATA	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	INT0	ST	–	External interrupt pin
	2W_DATA	ST	CMOS	OCD data line
	SDA1	ST	CMOS	I^2C serial data line. It is open-drain
P55/INT1/SCL1/OSCO 2W_CLK	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	INT1	ST	–	External interrupt pin
	2W_CLK	ST	CMOS	OCD clock line
	SCL1	ST	CMOS	I^2C serial clock line. It is open-drain
	OSCO	–	CMOS	Clock output of internal RC oscillator
P60/TK1/TC1	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK1	AN	–	TK1 are Touch Key pins
	TC1	ST	CMOS	8-bit Timer/Counter 1

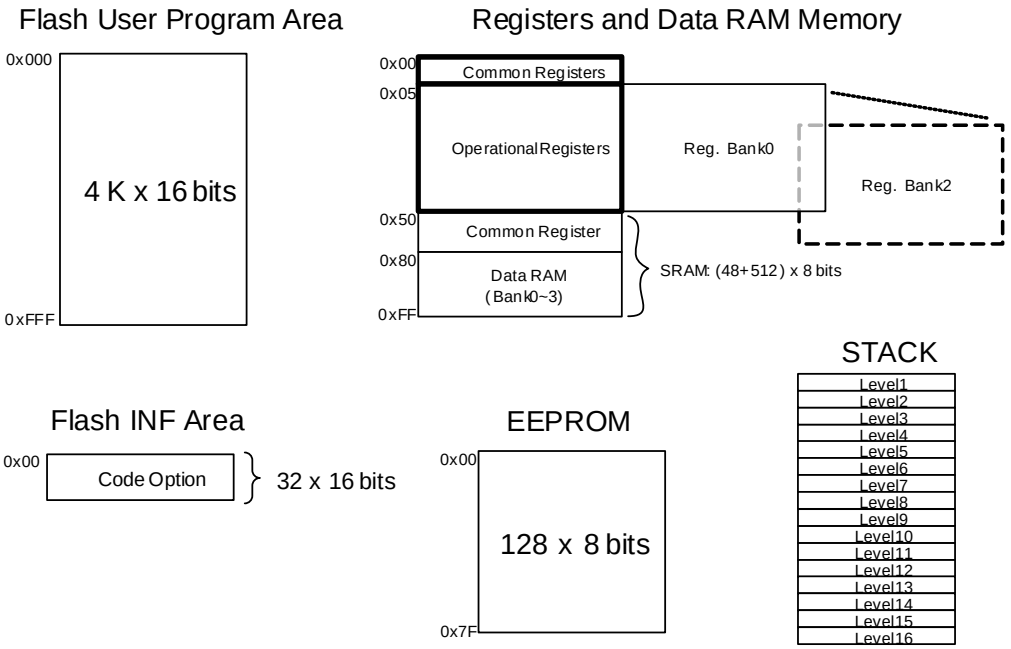
Name	Function	Input Type	Output Type	Description
P61/TK2	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK2	AN	–	TK2 are Touch Key pins
P62/TK3	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK3	AN	–	TK3 are Touch Key pins
P63/TK4	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK4	AN	–	TK4 are Touch Key pins
P64/TK5	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK5	AN	–	TK5 are Touch Key pins
P65/TK6	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK6	AN	–	TK6 are Touch Key pins
P66/TK7	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK7	AN	–	TK7 are Touch Key pins
P67/TK8	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK8	AN	–	TK8 are Touch Key pins
P70/TK9	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK9	AN	–	TK9 are Touch Key pins
P71/TK10	P71	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK10	AN	–	TK10 are Touch Key pins
P72/TK11	P72	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK11	AN	–	TK11 are Touch Key pins
P73/TK12	P73	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK12	AN	–	TK12 are Touch Key pins
P80/TK13/AD0/PWMA	P80	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD0	AN	–	Analog to Digital Converter input pins
	TK13	AN	–	TK13 are Touch Key pins
	PWMA	–	CMOS	PWMA output
P81/TK14/AD1/PWMB	P81	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up

Name	Function	Input Type	Output Type	Description
	TK14	AN	–	TK14 are Touch Key pins
	AD1	AN	–	Analog to Digital Converter input pins
	PWMB	–	CMOS	PWMB output
P82/TK15/AD2	P82	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK15	AN	–	TK15 are Touch Key pins
	AD2	AN	–	Analog to Digital Converter input pins
P83/TK16/AD3	P83	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TK16	AN	–	TK16 are Touch Key pins
	AD3	AN	–	Analog to Digital Converter input pins
P84/VREF/AD4	P84	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	VREF	AN	–	External reference voltage for ADC
	AD4	AN	–	Analog to Digital Converter input pins
P85/AD5	P85	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD5	AN	–	Analog to Digital Converter input pins
P86/AD6	P86	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD6	AN	–	Analog to Digital Converter input pins
P87/AD7	P87	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD7	AN	–	Analog to Digital Converter input pins

Note: *OCD: On-Chip Debug system*

5 System Overview

5.1 Memory Map



Notes:

1. Flash User Program Area is protected when power down occurs, and will not be read, written and erased from the OCDS.

2. EEPROM can be protected by Code Option Word0<2~0>, and will not be read from the OCDS.

5.2 Block Diagram

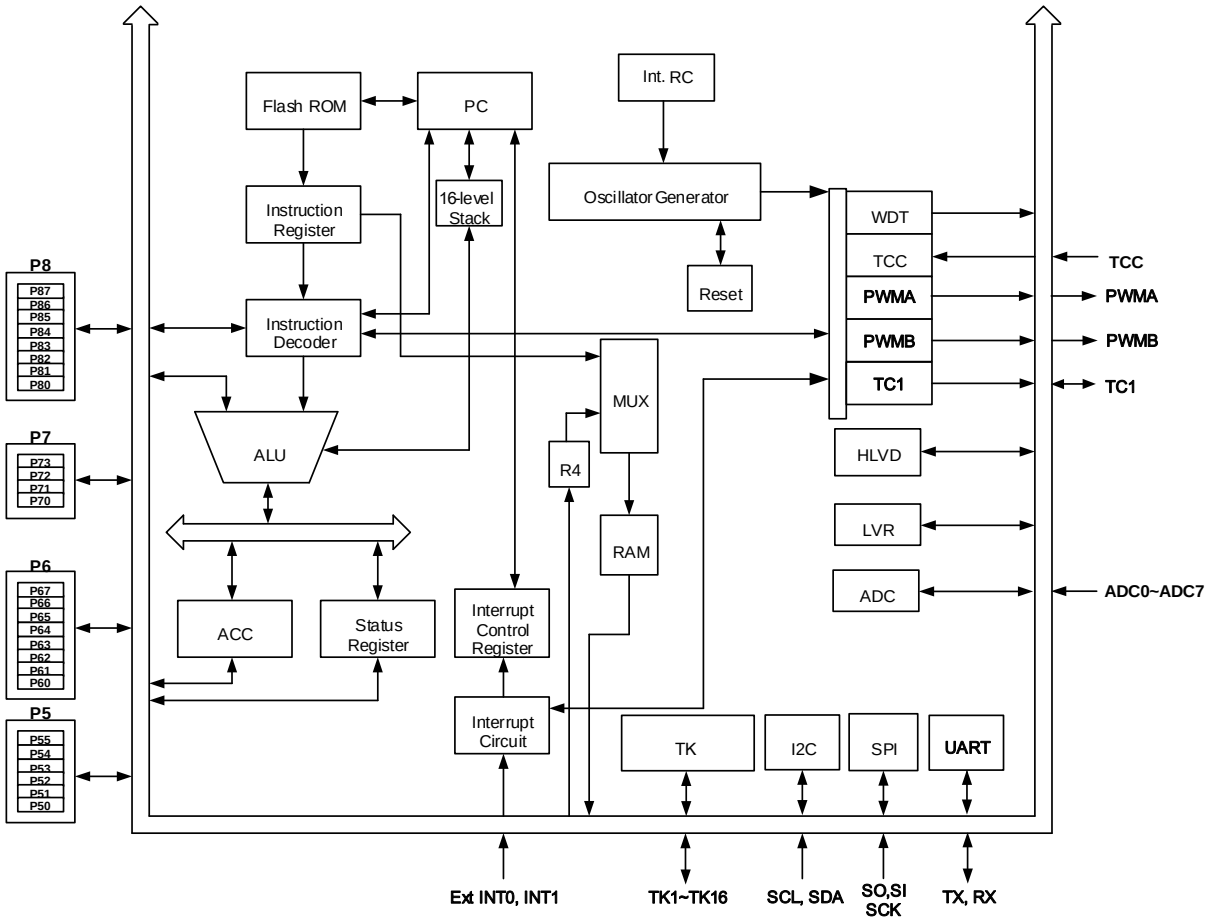


Figure 5-1 eKTF5616/08 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Selection Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SBS1	SBS0	-	-	GBS1	GBS0
0	0	R/W	R/W	0	0	R/W	R/W

Bits 7~6: Not used. Set to "0" all the time.

Bits 5~4 (SBS1~SBS0): Special register bank select bit. It is used to select Banks 0/1/2 of Special Registers **R5~R4F**.

SBS1	SBS0	Special Register Bank
0	**0**	0
0	**1**	1
1	**0**	2
1	**1**	X

Bit 3~2: Not used. Set to "0" all the time.

Bits 1~0 (GBS1~GBS0): General register bank select bit. It is used to select Banks 0~3 of General Registers **R80~RFF**.

GBS1	GBS0	RAM Bank
0	**0**	0
0	**1**	1
1	**0**	2
1	**1**	3

6.1.3 R2: PCL (Program Counter Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PC7~PC0): The low byte of program counter.

- Depending on the device type, R2 and hardware stack are 16-bits wide. The structure is depicted in Figure 6-1 *eKTF5616/08 Program Counter Organization*.
- Generating 4K×16 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "0"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will add 1 and is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC won't be changed.
- Any instruction except "ADD R2,A" that is written to R2 (e.g. "MOV R2, A", "BC R2, 6","INC R2",···) will cause the ninth bit and the above bits (PC8~PC12) of the PC not change.
- All instructions are single instruction cycle (Fsys/2).

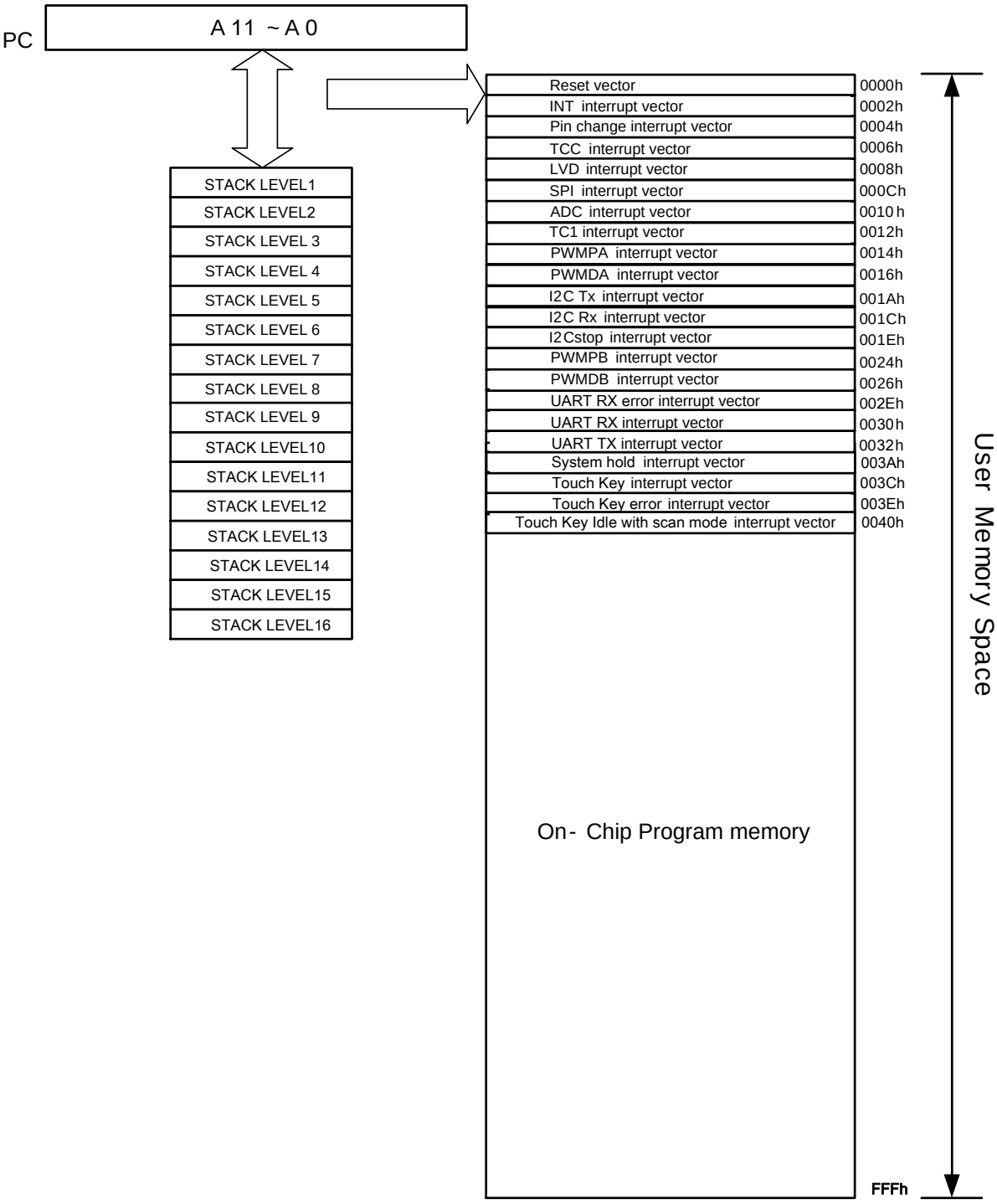


Figure 6-1 eKTF5616/08 Program Counter Organization

■ Data Memory Configuration

Address	SBANK 0	SBANK 1	SBANK 2
0X00	IAR (Indirect Addressing Reg.)		
0X01	BSR (Bank Selection Control Reg.)		
0X02	PCL (Program Counter Low)		
0X03	SR (Status Reg.)		
0X04	RSR (RAM Selection Reg.)		
0X05	Port 5	IOCR8	TKAPC
0X06	Port 6	Unused	TKBPC
0X07	Port 7	Unused	TKASCR
0X08	Port 8	P5PHCR	TKBSCR
0X09	Unused	P6PHCR	Unused
0X0A	Unused	P78PHCR	Unused
0x0B	IOCR5	P5PLCR	Unused
0X0C	IOCR6	P6PLCR	Unused
0X0D	IOCR7	P78PLCR	TKCR
0X0E	OMCR	P5HDSCR	TKCCR
0X0F	EIESCR	P6HDSCR	TKCSR
0X10	WUCR1	P789AHDSCR	TKCTR
0X11	WUCR2	P5ODCR	TKSWR
0X12	WUCR3	P6ODCR	TKAH
0X13	Unused	P78ODCR	TKAL
0X14	SFR1	Unused	TKBH
0X15	SFR2	Unused	TKBL
0X16	SFR3	PWMSCR	TKSCR
0X17	SFR4	PWMACR	TKA1WBH
0X18	Unused	PRDAL	TKA1WBL
0X19	SFR6	PRDAH	TKA1WR
0X1A	Unused	DTAL	TKA2WBH
0X1B	IMR1	DTAH	TKA2WBL
0X1C	IMR2	TMRAL	TKA2WR
0X1D	IMR3	TMRAH	TKB1WBH
0X1E	IMR4	PWMBCR	TKB1WBL
0X1F	Unused	PRDBL	TKB1WR
0X20	IMR6	PRDBH	TKB2WBH
0X21	WDTCR	DTBL	TKB2WBL
0X22	TCCCR	DTBH	TKB2WR
0X23	TCCD	TMRBL	Unused

Address	SBANK 0	SBANK 1	SBANK 2
0X24	TC1CR1	TMRBH	Unused
0X25	TC1CR2	Unused	Unused
0X26	TC1DA	Unused	Unused
0X27	TC1DB	Unused	Unused
0X28	Unused	Unused	Unused
0X29	Unused	Unused	Unused
0X2A	Unused	Unused	Unused
0x2B	Unused	Unused	Unused
0X2C	Unused	Unused	Unused
0X2D	Unused	Unused	Unused
0X2E	Unused	Unused	Unused
0X2F	Unused	Unused	Unused
0X30	I2CCR1	Unused	Unused
0X31	I2CCR2	Unused	Unused
0X32	I2CSA	Unused	Unused
0X33	I2CDB	URCR	Unused
0X34	I2CDAL	URS	Unused
0X35	I2CDAH	URTD	Unused
0X36	SPICR	URRDL	Unused
0X37	SPIS	URRDH	Unused
0X38	SPIR	Unused	Unused
0X39	SPIW	Unused	Unused
0X3A	Unused	Unused	Unused
0x3B	Unused	Unused	Unused
0X3C	Unused	Unused	Unused
0X3D	Unused	Unused	Unused
0X3E	ADCR1	Unused	Unused
0X3F	ADCR2	Unused	Unused
0X40	ADISR	EECR1	Unused
0X41	ADER1	EECR2	Unused
0X42	Unused	EERA	Unused
0X43	ADDL	EERD	Unused
0X44	ADDH	FLKR	Unused
0X45	ADCVL	TBPTL	Unused
0X46	ADCVH	TBPTH	Unused
0X47	Unused	STKMON	LOCKPR
0X48	Unused	PCH	LOCKCR

Address	SBANK 0	SBANK 1	SBANK 2
0X49	Unused	HLVDCR	Unused
0X4A	Unused	Unused	Unused
0x4B	Unused	Unused	Unused
0X4C	Unused	Unused	Unused
0X4D	Unused	TBWCR	Unused
0X4E	Unused	TBWAL	Unused
0X4F	Unused	TBWAH	Unused
0X50	**GENERAL PURPOSE REGISTER**		
0X51			
.			
.			
0X7F			
0X80	GBANK 0	GBANK 1	GBANK 2	GBANK 3
0X81				
.				
.				
.				
0XFE				
0XFF				

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	N	OV	T	P	Z	DC	C
F	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/RETI instructions

Bit 6 (N): Negative flag.

The negative flag stores the state of the most significant bit of the output result

0: The result of the operation is not negative.

1: The result of the operation is negative.

Bit 5 (OV): Overflow flag.

OV is set when a two's complement overflows occurs as a result of an operation

0: No overflow occurred.

1: Overflow occurred.

Bit 4 (T): Time-out bit.

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT time-out.

Bit 3 (P): Power down bit.

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry or Borrow flag

C : C is set when a carry occurs and cleared when a borrow occurs during an arithmetic operation. The Carry Flag bit is set or cleared, depending on the operation that is performed.

For ADD, ADC, INC, INCA instructions

0: No carry occurs.

1: Carry occurs.

For SUB, SUBB, DEC, DECA, NEG instructions

0: Borrow occurs.

1: No borrow occurs.

For RLC, RRC, RLCA, RRCA instructions

The Carry flag is used as a link between the least significant bit (LSB) and the most significant bit (MSB).

6.1.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (RSR7~RSR0): These bits are used to select registers (Address 00 ~ FF) in indirect addressing mode. For more details, refer to the table on Data Memory Configuration in Section 6.1.3, *R2: PCL (Program Counter Low)*.

6.1.6 Bank 0 R5 ~ R8: (Port 5 ~ Port 8)

R5, R6, R7, and R8 are I/O data registers.

6.1.7 Bank 0 R9 ~ RA: (Reserved)

6.1.8 Bank 0 RB~RD: (IOCR5 ~ IOCR7)

These registers are used to control the I/O port direction. They are both readable and writable.

0: Set the relative I/O pin as output

1: Set the relative I/O pin into high impedance

6.1.9 Bank 0 RE: OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	PERCS	-	FMSF	-	RCM1	RCM0
R/W	R/W	R/W	-	R	-	R/W	R/W

Bit 7 (CPUS): CPU Oscillator Source Select.

0: Fs: sub-oscillator

1: Fm: main-oscillator (default)

When CPUS=0, the CPU oscillator select sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit will decide SLEP instruction which mode to go.

0: "IDLE=0"+SLEP instruction → sleep mode

1: "IDLE=1"+SLEP instruction → idle mode (default)

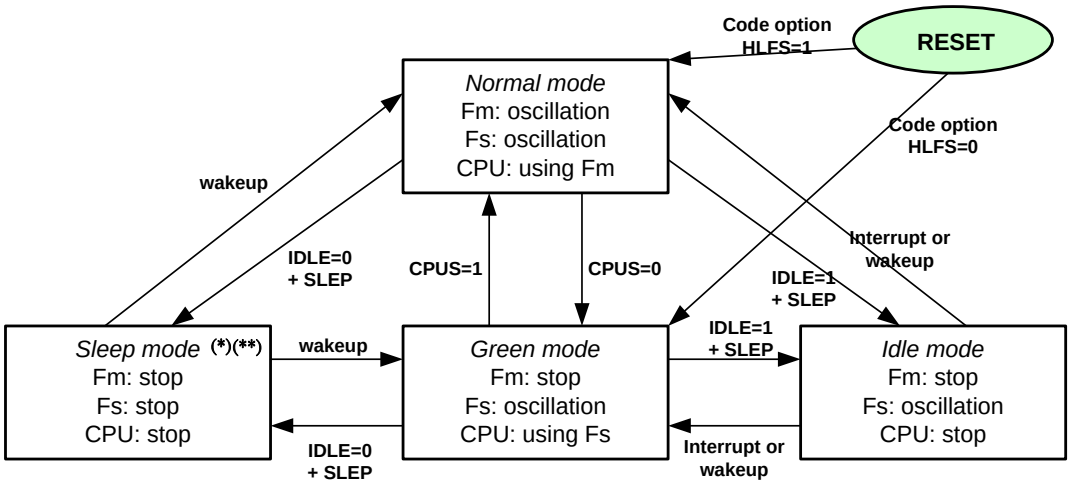


Figure 6-2 CPU Operation Mode

Note

(*)

If Watchdog function is enabled before entering into sleep mode, some circuits, such as timer (Its clock source is Fs) must stop counting.

If Watchdog function is enabled before entering into sleep mode, some circuits, such as timer (Its clock source is external pin) can still count and its interrupt flag can be active at matching condition as corresponding interrupt is enabled. But CPU cannot be woken up by this event.

(**)

Switching Operation Mode at sleep → Normal, Green → Normal:

If the clock source of the timer is Fm, the timer/counter must stop counting at sleep or green mode. Then, timer can continue to count until clock source is stable at normal mode. A stable clock source means CPU starts to work at normal mode.

Switching Operation Mode at Sleep → green:

If the clock source of the timer is Fs, the timer must stop counting at sleep mode. Then, the timer can continue to count until the clock source is stable at green mode. A stable clock source means that CPU starts to work at green mode.

Switching Operation Mode at Sleep → Normal:

If the clock source of the Timer is Fs, the timer must stop counting at sleep mode. Then, the timer can continue to count until the clock source is stable at normal mode. A stable clock source means that CPU starts to work at normal mode.

CPU mode switch	IRC Frequency	POR/LVR	Waiting time before CPU starting to work	
			PERCS = 1	PERCS = 0
Sleep -> Normal Idle -> Normal Green -> Normal	12M, 16M	16ms + WSTO + 32 clocks (main frequency)	32 clocks (main frequency)	WSTO + 32 clocks (main frequency)
	8M	16ms + WSTO + 8/32 clocks (main frequency)	8/32 clocks (main frequency)	WSTO + 8/32 clocks (main frequency)
Sleep -> Green Idle -> Green	32KHz	16ms + WSTO + 8 clocks (sub frequency)	WSTO + 8 clocks (sub frequency)	WSTO + 8 clocks (sub frequency)

WSTO: Waiting time of Start-to-Oscillation

Bit 5 (PERCS): Periphery Clock Source for Green and Idle modes.

0: Periphery Clock Source is Fs. Fm will be Stop into Green and Idle modes. (default)

1: Periphery Clock Source is Fm. Fm will be oscillation into Green and Idle modes.

Bits 4,2: Not used, set to “0” all the time

Bit 3 (FMSF): Fm Stable Flag bit.

0: Indicate that the frequency is unstable.

1: Indicate that the frequency has stabilized.

Bits 1~0 (RCM1~RCM0): Internal RC mode selection bits

*Default value corresponding code option Word1 RCM1~RCM0

*RCM1	*RCM0	Frequency (MHz)
0	0	NA
0	1	8
1	0	12*
1	1	16

***OCDS simulation 12MHz need select other frequency first, then set RCM1~RCM0 change to 12MHz**

6.1.10 Bank 0 RF: EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EIES1	EIES0	-	-
-	-	-	-	R/W	R/W	-	-

Bits 7~4: Not used, set to "0" all the time

Bits 3~2 (EIES1~0): external interrupt edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

Bits 1~0: Not used, set to "0" all the time

6.1.11 Bank 0 R10: WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	LVDWK	ADWK	INTWK1	INTWK0	-	-
-	-	R/W	R/W	R/W	R/W	-	-

Bits 7~6: Not used, set to “0” all the time

Bit 5 (LVDWK): Low Voltage Detect Wake-up Enable Bit

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

Bit 4 (ADWK): A/D Converter Wake-up Function Enable Bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

When the AD Complete status is used to enter interrupt vector or to wake up IC from sleep/idle with AD conversion running, the ADWK bit must be set to “enable”.

Bits 3~2 (INTWK1~0): External Interrupt (INT pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status changed is used to enter interrupt vector or to wake up IC from Sleep/Idle, the INTWK bits must be set to “enable”.

Bits 1~0: Not used, set to “0” all the time

6.1.12 Bank 0 R11: WUCR2 (Wake-up Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	SPIWK	I2CWK	-	-
-	-	-	-	R/W	R/W	-	-

Bits 7~4: Not used. Set to "**0**" all the time.

Bit 3 (SPIWK): SPI wake-up enable bit. Applicable when SPI works in Slave mode.

0: Disable SPI wake-up

1: Enable SPI wake-up

Bit 2 (I2CWK): I^2C wake-up enable bit. Applicable when I^2C works in Slave mode.

0: Disable I^2C wake-up

1: Enable I^2C wake-up

NOTE

When I^2C is in Slave mode, it cannot communicate with the MCU in Green mode. At the same time, the SCL in on hold and kept at low level when the MCU is in Green mode. SCL is released when the MCU switches to Normal mode.

Bits 1~0: Not used. Set to "**0**" all the time.

6.1.13 Bank 0 R12: WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICWKP8	ICWKP7	ICWKP6	ICWKP5	-	-	-	-
R/W	R/W	R/W	R/W	-	-	-	-

Bits 7~4 (ICWKP8~ICWKP5): Pin change Wake-up enable for Ports 8/7/6/5.

0: Disable wake-up function

1: Enable wake-up function

Bits 3~0: Not used. Set to "**0**" all the time.

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Pin Change INT	ICWKPx = 0, PxICIE = 0	Wake-up is invalid				Interrupt is invalid			
	ICWKPx = 0, PxICIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWKPx = 1, PxICIE = 0	Wake-up + Next Instruction				Interrupt is invalid			
	ICWKPx = 1, PxICIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

NOTE

*When the MCU wakes up from Sleep or Idle mode, the ICSF must equal to **1**. If ICSF is equal to **0**, it means the pin status does not change or the pin change ICIE is disabled. Hence the MCU cannot wake-up.*

6.1.14 Bank 0 R13: (Reserved)

6.1.15 Bank 0 R14: SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	LVDSF	ADSF	EXSF1	EXSF0	-	TCSF
-	-	F	F	F	F	-	F

Each corresponding status flag is set to "1" when interrupt condition is triggered.

Bits 7~6, 1: Not used, set to "0" all the time

Bit 5 (LVDSF): Low Voltage Detector status flag

Bit 4 (ADSF): Analog to digital conversion interrupt status flag. Set when AD conversion is completed. Reset by software.

Bits 3~2 (EXSF1~0): External interrupt status flag.

Bit 0 (TCSF): TCC overflow status flag. Set when TCC overflows, reset by software.

NOTE

If a function is enabled, the corresponding status flag would be active regardless of whether the interrupt mask is enabled or not.

6.1.16 Bank 0 R15: SFR2 (Status Flag Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	UERRSF	URSF	UTSF	-	-	TC1SF
-	-	F	F	F	-	-	F

Bits 7~6: Not used, set to "0" all the time

Bit 5 (UERRSF): UART receiving error status flag, cleared by software or UART disable.

Bit 4 (URSF): UART receive mode data buffer full status flag, cleared by software.

Bit 3 (UTSF): UART transmit mode data buffer empty flag, cleared by software.

Bits 2~1: Not used, set to "0" all the time

Bit 0 (TC1SF): 8-bit timer/counter 1 status flag, cleared by software.

6.1.17 Bank 0 R16: SFR3 (Status Flag Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PWMBPSF	PWMBDSF	PWMAPSF	PWMADSF
-	-	-	-	F	F	F	F

Bits 7~4: Not used, set to "0" all the time

Bit 3 (PWMBPSF): Status flag of period-matching for PWMB (Pulse Width Modulation). Set when a selected period is reached, reset by software.

Bit 2 (PWMBDSF): Status flag of duty-matching for PWMB (Pulse Width Modulation). Set when a selected duty is reached, reset by software.

Bit 1 (PWMAPSF): Status flag of period-matching for PWMA (Pulse Width Modulation). Set when a selected period is reached, reset by software.

Bit 0 (PWMADSF): Status flag of duty-matching for PWMA (Pulse Width Modulation). Set when a selected duty is reached, reset by software.

NOTE

If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.

6.1.18 Bank 0 R17: SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICSF	P7ICSF	P6ICSF	P5ICSF	SPISF	I2CSTPSF	I2CRSF	I2CTSF
F	F	F	F	F	F	F	F

Bits 7~4 (P8ICSF~P5ICSF): Ports 5~8 input status change status flag. Set when Ports 5~8 input changes. Reset by software.

Bit 3 (SPISF): SPI mode status flag. Flag is cleared by software.

Bit 2 (I2CSTPSF): I^2C stop status flag. Set when I^2C stop signal occurs.

Bit 1 (I2CRSF): I^2C receive status flag. Set when I^2C receives 1byte data and responds to ACK signal. Reset by firmware or I^2C disable.

Bit 0 (I2CTSF): I^2C transmit status flag. Set when I^2C transmits a 1 byte data and receives a handshake signal (ACK or NACK). Reset by firmware or I^2C disable.

NOTE

If a function is enabled, the corresponding status flag will be active regardless of whether the interrupt mask is enabled or not.

6.1.19 Bank 0 R18: (Reserved)

6.1.20 Bank 0 R19: SFR6 (Status Flag Register 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHSF	-	-	TKTOSF	TKCSF	TKPESF	TKOESF	TKSF
F	-	-	F	F	F	F	F

Bit 7 (SHSF): System hold status flag, Set when system hold occur, reset by software.

Bits 6~5: Not used, set to "0" all the time

Bit 4 (TKTOSF): Touch Key idle with scan mode time out status flag. Set when Touch Key idle with scan mode threshold compare condition dissatisfied and continued for 16 times, reset by software.

Bit 3 (TKCSF): Touch Key Compare status flag. Set when Touch Key idle with scan mode threshold compare conditions are satisfied, reset by software.

Bit 2 (TKPESF): Touch Key period Error status flag. Set when Touch Key period falls early, reset by software

Bit 1 (TKOESF): Touch Key Counter Overflow Error status flag. Set when Touch Key timer overflows, reset by software

Bit 0 (TKSF): Status flag for Touch Key Conversion. Set when Touch Key conversion is completed, reset by software (except idle with scan mode condition)

6.1.21 Bank 0 R1A: (Reserved)

6.1.22 Bank 0 R1B: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	LVDIE	ADIE	EXIE1	EXIE0	-	TCIE
-	-	R/W	R/W	R/W	R/W	-	R/W

Bits 7~6, 1: Not used, set to "0" all the time.

Bit 5 (LVDIE): LVDSF interrupt enable bit.

0: Disable LVDSF interrupt

1: Enable LVDSF interrupt

Bit 4 (ADIE): ADSF interrupt enable bit.

0: Disable ADSF interrupt

1: Enable ADSF interrupt.

Bit 3 (EXIE1): EXSF1 interrupt enable and **/INT1 function enable bit.**

0: P55/INT1/SCL1/OSCO is P55/SCL1/OSCO pin, EXSF1 always equals 0.

1: Enable EXSF1 interrupt and P55/INT1/SCL1/OSCO is /INT1 pin

Bit 2 (EXIE0): EXSF0 interrupt enable and **/INT0 function enable bit.**

0: P54/INT0/SDA1 is P54/SDA1 pin, EXSF0 always equals 0.

1: Enable EXSF0 interrupt and P54/INT0/SDA1 is /INT0 pin

Bit 0 (TCIE): TCSF interrupt enable bit.

0: Disable TCSF interrupt

1: Enable TCSF interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.23 Bank 0 R1C: IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	UERRIE	URIE	UTIE	-	-	TC1IE
-	-	R/W	R/W	R/W	-	-	R/W

Bits 7~6: Not used, set to "0" all the time.

Bit 5 (UERRIE): UART receive error interrupt enable bit.

0: Disable UERRSF interrupt

1: Enable UERRSF interrupt

Bit 4 (URIE): UART receive mode Interrupt enable bit.

0: Disable URSF interrupt

1: Enable URSF interrupt

Bit 3 (UTIE): UART transmit mode interrupt enable bit.

0: Disable UTSF interrupt

1: Enable UTSF interrupt

Bits 2~1: Not used, set to "0" all the time.

Bit 0 (TC1IE): Interrupt enable bit.

0: Disable TC1SF interrupt

1: Enable TC1SF interrupt

6.1.24 Bank 0 R1D: IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time.

Bit 3 (PWMBPIE): PWMBPSF interrupt enable bit.

0: Disable period-matching of PWMB interrupt

1: Enable period-matching of PWMB interrupt

Bit 2 (PWMBDIE): PWMBDSF interrupt enable bit.

0: Disable duty-matching of PWMB interrupt

1: Enable duty-matching of PWMB interrupt

Bit 1 (PWMAPIE): PWMAPSF interrupt enable bit.

0: Disable period-matching of PWMA interrupt

1: Enable period-matching of PWMA interrupt

Bit 0 (PWMADIE): PWMADSF interrupt enable bit.

0: Disable duty-matching of PWMA interrupt

1: Enable duty-matching of PWMA interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.25 Bank 0 R1E: IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICIE	P7ICIE	P6ICIE	P5ICIE	SPIIE	I2CSTPIE	I2CRIE	I2CTIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~4 (P8ICIE~P5ICIE): PxICSF interrupt enable bit

0: Disable PxICSF interrupt

1: Enable PxICSF interrupt

Bit 3 (SPIIE): Interrupt enable bit

0: Disable SPSF interrupt

1: Enable SPSF interrupt

Bit 2 (I2CSTPIE): I^2C stop interrupt enable bit.

0: Disable interrupt

1: Enable interrupt

Bit 1 (I2CRIE): I^2C Interface Rx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

Bit 0 (I2CTIE): I^{2}C Interface Tx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.26 Bank 0 R1F: (Reserved)

6.1.27 Bank 0 R20: IMR6 (Interrupt Mask Register 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHIE	-	-	-	TKCIE	-	TKERRIE	TKIE
R/W	-	-	-	R/W	-	R/W	R/W

Bit 7 (SHIE): SHSF Interrupt Enable Bit.

0: Disable SHSF interrupt

1: Enable SHSF interrupt

Bits 6~4,2: Not used, set to "0" all the time.

Bit 3 (TKCIE): TKCSF/TKTOSF Interrupt Enable Bit.

0: Disable TKCSF/TKTOSF interrupt

1: Enable TKCSF/TKTOSF interrupt

Bit 1 (TKERRIE): TKPESF /TKOESF Interrupt Enable Bit.

0: Disable TKPESF /TKOESF interrupt

1: Enable TKPESF /TKOESF interrupt

Bit 0 (TKIE): TKIE Interrupt Enable Bit.

0: Disable TKSF interrupt

1: Enable TKSF interrupt

6.1.28 Bank 0 R21: WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	FSSF	-	-	PSWE	WPSR2	WPSR1	WPSR0
R/W	R	-	-	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer enable bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bit 6 (FSSF): Fs Stable Flag bit

1: Indicate that the frequency has stabilized.

0: Indicate that the frequency is unstable.

Bits 5~4: Not used. Set to "**0**" all the time.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1.

1: Prescaler enable bit. The WDT rate is set at Bits 2~0.

Bits 2~0 (WPSR2~WPSR0): WDT Prescaler bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.29 Bank 0 R22: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TCCS	-	-	PSTE	TPSR2	TPSR1	TPSR0
-	R/W	-	-	R/W	R/W	R/W	R/W

Bit 7: Not used. Set to "**0**" all the time.

Bit 6 (TCCS): TCC Clock Source select bit

0: Fs (sub clock)

1: Fm (main clock)

Bits 5~4: Not used. Set to "**0**" all the time.

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit. TCC rate is 1:1.

1: Prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bits 2~0 (TPSR2~TPSR0): TCC Prescaler Bits

TPSR2	TPSR1	TPSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.30 Bank 0 R23: TCCD (TCC Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TCC7~TCC0): TCC data

Counter is increased by the instruction cycle clock. Writable and readable as any other registers.

6.1.31 Bank 0 R24: TC1CR1 (Timer 1 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1S	TC1RC	TC1SS1	-	TC1FF	TC1MOS	TC1IS1	TC1IS0
R/W	R/W	R/W	-	R/W	R/W	R/W	R/W

Bit 7 (TC1S): Timer/Counter 1 Start Control Bit

0: Stop and clear counter (default)

1: Start

Bit 6 (TC1RC): Timer 1 Read Control Bit. To load current number of counter into TC1DB register. It's useful only in counter mode.

0: Disable function. When using capture mode, this bit must be set to "0" (default).

1: Enable function. The number of counting are loaded into TC1DB.

Bit 5 (TC1SS1): Timer/Counter 1 Clock Source Select Bit 1

0: Internal clock as count source (Fc)- Fs/Fm (default)

1: External TC1 pin as count source (Fc). It is used only for timer/counter mode.

Bit 4: Not used, set to "0" all the time.

Bit 3(TC1FF): Inversion for Timer/Counter 1 as PWM or PDO mode

0: Duty is Logic 1 (default)

1: Duty is Logic 0

Bit 2 (TC1MOS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One–shot mode

NOTE

One-shot mode means the timer only counts a cycle.

Bits 1~0 (TC1IS1~ TC1IS0): Timer 1 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode.

TC1IS1	TC1IS0	Timer 1 Interrupt Type Select
0	0	TC1DA(period) matching
0	1	TC1DB(duty) matching
1	x	TC1DA and TC1DB matching

6.1.32 Bank 0 R25: TC1CR2 (Timer 1 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (TC1M2~TC1M0): Timer/Counter 1 operation mode select.

TC1M2	TC1M1	TC1M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of clock source must be 50/50)

Bit 4 (TC1SS0): Timer/Counter 1 clock source selection bit

0: The Fs is used as count source (Fc) (default)

1: The Fm is used as count source (Fc)

Bits 3~0 (TC1CK3~TC1CK0): Timer/Counter 1 clock source prescaler select.

TC1CK3	TC1CK2	TC1CK1	TC1CK0	Clock Source	Resolution 8MHZ	Max time 8MHz	Resolution 16KHZ	Max time 16KHz
				Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	0	F_C	125ns	32us	62.5us	16ms
0	0	0	1	$F_C/2$	250ns	64us	125us	32ms
0	0	1	0	$F_C/2^2$	500ns	128us	250us	64ms
0	0	1	1	$F_C/2^3$	1us	256us	500us	128ms
0	1	0	0	$F_C/2^4$	2us	512us	1ms	256ms
0	1	0	1	$F_C/2^5$	4us	1024us	2ms	512ms
0	1	1	0	$F_C/2^6$	8us	2048us	4ms	1024ms
0	1	1	1	$F_C/2^7$	16us	4096us	8ms	2048ms
1	0	0	0	$F_C/2^8$	32us	8192us	16ms	4096ms
1	0	0	1	$F_C/2^9$	64us	16384us	32ms	8192ms
1	0	1	0	$F_C/2^{10}$	128us	32768us	64ms	16384ms
1	0	1	1	$F_C/2^{11}$	256us	65536us	128ms	32768ms
1	1	0	0	$F_C/2^{12}$	512us	131072us	256ms	65536ms
1	1	0	1	$F_C/2^{13}$	1.024ms	262144us	512ms	131072ms
1	1	1	0	$F_C/2^{14}$	2.048ms	524.288ms	1.024s	262144ms
1	1	1	1	$F_C/2^{15}$	4.096ms	1.048s	2.048s	524288ms

6.1.33 Bank 0 R26: TC1DA (Timer/Counter 1 DATA Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC1DA7~TC1DA0): Data buffer A of 8 bit Timer/Counter 1

6.1.34 Bank 0 R27: TC1DB (Timer/Counter 1 DATA Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC1DB7~TC1DB0): Data Buffer B of 8 bit Timer/Counter 1

NOTE

1. *When Timer/Counter x is used as PWM mode, the duty value stored at register TCxDB must be less than or equal to the period value stored at register TCxDA. i.e., duty ≦ period. And then the PWM waveform is generated. If duty value is greater than period value, the PWM output waveform will be kept at **high** voltage levels.*
2. *The period value set by users is extra plus 1 in inner circuit.*

   For example:

   The period value is set as 0x4F, the circuit actually processes 0x50 period length.

   The period value is set as 0xFF, the circuit actually processes 0x100 period length.

6.1.35 Bank 0 R28 ~ R2F: (Reserved)

6.1.36 Bank 0 R30: I2CCR1 (I2C Status and Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
R/W	R/W	R/W	R/W	R	R	R	R

Bit 7 (Strobe/Pend): In Master mode, it is used as strobe signal to control I^2C circuit in sending SCL clock. Automatically reset after receiving or transmitting handshake signal (ACK or NACK). In Slave mode, it is used as pending signal. User should clear it after writing data into Tx buffer or taking data from Rx buffer to inform Slave I^2C circuit to release SCL signal.

Bit 6 (IMS): I^2C Master/Slave mode select bit
0: Slave (Default)
1: Master

Bit 5 (ISS): I^2C C Fast/Standard mode select bit (if Fm is 4 MHz and I2CTS1~0<0,0>)
0: Standard mode (100K bit/s)
1: Fast mode (400K bit/s)

Bit 4 (STOP): In Master mode, if STOP=1 and R/nW=1, then MCU must return nACK signal to Slave device before sending STOP signal. If STOP=1 and R/nW=0, then MCU sends STOP signal after receiving an ACK signal. MCU resets when it sends STOP signal to Slave device.
In Slave mode, if STOP=1 and R/nW=0, then MCU must return nACK signal to Master device.

Bit 3 (SAR_EMPTY): Set when MCU transmits 1 byte data from I^2C Slave Address Register and receive ACK (or nACK) signal. Reset when MCU writes 1 byte data to I^2C Slave Address Register.

Bit 2 (ACK): The ACK condition bit is set to 1 by hardware when the device responds with an acknowledge (ACK). Reset when the device responds with a not-acknowledge (nACK) signal.

Bit 1 (FULL): Set by hardware when I^2C Receive Buffer register is full. Reset by hardware when the MCU reads data from the I^2C Receive Buffer register.

Bit 0 (EMPTY): Set by hardware when I^2C Transmit Buffer register is empty and ACK (or nACK) signal is received. Reset by hardware when the MCU writes new data into the I^2C Transmit Buffer register.

6.1.37 Bank 0 R31: I2CCR2 (I2C Status and Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CBF	GCEN	I2COPT	BBF	-	I2CTS1	I2CTS0	I2CEN
R	R/W	R/W	R	-	R/W	R/W	R/W

Bit 7 (I2CBF): I2C Busy Flag Bit

0: clear to "0" in Slave mode, if receives a STOP signal or when I2C slave address does not match.

1: set when I2C communicate with master in slave mode.

*Set when STAR signal, clear when I2C disable or STOP signal for Slave mode.

Bit 6 (GCEN): I2C General Call Function Enable Bit

0: Disable General Call Function

1: Enable General Call Function

Bit 5 (I2COPT): I2C pin optional bit. It is used to switch the pin position of I2C function.

0: Placed I2C pins in P52 (SDA0) and P53 (SCL0).

1: Placed I2C pins in P54 (SDA1) and P55 (SCL1).

*Default value corresponding code option Word 2 I2COPT

Bit 4 (BBF): Busy Flag Bit. I2C detection is busy in the master mode. Read only.

*Set when STAR signal, clear when STOP signal for Master mode.

Bit 3: Not used, set to "0" all the time.

Bits 2~1 (I2CTS1~I2CTS0): I2C Transmit Clock Select Bits. When using different operating frequency (Fm), these bits must be set correctly to let SCL clock fill in with standard/fast mode.

I2CCR1 Bit 5=1, Fast Mode

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/10	4
0	1	Fm/20	8
1	0	Fm/30	12
1	1	Fm/40	16

I2CCR1 Bit 5=0, Standard Mode

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/40	4
0	1	Fm/80	8
1	0	Fm/120	12
1	1	Fm/160	16

Bit 0 (I2CEN): I2C Enable Bit

0: Disable I2C mode (Default)

1: Enable I2C mode

6.1.38 Bank 0 R32: I2CSA (I2C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~1 (SA6~SA0): When the MCU is used as Master device for I^2C application, these bits are the Slave Device Address register.

Bit 0 (IRW): When the MCU is used as Master device for I^2C application, this bit is Read/Write transaction control bit.

0: Write

1: Read

6.1.39 Bank 0 R33: I2CDB (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DB7~DB0): I^2C Receive/Transmit Data Buffer

6.1.40 Bank 0 R34: I2CDAL (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DA7~DA0): When the MCU is used as Slave device for I^2C application, this register stores the MCU address. It is used to identify the data on the I^2C bus to extract the message delivered to the MCU.

NOTE

Slave Address 0x77 is reserved for WTR use.

6.1.41 Bank 0 R35: I2CDAH (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	DA9	DA8
-	-	-	-	-	-	R/W	R/W

Bits 7~2: Not used. Set to "**0**" all the time.

Bits 1~0 (DA9~DA8): Device Address bits

6.1.42 Bank 0 R36: SPICR (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

Bit 7 (CES): Clock Edge Select bit

0: Data shift out on a rising edge, and shift in on a falling edge. Data is on hold during a low-level.

1: Data shift out on a falling edge, and shift in on a rising edge. Data is on hold during a high-level.

Bit 6 (SPIE): SPI Enable bit

0: Disable SPI mode

1: Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0: No overflow

1: A new data is received while the previous data is still being held in the SPIR register. Under this condition, the data in the SPIS register is destroyed. To avoid setting this bit, user should read the SPIR register although only transmission is implemented. This can only occur in Slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0: Reset as soon as the shifting is completed, and the next byte is read to shift.

1: Start to shift, and it remains at "**1**" while the current byte is still being transmitted.

Bit 3 (SDOC): SDO Output Status Control bit

0: After serial data output, the SDO remains high

1: After serial data output, the SDO remains low

Bits 2~0 (SBRS2~SBRS0): SPI Baud Rate Select bits

SBRS2	SBRS1	SBRS0	Mode	SPI Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Fosc/64
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

6.1.43 Bank 0 R37: SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	-	OD3	OD4	-	RBF
R/W	R/W	R/W	-	R/W	R/W	-	R

Bit 7 (DORD): Data shift type control bit

0: Shift left (MSB first)

1: Shift right (LSB first)

Bits 6~5 (TD1~TD0): SDO status output delay time options (Normal mode only). When the CPU oscillator source uses Fs, it will result in 1 CLK delay time.

NOTE

TD1~TD0 bits are applicable only to Normal mode → Normal mode. If under Sleep mode → Normal mode condition, then Wake-up time is "Warm up time + 1CLK".

TD1	TD0	Delay Time
0	**0**	8 CLK
0	**1**	16 CLK
1	**0**	24 CLK
1	**1**	32 CLK

Bit 4: Not used. Set to "**0**" all the time.

Bit 3 (OD3): Open-drain control bit

0: Open-drain disabled for SDO

1: Open-drain enabled for SDO

Bit 2 (OD4): Open-drain control bit

0: Open-drain disabled for SCK

1: Open-drain enabled for SCK

Bit 1: Not used. Set to "**0**" all the time.

Bit 0 (RBF): Read Buffer Full flag

0: Receiving is not completed, and SPIR has not fully exchanged data.

1: Receiving is completed, and SPIR has fully exchanged data.

6.1.44 Bank 0 R38: SPIR (SPI Read Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
R	R	R	R	R	R	R	R

Bits 7~0 (SRB7~SRB0): SPI Read Data Buffer

6.1.45 Bank 0 R39: SPIW (SPI Write Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (SWB7~SWB0): SPI Write Data Buffer

6.1.46 Bank 0 R3A ~ R3D: (Reserved)

6.1.47 Bank 0 R3E: ADCR1 (ADC Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (CKR2~0): Clock Rate Selection of ADC

System Mode	CKR2~0	Clock Rate	Max. System Operation Frequency in 2.2~2.5V	Max. System Operation Frequency in 2.5~3V	Max. System Operation Frequency in 3~5.5V
Normal Mode	000	$F_{Main}/4$	-	-	-
	001	$F_{Main}/8$	-	-	8 MHz
	010	$F_{Main}/16$	-	-	16 MHz
	011	$F_{Main}/32$	-	8 MHz	16 MHz
	100	$F_{Main}/64$	-	12 MHz	16 MHz
	101	$F_{Main}/128$	-	16 MHz	16 MHz
	110	$F_{Main}/256$	8 MHz	16 MHz	16 MHz
	111	F_{Sub}	Fs	Fs	Fs
Green Mode	xxx	F_{Sub}	Fs	Fs	Fs

Bit 4 (ADRUN): ADC Starts to Run

In single mode:

0: Reset on completion of the conversion by hardware, this bit cannot be reset by software.

1: A/D conversion starts. This bit can be set by software

In continuous mode:

0: ADC is stopped.

1: ADC is running unless this bit is reset by software

Bit 3 (ADP): ADC Power

0: ADC is in power down mode.

1: ADC is operating normally.

Bit 2 (ADOM): ADC Operation Mode Selection

0: ADC operates in single mode.

1: ADC operates in continuous mode.

Bits 1~0 (SHS1~0): Sample and Hold Timing Selection

SHS[1:0]	Sample and Hold Timing
00	2 x T_{AD}
01	4 x T_{AD}
10	8 x T_{AD}
11	12 x T_{AD}

6.1.48 Bank 0 R3F: ADCR2 (ADC Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	VPIS2	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
-	R/W	R/W	R/W	R/W	R/W	R/W	-

Bit 7: Not used, set to "0" all the time.

Bit 5 (ADIM): ADC Interrupt Mode

0: Normal mode. Interrupt occurred after AD conversion is completed.

1: Compare mode. Interrupt occurred when comparison result conforms the setting of ADCMS bits.

Bit 4 (ADCMS): ADC Comparison Mode Selection.

In compare mode:

0: Interrupt occurred when AD conversion data is greater than data in ADCD register.

It means when ADD > ADCD, interrupt occurred.

1: Interrupt occurred when AD conversion data is less than data in ADCD register.

It means when ADD < ADCD, interrupt occurred.

In normal mode:

No effect

Bits 6, 3 ~ 2 (VPIS2~0): Internal Positive Reference Voltage Selection.

VPIS[2]	VPIS[1:0]	Reference Voltage
0	00	AVDD
0	01	4 V
0	10	3 V
0	11	2.5 V
1	XX	2 V

Bit 1 (VREFP): Positive Reference Voltage Selection

0: Internal positive reference voltage. The actual voltage is set by VPIS[1:0] bits

1: From VREF pin.

Bit 0: Not used, set to "0" all the time.

NOTE

When using internal voltage reference and the code option word2<7> is set to "0", users need to wait at least 50us the first time to enable and stabilize the internal voltage reference circuit. After that, users only need to wait ~~at least~~ 6us whenever switching voltage references.

6.1.49 Bank 0 R40: ADISR (Analog to Digital Converter Input Channel Selection Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	ADIS3	ADIS2	ADIS1	ADIS0
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time.

Bits 3~0 (ADIS4~0): ADC input channel selection bits

ADIS[3:0]	Selected Channel
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5
0110	ADC6
0111	ADC7
1xxx*	1/2 VDD PowerDet.

Note:

*: For internal signal source use. Users only need to set ADIS3=1, these AD input channels will be active instantly, internal Vref stable time = 4 μs.

6.1.50 Bank 0 R41: ADER1 (Analog to Digital Converter Input Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (ADE7): AD converter enable bit of P87 pin.

0: Disable ADC7, P87/ADC7 act as I/O pin

1: Enable ADC7, act as analog input pin.

Bit 6 (ADE6): AD converter enable bit of P86 pin.

0: Disable ADC6, P86/ADC6 act as I/O pin

1: Enable ADC6, act as analog input pin

Bit 5 (ADE5): AD converter enable bit of P85 pin.

0: Disable ADC5, P85/ADC5 act as I/O pin

1: Enable ADC5, act as analog input pin

Bit 4 (ADE4): AD converter enable bit of P84 pin.

0: Disable ADC4, P84/VREF/ADC4 act as I/O or VREF pin

1: Enable ADC4, act as analog input pin

Bit 3 (ADE3): AD converter enable bit of P83 pin.

0: Disable ADC3, P83/TK16/ADC3 act as I/O or TK16 pin

1: Enable ADC3, act as analog input pin

Bit 2 (ADE2): AD converter enable bit of P82 pin.

0: Disable ADC2, P82/TK15/ADC2 act as I/O or TK15 pin

1: Enable ADC2, act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P81 pin.

0: Disable ADC1, P81/TK14/ADC1/PWMB act as I/O or TK14/PWMB pin

1: Enable ADC1, act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P80 pin.

0: Disable ADC0, P80/TK13/ADC0/VREF/PWMA act as I/O or TK13/PWMA pin

1: Enable ADC0, act as analog input pin

6.1.51 Bank 0 R42: (Reserved)

6.1.52 Bank 0 R43: ADDL (Low Byte of Analog to Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
R	R	R	R	R	R	R	R

Bits 7~0 (ADD7~0): Low Byte of AD Data Buffer

6.1.53 Bank 0 R44: ADDH (High Byte of Analog to Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
R	R	R	R	R	R	R	R

Bits 7~0 (ADD11~4): High Byte of AD Data Buffer

6.1.54 Bank 0 R45: ADCVL (Low Byte of Analog to Digital Converter Comparison)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (ADCD7~0): Low Byte Data for AD Comparison.

User should use the data format the same as ADDH and ADDL register. Otherwise, inaccurate result will be obtained after AD comparison.

6.1.55 Bank 0 R46: ADCVH (High Byte of Analog to Digital Converter Comparison)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	ADCD11	ADCD10	ADCD9	ADCD8
-	-	-	-	R/W	R/W	R/W	R/W

Bits 3~0 (ADCD11~8): High Byte Data for AD Comparison

6.1.56 Bank 0 R47~4F: (Reserved)

6.1.57 Bank 1 R5: IOCR8

These registers are used to control I/O port direction. They are both readable and writable.

1: Put the relative I/O pin into high impedance

0: Put the relative I/O pin as output

6.1.58 Bank 1 R6 ~ R7: (Reserved)

6.1.59 Bank 1 R8: P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PH55	PH54	PH53	PH52	PH51	PH50
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used, set to "0" all the time.

Bit 5 (PH55): Control bit used to enable pull-high of the P55 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 4 (PH54): Control bit used to enable pull-high of the P54 pin

Bit 3 (PH53): Control bit used to enable pull-high of the P53 pin

Bit 2 (PH52): Control bit used to enable pull-high of the P52 pin

Bit 1 (PH51): Control bit used to enable pull-high of the P51 pin

Bit 0 (PH50): Control bit used to enable pull-high of the P50 pin

6.1.60 Bank 1 R9: P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PH67): Control bit used to enable pull-high of the P67 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (PH66): Control bit used to enable pull-high of the P66 pin

Bit 5 (PH65): Control bit used to enable pull-high of the P65 pin

Bit 4 (PH64): Control bit used to enable pull-high of the P64 pin

Bit 3 (PH63): Control bit used to enable pull-high of the P63 pin

Bit 2 (PH62): Control bit used to enable pull-high of the P62 pin

Bit 1 (PH61): Control bit used to enable pull-high of the P61 pin

Bit 0 (PH60): Control bit used to enable pull-high of the P60 pin

6.1.61 Bank 1 RA: P78PHCR (Ports 7~8 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P8HPH	P8LPH	-	P7LPH
-	-	-	-	R/W	R/W	-	R/W

Bits 7~4,1: Not used, set to "0" all the time.

Bit 3 (P8HPH): Control bit used to enable the pull-high of Port 8 high nibble pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 2 (P8LPH): Control bit used to enable the pull-high of Port8 low nibble pin

Bit 0 (P7LPH): Control bit used to enable the pull-high of Port7 low nibble pin

6.1.62 Bank 1 RB: P5PLCR (Port 5 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PL55	PL54	PL53	PL52	PL51	PL50
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used, set to "0" all the time.

Bit 5 (PL55): Control bit used to enable pull-low of the P55 pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 4 (PL54): Control bit used to enable pull-low of the P54 pin

Bit 3 (PL53): Control bit used to enable pull low of the P53 pin

Bit 2 (PL52): Control bit used to enable pull-low of the P52 pin

Bit 1 (PL51): Control bit used to enable pull-low of the P51 pin

Bit 0 (PL50): Control bit used to enable pull-low of the P50 pin

6.1.63 Bank 1 RC: P6PLCR (Port 6 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PL67): Control bit used to enable the pull-low of P67 pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 6 (PL66): Control bit used to enable the pull-low of P66 pin

Bit 5 (PL65): Control bit used to enable the pull-low of P65 pin

Bit 4 (PL64): Control bit used to enable the pull-low of P64 pin

Bit 3 (PL63): Control bit used to enable the pull-low of P63 pin

Bit 2 (PL62): Control bit used to enable the pull-low of P62 pin

Bit 1 (PL61): Control bit used to enable the pull-low of P61 pin

Bit 0 (PL60): Control bit used to enable the pull-low of P60 pin

6.1.64 Bank 1 RD: P78PLCR (Ports 7~8 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P8HPL	P8LPL	-	P7LPL
-	-	-	-	R/W	R/W	-	R/W

Bits 7~4,1: Not used, set to "0" all the time.

Bit 3 (P8HPL): Control bit used to enable the pull-low of Port 8 high nibble pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 2 (P8LPL): Control bit used to enable the pull-low of Port 8 low nibble pin

Bit 0 (P7LPL): Control bit used to enable the pull-low of Port 7 low nibble pin

6.1.65 Bank 1 RE: P5HDSCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	H55	H54	H53	H52	H51	H50
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used, set to "0" all the time.

Bits 5~0 (H55~H50): P55~P50 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.66 Bank 1 RF: P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H67	H66	H65	H64	H63	H62	H61	H60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H67~H60): P67~P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.67 Bank 1 R10: P78HDSCR (Port 7~8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P8HHDS	P8LHDS	-	P7LHDS
-	-	-	-	R/W	R/W	-	R/W

Bits 7~4,1: Not used, set to "0" all the time.

Bit 3 (P8HHDS): Control bit used to enable high drive/sink of Port8 high nibble pin

0: Enable high drive/sink

1: Disable high drive/sink

Bit 2 (P8LHDS): Control bit used to enable high drive/sink of Port8 low nibble pin

Bit 0 (P7LHDS): Control bit used to enable high drive/sink of Port7 low nibble pin

6.1.68 Bank 1 R11: P5ODCR (Port 5 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	OD55	OD54	OD53	OD52	OD51	OD50
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used, set to "0" all the time.

Bits 5~0 (OD55~OD50): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.69 Bank 1 R12: P6ODCR (Port 6 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD67~OD60): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.70 Bank 1 R13: P78ODCR (Ports 7~8 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P8HOD	P8LOD	-	P7LOD
-	-	-	-	R/W	R/W	-	R/W

Bits 7~4,1: Not used, set to "0" all the time.

Bit 3 (P8HOD): Control bit used to enable open-drain of Port 8 high nibble pin

0: Disable open-drain function

1: Enable open-drain function

Bit 2 (P8LOD): Control bit used to enable open-drain of Port 8 low nibble pin

Bit 0 (P7LOD): Control bit used to enable open-drain of Port 7 low nibble pin

6.1.71 Bank 1 R14 ~ R15: (Reserved)

6.1.72 Bank 1 R16: PWMSCR (PWM Source Clock Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PWMBS	PWMAS
-	-	-	-	-	-	R/W	R/W

Bits 7~2: Not used, set to "0" all the time.

Bit 1 (PWMBS): Clock selection for PWMB timer

0: Fs (default)

1: Fm

Bit 0 (PWMAS): Clock selection for PWMA timer

0: Fs (default)

1: Fm

6.1.73 Bank 1 R17: PWMACR (PWMA Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMAE	-	-	-	TAEN	TAP2	TAP1	TAP0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWMAE): PWMA enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWMA pin

Bits 6~4: Not used, set to "0" all the time.

Bit 3 (TAEN): TMRA enable bit. All PWM functions are valid only when this bit is set

0: TMRA is off (default value)

1: TMRA is on

PWMXEN	TXEN	Function description
0	0	Not used as PWM function; I/O pin or other functional pin.
0	1	Timer function; I/O pin or other function pin.
1	0	PWM function, the waveform keeps at low level.
1	1	PWM function, the normal PWM output waveform.

Bits 2~0 (TAP2~TAP0): TMRA clock prescaler option bits

TAP2	TAP1	TAP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.74 Bank 1 R18: PRDAL (Low Byte of PWMA Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDA7~0): The contents of the register are low bytes of the PWMA period.

NOTE

If the PWMA duty/period needs to reload, the PRDAL register must be updated.

6.1.75 Bank 1 R19: PRDAH (High Byte of PWMA Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA15	PRDA14	PRDA13	PRDA12	PRDA11	PRDA10	PRDA9	PRDA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDA15~8): The contents of the register are high bytes of PWMA period

6.1.76 Bank 1 R1A: DTAL (Low Byte of PMWA Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTA7~0): The contents of the register are low bytes of the PWMA duty.

6.1.77 Bank 1 R1B: DTAH (High Byte of PMWA Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA15	DTA14	DTA13	DTA12	DTA11	DTA10	DTA9	DTA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTA15~8): The contents of the register are high bytes of the PWMA duty.

6.1.78 Bank 1 R1C: TMRAL (Low Byte of Timer 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
R	R	R	R	R	R	R	R

Bits 7~0 (TMRA7~0): The contents of the register are low bytes of the PWMA timer which is counting. This is read-only.

6.1.79 Bank 1 R1D: TMRAH (High Byte of Timer 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRA15	TMRA14	TMRA13	TMRA12	TMRA11	TMRA10	TMRA9	TMRA8
R	R	R	R	R	R	R	R

Bits 7~0 (TMRA15~8): The contents of the register are high bytes of the PWMA timer which is counting. This is read-only

6.1.80 Bank 1 R1E: PWMBCR (PWMB Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMBE	-	-	-	TBEN	TBP2	TBP1	TBP0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWMBE): PWMB enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWMB pin

Bits 6~4: Not used, set to "0" all the time.

Bit 3 (TBEN): TMRB enable bit. All PWM function is valid only when this bit is set

0: TMRB is off (default value)

1: TMRB is on

Bits 2~0 (TBP2~TBP0): TMRB clock prescaler option bits

TBP2	TBP1	TBP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.81 Bank 1 R1F: PRDBL (Low Byte of PWMB Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDB7~0): The contents of the register are low byte of the PWMB period

NOTE

If the PWMB duty/period needs to reload, the PRDBL register must be updated.

6.1.82 Bank 1 R20: PRDBH (High Byte of PWMB Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB15	PRDB14	PRDB13	PRDB12	PRDB11	PRDB10	PRDB9	PRDB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDB15~8): The contents of the register are high byte of PWMB period

6.1.83 Bank 1 R21: DTBL (Low Byte of PMWB Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTB7~0): The contents of the register are low byte of the PWMB duty

6.1.84 Bank 1 R22: DTBH (High Byte of PMW2 Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB15	DTB14	DTB13	DTB12	DTB11	DTB10	DTB9	DTB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTB15~8): The contents of the register are high byte of the PWMB duty

6.1.85 Bank 1 R23: TMRBL (Low Byte of Timer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
R	R	R	R	R	R	R	R

Bits 7~0 (TMRB7~0): The contents of the register are low byte of the PWMB timer which is counting. This is read-only

6.1.86 Bank 1 R24: TMRBH (High Byte of Timer 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRB15	TMRB14	TMRB13	TMRB12	TMRB11	TMRB10	TMRB9	TMRB8
R	R	R	R	R	R	R	R

Bits 7~0 (TMRB15~8): The contents of the register are high byte of the PWMB timer which is counting. This is read-only

6.1.87 Bank 1 R25 ~ R32: (Reserved)

6.1.88 Bank 1 R33: URCR (UART Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBF	TXE
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit 7 (UINVEN): Enable UART TXD and RXD Port Inverse Output Bit

0: Disable TXD and RXD port inverse output.

1: Enable TXD and RXD port inverse output.

Bits 6~5 (UMODE1~UMODE0): UART mode select bits

UMODE1	UMODE0	UART mode
0	0	Mode1: 7-bit
0	1	Mode1: 8-bit
1	0	Mode1: 9-bit
1	1	Reserved

Bits 4~2 (BRATE2~BRATE0): transmit Baud rate selection

BRATE2	BRATE1	BRATE0	Baud rate	8MHz
0	0	0	Fc/13	38400
0	0	1	Fc/26	19200
0	1	0	Fc/52	9600
0	1	1	Fc/104	4800
1	0	0	Fc/208	2400
1	0	1	Fc/416	1200
1	1	X	Reserved	

Bit 1 (UTBF): UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Reset to 0 automatically when write into URTD register. UTBF bit will be cleared by hardware when enabling transmission. And UTBF bit is read-only. Therefore, write URTD register is necessary when starting transmitting shifting.

Bit 0 (TXE): Enable transmission

0: Disable

1: Enable

6.1.89 Bank 1 R34: URS (UART Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit 7 (URTD8): UART transmit data bit 8. Write only.

Bit 6 (EVEN): select parity check

0: Odd parity

1: Even parity

Bit 5 (PRE): enable parity addition

0: Disable

1: Enable

Bit 4 (PRERR): Parity error flag. Set to 1 when parity error happened, and clear to 0 by software.

Bit 3 (OVERR): Over running error flag. Set to 1 when overrun error happened, and clear to 0 by software.

Bit 2 (FMERR): Framing error flag. Set to 1 when framing error happen, and clear to 0 by software.

Bit 1 (URBF): UART read buffer full flag. Set to 1 when one character is received. Reset to 0 automatically when read from URRDL register. URBF will be cleared by hardware when enabling receiving. And URBF bit is read-only. Therefore, read URRDL register is necessary to avoid overrun error.

Bit 0 (RXE): Enable receiving

0: Disable

1: Enable

6.1.90 Bank 1 R35: URTD (UART Transmit Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
W	W	W	W	W	W	W	W

Bits 7~0 (URTD7~URTD0): UART transmit data buffer. Write only.

6.1.91 Bank 1 R36: URRDL (UART Receive Data Low Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
R	R	R	R	R	R	R	R

Bits 7~0 (URRD7~URRD0): UART Receive Data Buffer. Read only

6.1.92 Bank 1 R37: URRDH (UART Receive Data High Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	-	-	-	-	-	-	URSS
R	-	-	-	-	-	-	R/W

Bit 7 (URRD8): UART receive data bit 8. Read only.

Bits 6~1: Not used, set to "0" all the time.

Bit 0 (URSS): UART clock source select bit

0: Fc is set to Fs

1: Fc is set to Fm (Default)

6.1.93 Bank 1 R38 ~ R3F: (Reserved)

6.1.94 Bank 1 R40: EECR1 (EEPROM Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	RD	WR
-	-	-	-	-	-	R/W	R/W

Bits 7~2: unused bit, set to 0 all the time

Bit 1(RD): Read control bit

0: Don't execute EEPROM read

1: Read EEPROM content (RD can be set by software. When read instruction is completed, RD will be cleared by hardware.)

Bit 0 (WR): Write control bit

0: Write cycle to the EEPROM is completed.

1: Initiate a write cycle (WR can be set by software. When write cycle is completed, WR will be cleared by hardware).

6.1.95 Bank 1 R41: EECR2 (EEPROM Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEWE	EEDF	EEPC	-	-	-	-	-
R/W	R/W	R/W	-	-	-	-	-

Bit 7 (EEWE): EEPROM write enable bit

0: Prohibit write to the EEPROM

1: Allow EEPROM write cycles

Bit 6 (EEDF): EEPROM detect flag

0: Write cycle is completed

1: Write cycle is unfinished

Bit 5 (EEPC): EEPROM power down control bit

0: Switch of EEPROM

1: EEPROM is operating

Bits 4~0: unused bit, set to 0 all the time

6.1.96 Bank 1 R42: EERA (EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 6~0 (EERA6~EERA0): EEPROM address register

6.1.97 Bank 1 R43: EERD (EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (EERD7~EERD0): EEPROM data register.

6.1.98 Bank 1 R44: FLKR (Flash Key Register for Table write use)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FLK[7]	FLK[6]	FLK[5]	FLK[4]	FLK[3]	FLK[2]	FLK[1]	FLK[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This FLASHKEY register is used by table write IAP mode operation. The IAP enable signal is generated when a specific value is written into this register, e.g., **0xB4**. The register is designed to make sure that IAP operation occurs for flash update. Written into register value **0XC5**. The register is designed to make sure that IAP lock.

6.1.99 Bank 1 R45: TBPTL (Table Point Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB7~TB0): Table Point Address Bits 7~0.

6.1.100 Bank 1 R46: TBPTH (Table Point High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	-	-	-	TB11	TB10	TB9	TB8
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (HLB): Obtain MLB or LSB at machine code of ROM or Data area.

0: the address of read byte value is Bit7 ~Bit0

1: the address of read byte value is Bit15~Bit8

Bits 6~4: unused bit, set to 0 all the time

Bits 5~0 (TB11~TB8): Table point Address Bits 11~8.

6.1.101 Bank 1 R47: STKMON (Stack Pointer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOV	-	-	-	STL3	STL2	STL1	STL0
R	-	-	-	R	R	R	R

Bit 7 (STOV): Stack pointer overflow indicator bit. Read only.

Bits 4~0 (STL3~0): Stack pointer number. Read only.

6.1.102 Bank 1 R48: PCH (Program Counter High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PC11	PC10	PC9	PC8
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Not used. Set to "**0**" all the time.

Bits 3~0 (PC11~PC8): The high byte of program counter

6.1.103 Bank 1 R49: HLVDCR (High / Low Voltage Detector Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLVDEN	IRVSF	VDSB	VDM	HLVDS3	HLVDS2	HLVDS1	HLVDS0
R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit 7 (HLVDEN): High/Low Voltage Detector Enable Bit

0: Disable low voltage detector (LVD function related setting must be disabled in HLVDEN)

1: Enable low voltage detector

Bit 6 (IRVSF): Internal Reference Voltage Stable Flag bit

1: Indicate that the voltage detect logic will generate the interrupt flag at the specified voltage range

0: Indicate that the voltage detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

Bit 5 (VDSB): Voltage Detector State Bit. This is a read only bit.

1: VDD > HLVD trip point (HLVDS<3:0>)

0: VDD < HLVD trip point (HLVDS<3:0>)

Bit 4 (VDM): Voltage Direction Magnitude Select bit

1: Event occurs when voltage equals or exceeds trip point (HLVDS<3:0>)

0: Event occurs when voltage equals or falls below trip point (HLVDS<3:0>)

HLVDIE	HLVDEN	VDM	IRVSF	VDSB	HLVDSF	Interrupt
0	1	1	1	0->1	0->1	Not happened
0	1	1	1	1->0	0	Not happened
0	1	0	1	0->1	0	Not happened
0	1	0	1	1->0	0->1	Not happened
1	0	X	X	X	0	Not happened
1	1	X	0	X	0	Not happened
1	1	1	1	0->1	0->1	Happened
1	1	1	1	1->0	0	Not happened
1	1	0	1	0->1	0	Not happened
1	1	0	1	1->0	0->1	Happened

Bits 3~0 (HLVDS3~HLVDS0): High/Low Voltage Detector Level Bits

HLVDS3	HLVDS2	HLVDS1	HLVDS0	HLVD Voltage Level
0	0	0	0	4.73V
0	0	0	1	4.53V
0	0	1	0	4.33V
0	0	1	1	4.14V
0	1	0	0	3.94V
0	1	0	1	3.74V
0	1	1	0	3.54V
0	1	1	1	3.34V
1	0	0	0	3.14V
1	0	0	1	2.94V
1	0	1	0	2.84V
1	0	1	1	2.64V
1	1	0	0	2.54V
1	1	0	1	2.44V
1	1	1	0	2.34V
1	1	1	1	2.24V

6.1.104 Bank 1 R4A~ R4C: (Reserved)

6.1.105 Bank 1 R4D: TBWCR (Table Write Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	IAPEN
-	-	-	-	-	-	-	R/W

Bit 7~1: not used, fixed to “0” all the time.

Bits 0 (IAPEN): IAP enable bit

0: IAP mode Disable.

1: IAP mode Enable.

6.1.106 Bank 1 R4E: TBWAL (Table Write start Address Low byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBWA[7]	TBWA[6]	TBWA[5]	TBWA[4]	TBWA[3]	TBWA[2]	TBWA[1]	TBWA[0]
R/W	R/W	R/W	R	R	R	R	R

Bits 7~0(TBWA[7]~TBWA[0]): Table write star address bits 7~0, TBWA[4]~TBWA[0] always fixed to “0”.

6.1.107 Bank 1 R4F: TBWAH (Table Write start Address High byte)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	TBWA[11]	TBWA[10]	TBWA[9]	TBWA[8]
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Fixed to “0” all the time. (Read only)

Bits 3~0(TBWA[11]~TBWA[8]): Table write address bits 11~8.

※Note:

ROM Code Buffer (Start)	Table Write ROM Address (Destination)
BANK3 0x80	[TBWA] Low byte(bits7~0)
BANK3 0x81	[TBWA] High byte(bits14~8)
BANK3 0x82	[TBWA+1] Low byte(bits7~0)
BANK3 0x83	[TBWA+1] High byte(bits14~8)
⋮	⋮
BANK3 0XBE	[TBWA+31] Low byte(bits7~0)
BANK3 0XBF	[TBWA+31] High byte(bits14~8)

6.1.108 Bank 2 R5: TKAPC (Touch Key Group A Pin Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKAEP7	TKAEP6	TKAEP5	TKAEP4	TKAEP3	TKAEP2	TKAEP1	TKAEP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 (TKAEP7): Touch Key Enable Pin Control Bits

0: P67/TK8 is P67 pin.

1: Functions as Touch Key pin, TK8 is TK Sensor.

Bits 6 (TKAEP6): Touch Key Enable Pin Control Bits

0: P66/TK7 is P66 pin.

1: Functions as Touch Key pin, TK7 is TK Sensor.

Bits 5 (TKAEP5): Touch Key Enable Pin Control Bits

0: P65/TK6 is P65 pin.

1: Functions as Touch Key pin, TK6 is TK Sensor.

Bits 4 (TKAEP4): Touch Key Enable Pin Control Bits

0: P64/TK5 is P64 pin.

1: Functions as Touch Key pin, TK5 is TK Sensor.

Bits 3 (TKAEP3): Touch Key Enable Pin Control Bits

0: P63/TK4 is P63 pin.

1: Functions as Touch Key pin, TK4 is TK Sensor.

Bits 2 (TKAEP2): Touch Key Enable Pin Control Bits

0: P62/TK3 is P62 pin.

1: Functions as Touch Key pin, TK3 is TK Sensor.

Bits 1 (TKAEP1): Touch Key Enable Pin Control Bits

0: P61/TK2 is P61 pin.

1: Functions as Touch Key pin, TK2 is TK Sensor.

Bits 0 (TKAEP0): Touch Key Enable Pin Control Bits

0: P60/TK1 is P60 pin.

1: Functions as Touch Key pin, TK1 is TK Sensor.

6.1.109 Bank 2 R6: TKBPC (Touch Key Group B Pin Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKBEP7	TKBEP6	TKBEP5	TKBEP4	TKBEP3	TKBEP2	TKBEP1	TKBEP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 (TKBEP7): Touch Key Enable Pin Control Bits

0: P83/TK16/AD3 is P83/AD3 pin.

1: Functions as Touch Key pin, TK16 is TK Sensor.

Bits 6 (TKBEP6): Touch Key Enable Pin Control Bits

0: P82/TK15/AD2 is P82/AD2 pin.

1: Functions as Touch Key pin, TK15 is TK Sensor.

Bits 5 (TKBEP5): Touch Key Enable Pin Control Bits

0: P81/TK14/AD1/PWMB is P81/AD1/PWM pin.

1: Functions as Touch Key pin, TK14 is TK Sensor.

Bits 4 (TKBEP4): Touch Key Enable Pin Control Bits

0: P80/TK13/AD0/PWMA is P80/AD0/PWMA pin.

1: Functions as Touch Key pin, TK13 is TK Sensor.

Bits 3 (TKBEP3): Touch Key Enable Pin Control Bits

0: P73/TK12 is P73 pin.

1: Functions as Touch Key pin, TK12 is TK Sensor.

Bits 2 (TKBEP2): Touch Key Enable Pin Control Bits

0: P72/TK11 is P72 pin.

1: Functions as Touch Key pin, TK11 is TK Sensor.

Bits 1 (TKBEP1): Touch Key Enable Pin Control Bits

0: P71/TK10 is P71 pin.

1: Functions as Touch Key pin, TK10 is TK Sensor.

Bits 0 (TKBEP0): Touch Key Enable Pin Control Bits

0: P70/TK9 is P70 pin.

1: Functions as Touch Key pin, TK9 is TK Sensor.

6.1.110 Bank 2 R7: TKASCR (Touch Key Group A Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKAEN	-	-	-	-	TKASW2	TKASW1	TKASW0
R/W	-	-	-	-	R/W	R/W	R/W

Bit 7 (TKAEN): Touch Key Group A Enable Bit

0: Disable.

1: Enable.

Bit 6~3: not used, fixed to “0” all the time.

Bits 2~0 (TKASW2~TKASW0): Touch Key Group A pin Selected Bits.

TKASW[2:0]	Selected Channel
000	TK1
001	TK2
010	TK3
011	TK4
100	TK5
101	TK6
110	TK7
111	TK8

6.1.111 Bank 2 R8: TKBSCR (Touch Key Group B Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKBEN	-	-	-	-	TKBSW2	TKBSW1	TKBSW0
R/W	-	-	-	-	R/W	R/W	R/W

Bit 7 (TKBEN): Touch Key Group B Enable Bit

0: Disable.

1: Enable.

Bit 6~3: not used, fixed to “0” all the time.

Bits 2~0 (TKBSW2~TKBSW0): Touch Key Group B pin Selected Bits.

TKBSW[2:0]	Selected Channel
000	TK9
001	TK10
010	TK11
011	TK12
100	TK13
101	TK14
110	TK15
111	TK16

6.1.112 Bank 2 R9 ~ RC: (Reserved)

6.1.113 Bank 2 RD: TKCR (Touch Key Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKS	LDOEN	TKPSB	-	-	-	-	GMC
R/W	R/W	R/W	-	-	-	-	R/W

Bit 7 (TKS): TK Conversion start bit.

0: Reset on completion of the conversion by hardware, this bit cannot be reset by software.

1: Conversion start

Bit 6 (LDOEN): LDO Enable bit, if TK power source from VDD, this bit will be invalid.

0: LDO Disable

1: LDO Enable (Default)

Bit 5 (TKPSB): TK power source select bit.

0: TK power source from TK Regulator. (Default)

1: TK power source from VDD.

Bit 4~1: not used, fixed to "0" all the time.

Bits 0 (GMC): Touch Key Gain control Bit.

0: High gain sensing (Default)

1: Normal gain sensing

6.1.114 Bank 2 RE: TKCCR (Touch Key Calculate Cycle Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCCY7	TCCY6	TCCY5	TCCY4	TCCY3	TCCY2	TCCY1	TCCY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TCCY7~TCCY0): Touch Key Calculate Cycle set bits, the register default value = 0x40.

*Cycle=(TKCCR+1)*2

6.1.115 Bank 2 RF: TKCSR (Touch Key Calculate Step Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	CS3	CS2	CS1	CS0
-	-	-	-	R/W	R/W	R/W	R/W

Bit 7~4: not used, fixed to "0" all the time.

Bits 3~0 (CS3~CS0): Calculate Step select bits, the register default value = 0x0A.

6.1.116 Bank 2 R10: TKCTR (Touch Key Calculate Time Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCT7	TCT6	TCT5	TCT4	TCT3	TCT2	TCT1	TCT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TCT7~TCT0): Calculate time set bits, the register default value = 0x40.

Note: The TKCTR must be greater than 0x35.

6.1.117 Bank 2 R11: TKSWR (Touch Key Sensing Window Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	TSW4	TSW3	TSW2	TSW1	TSW0
-	-	-	R/W	R/W	R/W	R/W	R/W

Bit 7~5: not used, fixed to "0" all the time.

Bits 4~0 (TSW4~TSW0): Touch Key Sensing Window set bits, the register default value = 0x0A.

6.1.118 Bank 2 R12: TKAH (The Most Significant Byte of A Group Touch Key Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKA[15]	TKA[14]	TKA[13]	TKA[12]	TKA[11]	TKA[10]	TKA[9]	TKA[8]
R	R	R	R	R	R	R	R

Bits 7~0 (TKA [15]~TKA[8]): The Most Significant Byte of A Group Touch Key Buffer**.**

6.1.119 Bank 2 R13: TKAL (The Least Significant Byte of A Group Touch Key Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKA[7]	TKA[6]	TKA[5]	TKA[4]	TKA[3]	TKA[2]	TKA[1]	TKA[0]
R	R	R	R	R	R	R	R

Bits 7~0 (TKA[7]~TKA[0]): The Least Significant Byte of A Group Touch Key Buffer.

6.1.120 Bank 2 R14: TKBH (The Most Significant Byte of B Group Touch Key Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKB[15]	TKB[14]	TKB[13]	TKB[12]	TKB[11]	TKB[10]	TKB[9]	TKB[8]
R	R	R	R	R	R	R	R

Bits 7~0 (TKB[15]~TKB[8]): The Most Significant Byte of B Group Touch Key Buffer.

6.1.121 Bank 2 R15: TKBL (The Least Significant Byte of B Group Touch Key Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKB[7]	TKB[6]	TKB[5]	TKB[4]	TKB[3]	TKB[2]	TKB[1]	TKB[0]
R	R	R	R	R	R	R	R

Bits 7~0 (TKB[7]~TKB[0]): The Least Significant Byte of B Group Touch Key Buffer.

6.1.122 Bank 2 R16: TKSCR (Touch Key idle Scan Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKMCS1	TKMCS0	-	-	TKISE	TKST2	TKST1	TKST0
R/W	R/W	-	-	R/W	R/W	R/W	R/W

Bit 7~6 (TKMCS1~0): Touch Key Multi-pin combine mode select bits.

TKMCS1	TKMCS0	Group A Condition	Group B Condition	Note
0	0	Depend on TKASCR	Depend on TKBSCR	
0	1	TK1~8 Combine	TK9~16 Combine	1.Suggest for “TK idle with scan Mode” Application. 2. TK Idle with scan mode only have 1 flow
1	0	TK1~4 Combine	TK9~12 Combine	1.Suggest for “TK idle with scan Mode” Application. 2. TK Idle with scan mode have 2 flows, And this condition is the 1st flow mode
1	1	TK5~8 Combine	TK13~16 Combine	1.Suggest for “TK idle with scan Mode” Application. 2. TK Idle with scan mode have 2 flows And this condition is the 2nd flow mode

Bit 5,4: not used, fixed to “0” all the time.

Bit 3 (TKISE): TK idle with scan mode enable bit, for Low consumption application.

0: Disable

1: Enable, TK automatically scan for sleep mode condition.

Bits 2~0 (TKST2~TKST0): Touch Key idle scan time setting Bits.

000: 12.5ms

001: 25ms

010: 50ms

011: 100ms

100: 200ms

101: 400ms

110: 800ms

111: 1600ms

6.1.123 Bank 2 R17: TKA1WBH (TK Group A idle Scan Wakeup Base High byte Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TA1WB[15]	TA1WB[14]	TA1WB[13]	TA1WB[12]	TA1WB[11]	TA1WB[10]	TA1WB[9]	TA1WB[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TA1WB[15]~TA1WB[8]): 1st flow TK group A idle scan wakeup base high byte set bits.

6.1.124 Bank 2 R18: TKA1WBL (TK Group A idle Scan Wakeup Base Low byte Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TA1WB[7]	TA1WB[6]	TA1WB[5]	TA1WB[4]	TA1WB[3]	TA1WB[2]	TA1WB[1]	TA1WB[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TA1WB[7]~TA1WB[0]): 1st flow TK group A idle scan wakeup base high byte set bits.

6.1.125 Bank 2 R19: TKA1WR (Touch Key of Group A idle scan Wakeup Range Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TA1WR[7]	TA1WR[6]	TA1WR[5]	TA1WR[4]	TA1WR[3]	TA1WR[2]	TA1WR[1]	TA1WR[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6 (TA1WR[7:6]): 1st flow TK group A idle scan wakeup range multiple set bits.

Bits 5~0 (TA1WR[5:0]): 1st flow TK group A idle scan wakeup range multiplicand set bits.

Tx1WR[7:6]	Idle scan wakeup range
00	**Tx1WR[5:0] x 1**
01	**Tx1WR[5:0] x 2**
10	**Tx1WR[5:0] x 4**
11	**Tx1WR[5:0] x 8**

X = A, B

6.1.126 Bank 2 R1A: TKA2WBH (TK Group A idle Scan Wakeup Base High byte Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TA2WB[15]	TA2WB[14]	TA2WB[13]	TA2WB[12]	TA2WB[11]	TA2WB[10]	TA2WB[9]	TA2WB[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TA2WB[15]~TA2WB[8]): 2nd flow TK group A idle scan wakeup base high byte set bits.

6.1.127 Bank 2 R1B: TKA2WBL (TK Group A idle Scan Wakeup Base Low byte Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TA2WB[7]	TA2WB[6]	TA2WB[5]	TA2WB[4]	TA2WB[3]	TA2WB[2]	TA2WB[1]	TA2WB[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TA2WB[7]~TA2WB[0]): 2nd flow TK group A idle scan wakeup base high byte set bits.

6.1.128 Bank 2 R1C: TKA2WR (Touch Key of Group A idle scan Wakeup Range Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TA2WR[7]	TA2WR[6]	TA2WR[5]	TA2WR[4]	TA2WR[3]	TA2WR[2]	TA2WR[1]	TA2WR[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6 (TA2WR[7:6]): 1st flow TK group A idle scan wakeup range multiple set bits.

Bits 5~0 (TA2WR[5:0]): 1st flow TK group A idle scan wakeup range multiplicand set bits.

Tx2WR[7:6]	Idle scan wakeup range
00	**Tx2WR[5:0] x 1**
01	**Tx2WR[5:0] x 2**
10	**Tx2WR[5:0] x 4**
11	**Tx2WR[5:0] x 8**

X = A,B

6.1.129 Bank 2 R1D: TKB1WBH (TK Group B idle Scan Wakeup Base High byte Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB1WB[15]	TB1WB[14]	TB1WB[13]	TB1WB[12]	TB1WB[11]	TB1WB[10]	TB1WB[9]	TB1WB[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB1WB[15]~TB1WB[8]): 1st flow TK group B idle scan wakeup base high byte set bits.

6.1.130 Bank 2 R1E: TKB1WBL (TK Group B idle Scan Wakeup Base Low byte Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB1WB[7]	TB1WB[6]	TB1WB[5]	TB1WB[4]	TB1WB[3]	TB1WB[2]	TB1WB[1]	TB1WB[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB1WB[7]~TB1WB[0]): 1st flow TK group B idle scan wakeup base high byte set bits.

6.1.131 Bank 2 R1F: TKB1WR (Touch Key of Group B idle scan Wakeup Range Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB1WR[7]	TB1WR[6]	TB1WR[5]	TB1WR[4]	TB1WR[3]	TB1WR[2]	TB1WR[1]	TB1WR[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6 (TB1WR[7:6]): 1st flow TK group B idle scan wakeup range multiple set bits.

Bits 5~0 (TB1WR[5:0]): 1st flow TK group B idle scan wakeup range multiplicand set bits.

Tx1WR[7:6]	Idle scan wakeup range
00	**Tx1WR[5:0] x 1**
01	**Tx1WR[5:0] x 2**
10	**Tx1WR[5:0] x 4**
11	**Tx1WR[5:0] x 8**

X = A, B

6.1.132 Bank 2 R20: TKB2WBH (TK Group B idle Scan Wakeup Base High byte Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB2WB[15]	TB2WB[14]	TB2WB[13]	TB2WB[12]	TB2WB[11]	TB2WB[10]	TB2WB[9]	TB2WB[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB2WB[15]~TB2WB[8]): 2nd flow TK group B idle scan wakeup base high byte set bits.

6.1.133 Bank 2 R21: TKB2WBL (TK Group B idle Scan Wakeup Base Low byte Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB2WB[7]	TB2WB[6]	TB2WB[5]	TB2WB[4]	TB2WB[3]	TB2WB[2]	TB2WB[1]	TB2WB[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB2WB[7]~TB2WB[0]): 2nd flow TK group B idle scan wakeup base high byte set bits.

6.1.134 Bank 2 R22: TKB2WR (Touch Key of Group B idle scan Wakeup Range Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB2WR[7]	TB2WR[6]	TB2WR[5]	TB2WR[4]	TB2WR[3]	TB2WR[2]	TB2WR[1]	TB2WR[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6 (TB2WR[7:6]): 2nd flow TK group B idle scan wakeup range multiple set bits.

Bits 5~0 (TB2WR[5:0]): 2nd flow TK group B idle scan wakeup range multiplicand set bits.

Tx2WR[1:0]	Idle scan wakeup range
00	**Tx2WR[5:0] x 1**
01	**Tx2WR[5:0] x 2**
10	**Tx2WR[5:0] x 4**
11	**Tx2WR[5:0] x 8**

X = A,B

6.1.135 Bank 2 R23 ~ R46: (Reserved)

6.1.136 Bank 2 R47: LOCKPR (Lock Page Number Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	LOCKPR4	LOCKPR3	LOCKPR2	LOCKPR1	LOCKPR0
-	-	-	R/W	R/W	R/W	R/W	R/W

Bits 4~0 (LOCKPR6~ LOCKPR0): Lock Page Number
*IAP Enhanced Protect Lock Address (1step = 128word)

6.1.137 Bank 2 R48: LOCKCR (Lock Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOCKEN	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-

Bit 7 (LOCKEN): Enhanced Protect Control Bit

1: Enable

0: Disable (Default)

Bits 6~0: Not used, set to “0” all the time.

6.1.138 Bank 2 R49 ~ R4F: (Reserved)

6.1.139 R50~R7F, Banks 0~3 R80~RFF

These are all 8-bit general-purpose registers.

6.2 TCC/WDT and Prescaler

Two 8-bit counters are available as prescalers for the TCC and WDT. The TPSR0~ TPSR2 bits of the TCCCR register (Bank 0 R22) are used to determine the ratio of the TCC prescaler. Likewise, the WPSR0~WPSR2 bits of the WDTCR register (Section) are used to determine the WDT prescaler. The prescaler counter is cleared by the instructions each time they are written into TCC. The WDT and prescaler are cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 below depicts the circuit diagram of TCC/WDT.

The TCCD (Section *6.1.27 TCC Data Register*) is an 8-bit timer/counter. The TCC clock source is from the internal clock only and TCC will be incremented by 1 at Fc clock (without prescaler). **The TCC will stop running when Sleep mode occurs.**

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in Sleep mode). During Normal operation or Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during Normal mode by software programming (see WDTE bit of WDTCR (Section) register). With no prescaler, the WDT time-out period is approximately 18 ms (one oscillator start-up timer period).

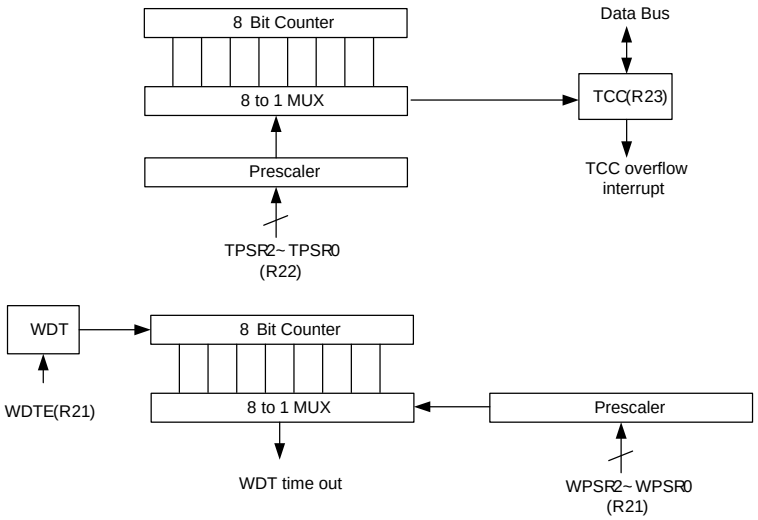
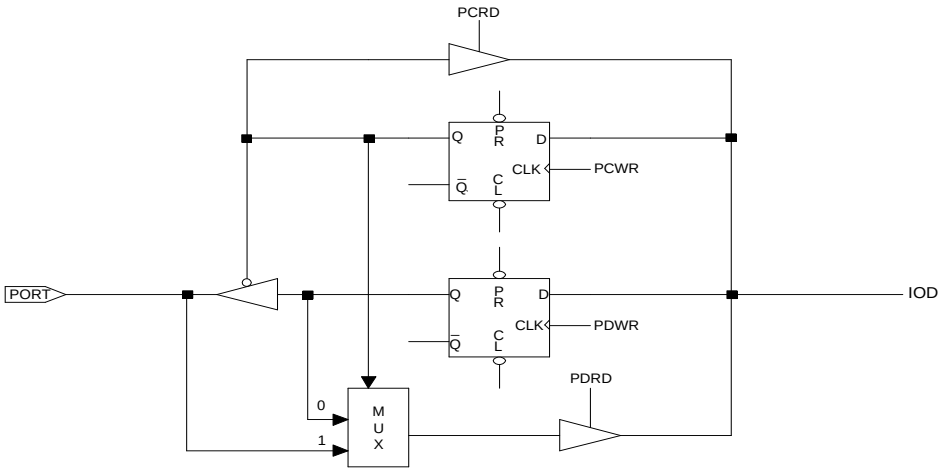


Figure 6-3 TCC and WDT Block Diagram

6.3 I/O Ports

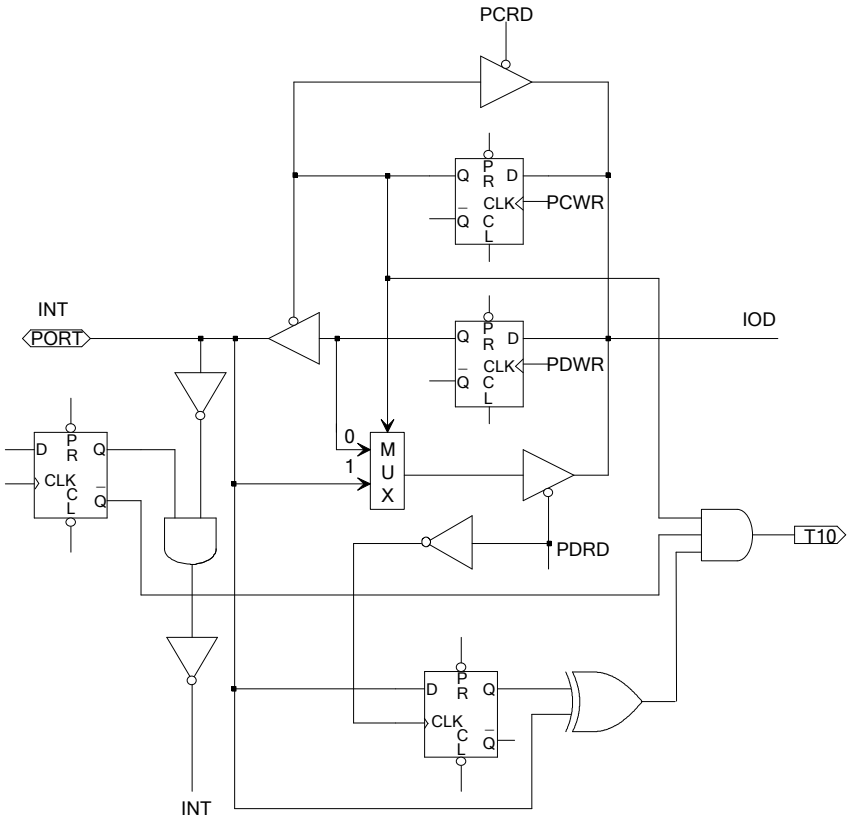
The I/O registers, Port 5~Port 8 are bidirectional tri-state I/O ports. All can be pulled high and pulled low internally by software. Furthermore, they can also be set as open-drain output and high sink/drive by software. Ports 5~8 features wake-up and interrupt function as well as input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 8 are shown in the following Figures 6-4a to 6-4d.



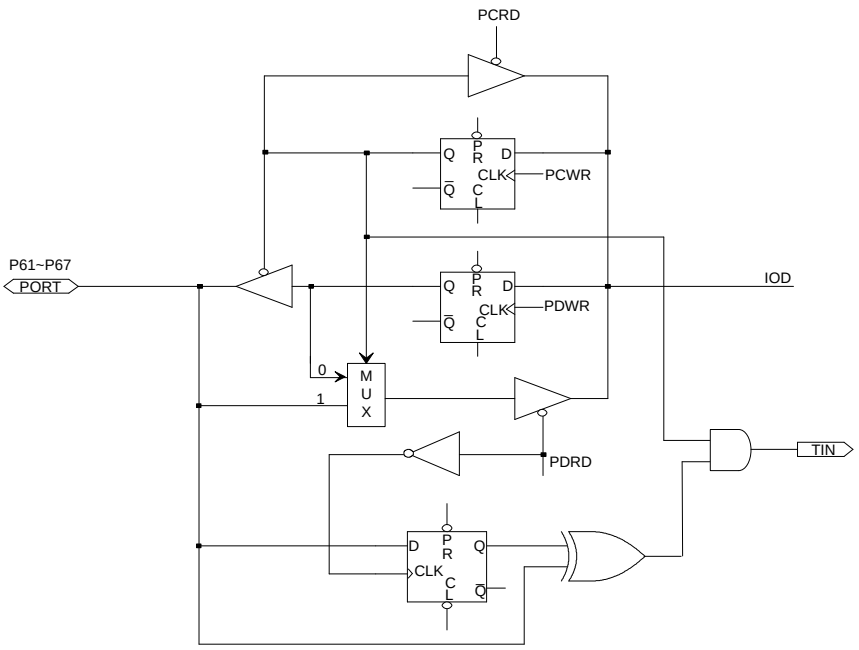
Note: *Pull-down is not shown in the figure.*

Figure 6-4a I/O Port and I/O Control Register for Port 5~8 Circuit Diagram



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4b I/O Port and I/O Control Register for /INT Circuit



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4c I/O Port and I/O Control Register for Ports 5~8 Circuit

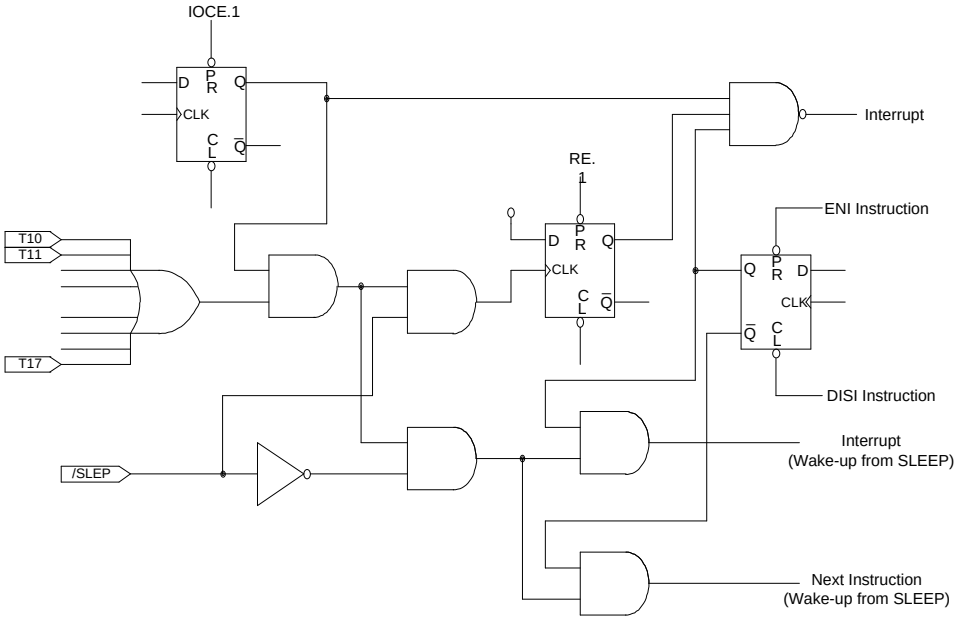


Figure 6-4d I/O Port 5~8 with Input Change Interrupt/Wake-up Block Diagram

6.3.1 Usage of Ports 5~8 Input Change Wake-up/Interrupt Function

1. Wake-up
a) Before Sleep:
1) Disable WDT
2) Read I/O Port (MOV R6,R6)
3) Execute "ENI" or "DISI"
4) Enable Wake-up bit (Set **ICWKPx** = 1)
5) Execute "SLEP" instruction
b) After Wake-up:
→ Next instruction

2. Wake-up and Interrupt
a) Before SLEEP
1) Disable WDT
2) Read I/O Port (MOV R6,R6)
3) Execute "ENI" or "DISI"
4) Enable Wake-up bit (Set **ICWKPx** = 1)
5) Enable interrupt (Set PxICIE = 1)
6 Execute "SLEP" instruction
b) After Wake-up
1) IF "ENI" → Interrupt vector (0006H)
2) IF "DISI" → Next instruction

6.4 Reset and Wake-up

A Reset is initiated by one of the following events:

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)
4) LVR (if enabled)

The device is kept in a Reset condition for a period of approximately 18ms (one oscillator start-up timer period) after a reset is detected. If the /Reset pin goes “low” or the WDT time-out is active, a reset is generated. In IRC mode, the reset time is 8-/32 clocks. Once a Reset occurs, the following functions are performed (see Figure 6-5 below):

- The oscillator is continuously running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- The control register bits are set as shown in the table below under Section 6.4.3, *Summary of Register Initial Values after Reset*.

The Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. Wake-up is then generated (in IRC mode the wake-up time is 8-/32 clocks). The controller can be awakened by any of the following events:

1) External reset input on /RESET pin
2) WDT time-out (if enabled)
3) External (/INT) pin changes (if INTWE is enabled)
4) Port input status changes (if ICWKPx is enabled)
5) SPI receives data while it serves as Slave device (if SPIWK is enabled)
6) I^2C receives data while it serves as Slave device (if I2CWK is enabled)
7) Low Voltage Detector (if LVDWK is enabled)
8) A/D conversion completed (if ADWK is enabled)

The first two events (1 and 2) will cause the eKTF5616/08 to reset. The T and P flags of R3 are used to determine the source of the reset (Wake-up). Events 3 to 7 are considered as continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x02~0x40 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up.

Only one event (from Events 3 to 6) can be enabled before entering into Sleep mode. That is:

a) If WDT is enabled before SLEP, the eKTF5616/08 can wake up only when Events 1 or 2 occurs. Refer to Section 6.5 *Interrupt* for further details.

b) If External (/INT) pin change is used to wake up the eKTF5616/08 and the EXWE bit is enabled before SLEP (with WDT disabled), the eKTF5616/08 can only wake up when Event 3 occurs.

c) If Port Input Status Change is used to wake-up the eKTF5616/08 and the corresponding wake-up setting is enabled before SLEP (with WDT disabled), the eKTF5616/08 will wake up only when Event 4 occurs.

d) With SPI serves as Slave device and the SPIWK bit of Bank0 R11 register is enabled before SLEP (with WDT disabled), the SPI will wake up the eKTF5616/08 after it receives data. Hence, the eKTF5616/08 can wake up only when Event 5 occurs.

e) When I^2C is serving as Slave device and I2CWK bit of Bank 0 R11 register is enabled before SLEP (with WDT disabled), the I^2C will wake up the eKTF5616/08 after it receives data. Hence, the eKTF5616/08 can only be woken up by Event 6.

f) If Low voltage detector is used to wake up the eKTF5616/08 and the LVDWK bit of Bank 0 R10 register is enabled before SLEP, WDT must be disabled by software. Hence, the eKTF5616/08 can only be woken up by Event 7.

g) If AD conversion completed is used to wake up the eKTF5616/08 and the ADWK bit of Bank 0 R10 register is enabled before SLEP, WDT must be disabled by software. Hence, the eKTF5616/08 can only be woken up by Event 8.

6.4.1 Summary of Wake-up and Interrupt Mode Operation

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	INTWK = 0, EXIE = 0	/INT pin Disable							
	INTWK = 0, EXIE = 1	Wake-up is invalid.				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	INTWK = 1, EXIE = 0	/INT pin Disable							
	INTWK = 1, EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC INT	TCIE = 0	Wake-up is invalid.				Interrupt is invalid.			
	TCIE = 1	Wake-up is invalid.		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC1 Interrupt (Used as timer)	TC1IE = 0	Wake-up is invalid		Wake-up is invalid.	Interrupt is invalid	Interrupt is invalid			
	TC1IE = 1			Wake up +	Wake up +	Next Instruction	Interrupt +	Next Instructio	Interrupt +

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
				Next Instruction	Interrupt Vector		Interrupt Vector	n	Interrupt Vector
TC1 Interrupt (Used as counter)	TC1IE = 0	Wake-up is invalid				Interrupt is invalid.			
	TC1IE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWMA/B (When TimerA/B Match PRD or DT)	PWMxPIE = 0	Wake-up is invalid.				Interrupt is invalid.			
	PWMxPIE = 1	Wake-up is invalid.		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Pin Change INT	WKPxH/L = 0, PxICIE = 0	Wake-up is invalid.				Interrupt is invalid.			
	WKPxH/L = 0, PxICIE = 1	Wake-up is invalid.				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	WKPxH/L = 1, PxICIE = 0	Wake up + Next Instruction				Interrupt is invalid.			
	WKPxH/L = 1, PxICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Detector	LVDWK = 0, LVDIE = 0	Wake-up is invalid.				Interrupt is invalid.			
	LVDWK = 0, LVDIE = 1	Wake-up is invalid.				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVDWK = 1, LVDIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid.			
	LVDWK = 1, LVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C (Slave mode)	I2CWK = 0, I2CxIE = 0	Wake-up is invalid.				I2C Can't use		Interrupt is invalid.	
	I2CWK = 0, I2CxIE = 1	Wake-up is invalid.				I2C Can't use		Next Instruction	Interrupt + Interrupt Vector
	I2CWK = 1, I2CxIE = 0	Wake up + Next Instruction **I2C must be slave mode**				I2C Can't use		Interrupt is invalid.	
	I2CWK = 1, I2CxIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	I2C Can't use		Next Instruction	Interrupt + Interrupt Vector
SPI (Slave mode)	SPIWK = 0, SPIE = 0	Wake-up is invalid.				Interrupt is invalid.			

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
	SPIWK = 0, SPIE = 1	Wake-up is invalid.				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	SPIWK = 1, SPIE = 0	Wake up + Next Instruction				Interrupt is invalid.			
	SPIWK = 1, SPIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Transmit complete Interrupt	UTIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	UTIE = 1					Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive data Buffer full Interrupt	URIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	URIE = 1					Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive Error Interrupt	UTIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid.		Interrupt is invalid.	
	UTIE = 1					Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
AD INT	ADWK = 0, ADIE = 0	wake-up is invalid.				Interrupt is invalid.			
	ADWK = 0, ADIE = 1	wake-up is invalid.				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ADWK = 1, ADIE = 0	Wake up + Next Instruction **Fs and Fm don't stop**				Interrupt is invalid.			
	ADWK = 1, ADIE = 1	Wake up + Next Instruction **Fs and Fm don't stop**	Next Instruction	Next Instruction	Next Instruction	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
WDT time out		RESET	RESET	RESET	RESET	RESET	RESET	RESET	RESET

NOTE

After wake up:

1. If interrupt enables → interrupt + next instruction

2. If interrupt disables → next instruction

6.4.2 The Status of RST, T, and P of the Status Register

A reset condition is initiated by one of the following events:

1) Power-on condition
2) High-low-high pulse on the /RESET pin
3) Watchdog timer time-out
4) When LVR occurs

The values of T and P, as listed in the following table are used to check how the MCU wakes up. The next table shows the events that may affect the status of T and P.

■ **Values of RST, T and P after Reset:**

Reset Type	T	P
Power-on	1	1
/RESET during Operation mode	P*	P*
/RESET Wake-up during Sleep mode	1	0
WDT during Operation mode	0	P*
WDT Wake-up during Sleep mode	0	0
Wake up on pin change during Sleep mode	1	0

* ***P:*** *Previous status before reset*

■ **Status of T and P being affected by Events:**

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake up on pin change during Sleep mode	1	0

* ***P:*** *Previous value before reset*

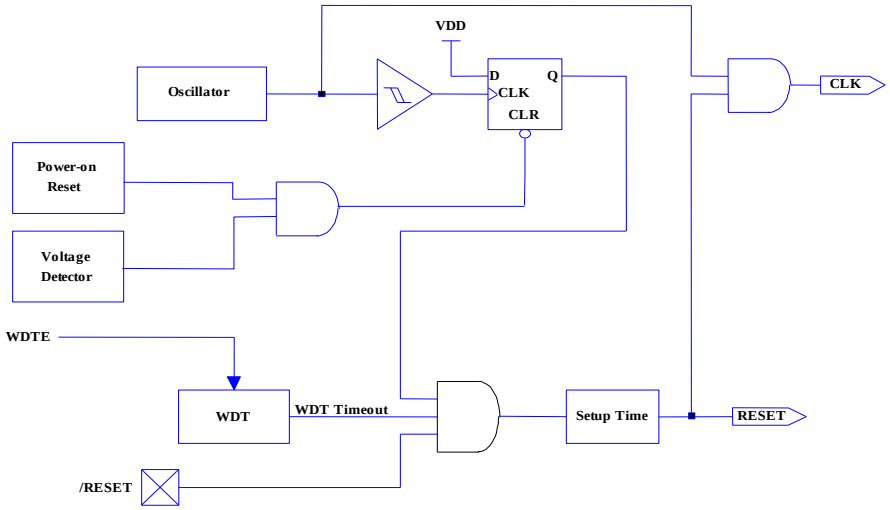


Figure 6-5 Block Diagram of Controller Reset

6.4.3 Summary of Register Initial Values after Reset

Legend: ***U:*** *Unknown or don't care* ***P:*** *Previous value before reset*
C: *Same with Code option* ***t:*** *Check tables under Section 6.4.2*

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x01	R1 (BSR)	Bit Name	-	-	SBS1	SBS0	-	-	GBS1	GBS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	0	0	P	P
0x02	R2 (PCL)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	INT	N	OV	T	P	Z	DC	C
		Power-On	0	U	U	1	1	U	U	U
		/RESET and WDT	0	P	P	t	t	P	P	P
		Wake-up from Sleep/Idle	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X05	Bank 0, R5 (Port 5)	Bit Name	-	-	P55	P54	P53	P52	P51	P50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0x06	Bank 0, R6 (Port 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x07	Bank 0, R7 (Port 7)	Bit Name	-	-	-	-	P73	P72	P71	P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0x08	Bank 0, R8 (Port 8)	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0B	Bank 0, RB (IOCR5)	Bit Name	-	-	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0x0C	Bank 0, RC (IOCR6)	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 0, RD (IOCR7)	Bit Name	-	-	-	-	IOC73	IOC72	IOC71	IOC70
		Power-On	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0x0E	Bank 0, RE (OMCR)	Bit Name	CPUS	IDLE	PERCS	-	FMSF	-	RCM1	RCM0
		Power-On	Code option (HLFS)	1	0	0	1	0	Code option (RCM1)	Code option (RCM0)
		/RESET and WDT	Code option (HLFS)	1	0	0	1	0	P	P
		Wake-up from Sleep/Idle	P	P	P	0	P	0	P	P
0X0F	Bank 0, RF EIESCR	Bit Name	-	-	-	-	EIES1	EIES0	-	-
		Power-On	0	0	0	0	1	1	0	0
		/RESET and WDT	0	0	0	0	1	1	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	0
0x10	Bank 0, R10 (WUCR1)	Bit Name	-	-	LVDWK	ADWK	INTWK1	INTWK0	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	0	0

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x11	Bank 0, R11 WUCR2	Bit Name	-	-	-	-	SPIWK	I2CWK	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	0	0
0x12	Bank 0, R12 WUCR3	Bit Name	ICWKP8	ICWKP 7	ICWKP6	ICWKP 5	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	0	0	0	0
0X14	Bank 0, R14 SFR1	-	-	-	LVDSF	ADSF	EXSF1	EXSF0	-	TCSF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	0	P
0X15	Bank 0, R15 SFR2	-	-	-	UERRSF	URSF	UTSF	-	-	TC1SF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	0	0	P
0X16	Bank 0, R16 SFR3	Bit Name	-	-	-	-	PWMBP SF	PWMBD SF	PWMAP SF	PWMAD SF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X17	Bank 0, R17 SFR4	Bit Name	P8ICSF	P7ICSF	P6ICSF	P5ICSF	SPISF	I2CSTP SF	I2CRSF	I2CTSF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	Bank 0, R19 SFR6	Bit Name	SHSF	-	-	TKTOS F	TKCSF	TKPESF	TKOESF	TKSF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	P	P	P	P	P
0X1B	Bank 0, R1B IMR1	Bit Name	-	-	LVDIE	ADIE	EXIE1	EXIE0	-	TCIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	0	P
0X1C	Bank 0, R1C IMR2	Bit Name	-	-	UERRIE	URIE	UTIE	-	-	TC1IE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	0	0	P
0X1D	BANK 0, R1D IMR3	Bit Name	-	-	-	-	PWMBPI E	PWMBDI E	PWMAPI E	PWMAD IE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1E	Bank 0, R1E IMR4	Bit Name	P8ICIE	P7ICIE	P6ICIE	P5ICIE	SPIIE	I2CSTPIE	I2CRIE	I2CTIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X20	Bank 0, R20 IMR6	Bit Name	SHIE	-	-	-	TKCIE	-	TKERRIE	TKIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	0	P	P
0X21	Bank 0, R21 WDTCR	Bit Name	WDTE	FSSF	-	-	PSWE	WPSR2	WPSR1	WPSR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	0	0	P	P	P	P
0X22	Bank 0, R22 TCCCR	Bit Name	-	TCCS	-	-	PSTE	TPSR2	TPSR1	TPSR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	P	P	P	P	P	P	P
0X23	Bank 0, R23 TCCD	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X24	Bank 0, R24 TC1CR1	Bit Name	TC1S	TC1RC	TC1SS1	-	TC1FF	TC1MOS	TC1IS1	TC1IS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	0	P	P	P	P
0X25	Bank 0, R25 TC1CR2	Bit Name	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X26	Bank 0, R26 TC1DA	Bit Name	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X27	Bank 0, R27 TC1DB	Bit Name	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X30	Bank 0, R30 I2CCR1	Bit Name	Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
		Power-On	0	0	0	0	1	0	0	1
		/RESET and WDT	0	0	0	0	1	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X31	Bank 0, R31 I2CCR2	Bit Name	I2CBF	GCEN	I2COPT	BBF	-	I2CTS1	I2CTS0	I2CEN
		Power-On	0	0	Code option (I2COPT)	0	0	0	0	1

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		/RESET and WDT	0	0	P	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	0	P	P	P
0X32	Bank 0, R32 I2CSA	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X33	Bank 0, R33 I2CDB	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X34	Bank 0, R34 I2CDAL	Bit Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X35	Bank 0, R35 I2CDAH	Bit Name	-	-	-	-	-	-	DA9	DA8
		Power-On	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X36	Bank 0, R36 SPICR	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X37	Bank 0, R37 SPIS	Bit Name	DORD	TD1	TD0	-	OD3	OD4	-	RBF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	0	P	P	0	P
0X38	Bank 0, R38 SPIR	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-On	U*	U*	U*	U*	U*	U*	U*	U*
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X39	BANK 0, R39 SPIW	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-On	U*	U*	U*	U*	U*	U*	U*	U*
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3E	BANK 0, R3E ADCR1	Bit Name	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3F	BANK 0, R3F ADCR2	Bit Name	-	VPIS2	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	P	P	P	P	P	P	0

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X40	BANK 0, R40 ADISR	Bit Name	-	-	-	-	ADIS3	ADIS2	ADIS1	ADIS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X41	BANK 0, R41 ADER1	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X43	BANK 0, R43 ADDL	Bit Name	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
		Power-On	0	0	0	0	0	0	0	U0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X44	BANK 0, R44 ADDH	Bit Name	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		Power-On	0	0	0	0	0	0	0	U0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X45	BANK 0, R45 ADCVL	Bit Name	ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
		Power-On	0	0	0	0	0	0	0	U0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	BANK 0, R46 ADCVH	Bit Name	-	-	-	-	ADCD11	ADCD10	ADCD9	ADCD8
		Power-On	0	0	0	0	0	0	0	U0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X05	Bank 1, R5 IOCR8	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X08	Bank 1, R8 P5PHCR	Bit Name	-	-	PH55	PH54	PH53	PH52	PH51	PH50
		Power-On	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0X09	Bank 1, R9 P6PHCR	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0A	Bank 1, RA P78PHCR	Bit Name	-	-	-	-	P8HPH	P8LPH	-	P7LPH
		Power-On	0	0	0	0	1	1	0	1
		/RESET and WDT	0	0	0	0	1	1	0	1
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0B	Bank 1, RB P5PLCR	Bit Name	-	-	PL55	PL54	PL53	PL52	PL51	PL50
		Power-On	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0X0C	Bank 1, RC P6PLCR	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 1, RD P78PLCR	Bit Name	-	-	-	-	P8HPL	P8LPL	-	P7LPL
		Power-On	0	0	0	0	1	1	0	1
		/RESET and WDT	0	0	0	0	1	1	0	1
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	P
0X0E	Bank 1, RE P5HDSCR	Bit Name	-	-	H55	H54	H53	H52	H51	H50
		Power-On	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0X0F	Bank 1, RF P6HDSCR	Bit Name	H67	H66	H65	H64	H63	H62	H61	H60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X10	Bank 1, R10 P78HDSCR	Bit Name	-	-	-	-	P8HHDS	P8LHDS	-	P7LHDS
		Power-On	0	0	0	0	1	1	0	1
		/RESET and WDT	0	0	0	0	1	1	0	1
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	P
0X11	Bank 1, R11 P5ODCR	Bit Name	-	-	OD55	OD54	OD53	OD52	OD51	OD50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0X12	Bank 1, R12 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X13	Bank 1, R13 P78ODCR	Bit Name	-	-	-	-	P8HOD	P8LOD	-	P7LOD
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	P
0X16	Bank 1, R16 PWMSCR	Bit Name	-	-	-	-	-	-	PWMBS	PWMAS
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X17	Bank 1, R17 PWMACR	Bit Name	PWMAE	-	-	-	TAEN	TAP2	TAP1	TAP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X18	Bank 1, R18 PRDAL	Bit Name	PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	Bank 1, R19 PRDAH	Bit Name	PRDA15	PRDA14	PRDA13	PRDA12	PRDA11	PRDA10	PRDA9	PRDA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1A	Bank 1, R1A	Bit Name	DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DTAL	Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 1, R1B DTAH	Bit Name	DTA15	DTA14	DTA13	DTA12	DTA11	DTA10	DTA9	DTA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1C	Bank 1, R1C TMRAL	Bit Name	TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	Bank 1, R1D TMRAH	Bit Name	TMRA15	TMRA14	TMRA13	TMRA12	TMRA11	TMRA10	TMRA9	TMRA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1E	BANK 1, R1E PWMBCR	Bit Name	PWMBE	-	-	-	TBEN	TBP2	TBP1	TBP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	P	P	P	P
0X1F	Bank 1, R1F PRDBL	Bit Name	PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X20	Bank 1, R20 PRDBH	Bit Name	PRDB15	PRDB14	PRDB13	PRDB12	PRDB11	PRDB10	PRDB9	PRDB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X21	Bank 1, R21 DTBL	Bit Name	DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X22	Bank 1, R22 DTBH	Bit Name	DTB15	DTB14	DTB13	DTB12	DTB11	DTB10	DTB9	DTB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X23	Bank 1, R23 TMRBL	Bit Name	TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X24	Bank 1, R24 TMRBH	Bit Name	TMRB15	TMRB14	TMRB13	TMRB12	TMRB11	TMRB10	TMRB9	TMRB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X**33**	Bank 1, R**33** URCR	Bit Name	UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBF	TXE
		Power-On	0	0	0	0	0	0	1	0
		/RESET and WDT	0	0	0	0	0	0	1	0

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X**34**	Bank 1, R**34** URS	Bit Name	URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X**35**	Bank 1, R35 URTD	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X**36**	Bank 1, R36 URRDL	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X**37**	Bank 1, R37 URRDH	Bit Name	URRD8	-	-	-	-	-	-	URSS
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Sleep/Idle	P	0	0	0	0	0	0	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X**40**	Bank 1, R40 EECR1	Bit Name	-	-	-	-	-	-	RD	WR
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X**41**	Bank 1, R41 EECR2	Bit Name	EEWE	EEDF	EEPC	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	0	0	0	0	0
0X**42**	Bank 1, R42 EERA	Bit Name	-	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	P	P	P	P	P	P	P
0X**43**	Bank 1, R43 EERD	Bit Name	EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X**44**	Bank 1, R44 FLKR	Bit Name	FLK[7]	FLK[6]	FLK[5]	FLK[4]	FLK[3]	FLK[2]	FLK[1]	FLK[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X45	Bank 1, R45 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 1, R46 TBPTH	Bit Name	HLB	-	-	-	TB11	TB10	TB9	TB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-up from Sleep/Idle	P	P	0	0	P	P	P	P
0X47	Bank 1, R47 STKMON	Bit Name	STOV	-	-	-	STL3	STL2	STL1	STL0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X48	Bank 1, R48 PCH	Bit Name	-	-	-	-	PC11	PC10	PC9	PC8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X49	Bank 1, R49 HLVDCR	Bit Name	HLVDEN	IRVSF	VDSB	VDM	HLVDS3	HLVDS2	HLVDS1	HLVDS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X4D	Bank 1, R4D TBWCR	Bit Name	-	-	-	-	-	-	-	IAP
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	0	P
0X4E	Bank 1, R4E TBWAL	Bit Name	TBWA[7]	TBWA[6]	TBWA[5]	TBWA[4]	TBWA[3]	TBWA[2]	TBWA[1]	TBWA[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X4F	Bank 1, R4F TBWAH	Bit Name	-	-	-	-	TBWA[11]	TBWA[10]	TBWA[9]	TBWA[8]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X05	Bank 2, R5 TKAPC	Bit Name	TKAEP7	TKAEP6	TKAEP5	TKAEP4	TKAEP3	TKAEP2	TKAEP1	TKAEP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X06	Bank 2, R6 TKBPC	Bit Name	TKBEP7	TKBEP6	TKBEP5	TKBEP4	TKBEP3	TKBEP2	TKBEP1	TKBEP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X07	Bank 2, R7 TKASCR	Bit Name	TKAEN	-	-	-	-	TKASW2	TKASW1	TKASW0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	0	P	P	P
0X08	Bank 2, R8 TKBSCR	Bit Name	TKBEN	-	-	-	-	TKBSW2	TKBSW1	TKBSW0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	0	P	P	P
0X0D	Bank 2, RD TKCR	Bit Name	TKS	LDOEN	TKPSB	-	-	-	-	GMC
		Power-On	0	**1**	0	0	0	0	0	0
		/RESET and WDT	0	**1**	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0E	Bank 2, RE	Bit Name	TCCY7	TCCY6	TCCY5	TCCY4	TCCY3	TCCY2	TCCY1	TCCY0

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TKCCR	Power-On	0	1	0	0	0	0	0	0
		/RESET and WDT	0	1	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	Bank 2, RF TKCSR	Bit Name	-	-	-	-	CS3	CS2	CS1	CS0
		Power-On	0	0	0	0	1	0	1	0
		/RESET and WDT	0	0	0	0	1	0	1	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X10	Bank 2, R10 TKCTR	Bit Name	TCT7	TCT6	TCT5	TCT4	TCT3	TCT2	TCT1	TCT0
		Power-On	0	1	0	0	0	0	0	0
		/RESET and WDT	0	1	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X11	Bank 2, R11 TKSWR	Bit Name	-	-	-	TSW4	TSW3	TSW2	TSW1	TSW0
		Power-On	0	0	0	0	1	0	1	0
		/RESET and WDT	0	0	0	0	1	0	1	0
		Wake-up from Sleep/Idle	0	0	0	P	P	P	P	P
0X12	Bank 2, R12 TKAH	Bit Name	TKA[15]	TKA[14]	TKA[13]	TKA[12]	TKA[11]	TKA[10]	TKA[9]	TKA[8]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X13	Bank 2, R13 TKAL	Bit Name	TKA[7]	TKA[6]	TKA[5]	TKA[4]	TKA[3]	TKA[2]	TKA[1]	TKA[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X14	Bank 2, R14 TKBH	Bit Name	TKB[15]	TKB[14]	TKB[13]	TKB[12]	TKB[11]	TKB[10]	TKB[9]	TKB[8]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X15	Bank 2, R15 TKBL	Bit Name	TKB[7]	TKB[6]	TKB[5]	TKB[4]	TKB[3]	TKB[2]	TKB[1]	TKB[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X16	Bank 2, R16 TKSCR	Bit Name	TKMCS1	TKMCS0	-	-	TKISE	TKST2	TKST1	TKST0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	0	0	P	P	P	P
0X17	Bank 2, R17 TKA1WBH	Bit Name	TA1WB[15]	TA1WB[14]	TA1WB[13]	TA1WB[12]	TA1WB[11]	TA1WB[10]	TA1WB[9]	TA1WB[8]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X18	Bank 2, R18 TKA1WBL	Bit Name	TA1WB[7]	TA1WB[6]	TA1WB[5]	TA1WB[4]	TA1WB[3]	TA1WB[2]	TA1WB[1]	TA1WB[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	Bank 2, R19 TKA1WR	Bit Name	TA1WR[7]	TA1WR[6]	TA1WR[5]	TA1WR[4]	TA1WR[3]	TA1WR[2]	TA1WR[1]	TA1WR[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1A	Bank 2, R1A TKA2WBH	Bit Name	TA2WB[15]	TA2WB[14]	TA2WB[13]	TA2WB[12]	TA2WB[11]	TA2WB[10]	TA2WB[9]	TA2WB[8]

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 2, R1B TKA2WBL	Bit Name	TA2WB[7]	TA2WB[6]	TA2WB[5]	TA2WB[4]	TA2WB[3]	TA2WB[2]	TA2WB[1]	TA2WB[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1C	Bank 2, R1C TKA2WR	Bit Name	TA2WR[7]	TA2WR[6]	TA2WR[5]	TA2WR[4]	TA2WR[3]	TA2WR[2]	TA2WR[1]	TA2WR[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	Bank 2, R1D TKB1WBH	Bit Name	TB1WB[15]	TB1WB[14]	TB1WB[13]	TB1WB[12]	TB1WB[11]	TB1WB[10]	TB1WB[9]	TB1WB[8]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1E	Bank 2, R1E TKB1WBL	Bit Name	TB1WB[7]	TB1WB[6]	TB1WB[5]	TB1WB[4]	TB1WB[3]	TB1WB[2]	TB1WB[1]	TB1WB[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1F	Bank 2, R1F TKB1WR	Bit Name	TB1WR[7]	TB1WR[6]	TB1WR[5]	TB1WR[4]	TB1WR[3]	TB1WR[2]	TB1WR[1]	TB1WR[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X20	Bank 2, R20 TKB2WBH	Bit Name	TB2WB[15]	TB2WB[14]	TB2WB[13]	TB2WB[12]	TB2WB[11]	TB2WB[10]	TB2WB[9]	TB2WB[8]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X21	Bank 2, R21 TKB2WBL	Bit Name	TB2WB[7]	TB2WB[6]	TB2WB[5]	TB2WB[4]	TB2WB[3]	TB2WB[2]	TB2WB[1]	TB2WB[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X22	Bank 2, R22 TKB2WR	Bit Name	TB2WR[7]	TB2WR[6]	TB2WR[5]	TB2WR[4]	TB2WR[3]	TB2WR[2]	TB2WR[1]	TB2WR[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X47	Bank 2, R47 LOCKPR	Bit Name	-	-	-	LOCKPR4	LOCKPR3	LOCKPR2	LOCKPR1	LOCKPR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	P	P	P	P	P
0X48	Bank 2, R48 LOCKCR	Bit Name	LOCKEN	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	0	0	0	0

6.5 Interrupt

The eKTF5616/08 has 21 interrupts (External, Internal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0	High 0
External	INT	ENI + EXIE=1	EXSF	2	1
External	Pin change	ENI +ICIE=1	ICSF	4	2
Internal	TCC	ENI + TCIE=1	TCSF	6	3
Internal	LVD	ENI+LVDEN & LVDIE=1	LVDSF	8	4
Internal	SPI	ENI + SPIIE=1	SPISF	C	5
Internal	AD	ENI + ADIE=1	ADSF	10	6
Internal	TC1	ENI + TC1IE=1	TC1SF	12	7
Internal	PWMPA	ENI+PWMAPIE=1	PWMAPSF	14	8
Internal	PWMDA	ENI+PWMADIE=1	PWMADSF	16	9
Internal	I2C Transmit	ENI+ I2CTIE	I2CTSF	1A	10
Internal	I2C Receive	ENI+ I2CRIE	I2CRSF	1C	11
Internal	I2CSTOP	ENI+ I2CSTPIE	I2CSTPSF	1E	12
Internal	PWMPB	ENI+PWMBPIE=1	PWMBPSF	24	13
	PWMDB	ENI+PWMBDIE=1	PWMBDSF	26	14
Internal	UART Receive error	ENI+UERRIE=1	UERRSF	2E	15
Internal	UART Receive	ENI + URIE=1	URSF	30	16
Internal	UART Transmit	ENI + UTIE=1	UTSF	32	17
Internal	System hold	ENI+SHIE=1	SHSF	3A	18
Internal	Touch Key	ENI+TKIE=1	TKSF	3C	19
Internal	Touch Key error	ENI+TKERRIE=1	TKPESF TKOESF	3E	20
Internal	Touch Key Idle with scan	ENI+TKCIE=1	TKCSF TKTOSF	40	21

Bank 0 R14~R19 are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank0 R1B~R20 are the interrupt Mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICSF bit which is set to “0”) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse of less than **4 System Clock Time** is eliminated as noise)**.** When an interrupt (Falling edge) is generated by the External interrupt (if enabled), the next instruction will be fetched from Address 002H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 (Bit 0~Bit 6) and R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3 (Bit 0~Bit 4), and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC, R3 (Bit 0~Bit 6), and R4 restore.

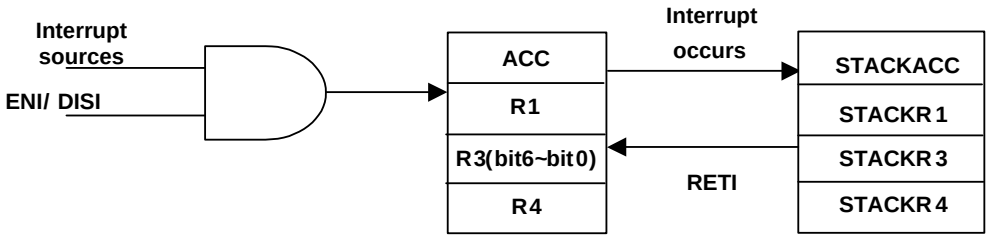


Figure 6-6a Interrupt Backup Diagram

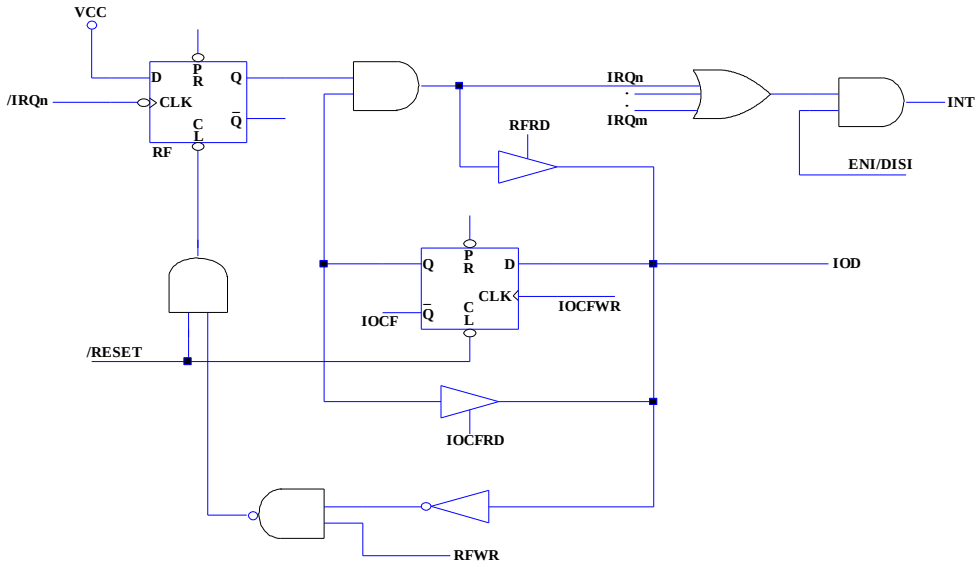


Figure 6-6b Interrupt Input Circuit

6.6 A/D Converter

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x3E	ADCR1	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x3F	ADCR2	-	VPIS2	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
			-	-	R/W	R/W	R/W	R/W	R/W	-
Bank 0	0x40	ADISR	-	-	-	-	ADIS3	ADIS2	ADIS1	ADIS0
			-	-	-	-	R/W	R/W	R/W	R/W
Bank 0	0x41	ADER1	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x43	ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
			R	R	R	R	R	R	R	R
Bank 0	0x44	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
			R	R	R	R	R	R	R	R
Bank 0	0x45	ADCVL	ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x46	ADCVH	-	-	-	-	ADCD11	ADCD10	ADCD9	ADCD8
			-	-	-	-	R/W	R/W	R/W	R/W
Bank 0	0x10	WUCR2	-	-	-	ADWK	-	-	-	-
			-	-	-	R/W	-	-	-	-
Bank 0	0x14	SFR1	-	-	-	ADSF	-	-	-	-
			-	-	-	R/W	-	-	-	-
Bank 0	0x1B	IMR1	-	-	-	ADIE	-	-	-	-
			-	-	-	R/W	-	-	-	-

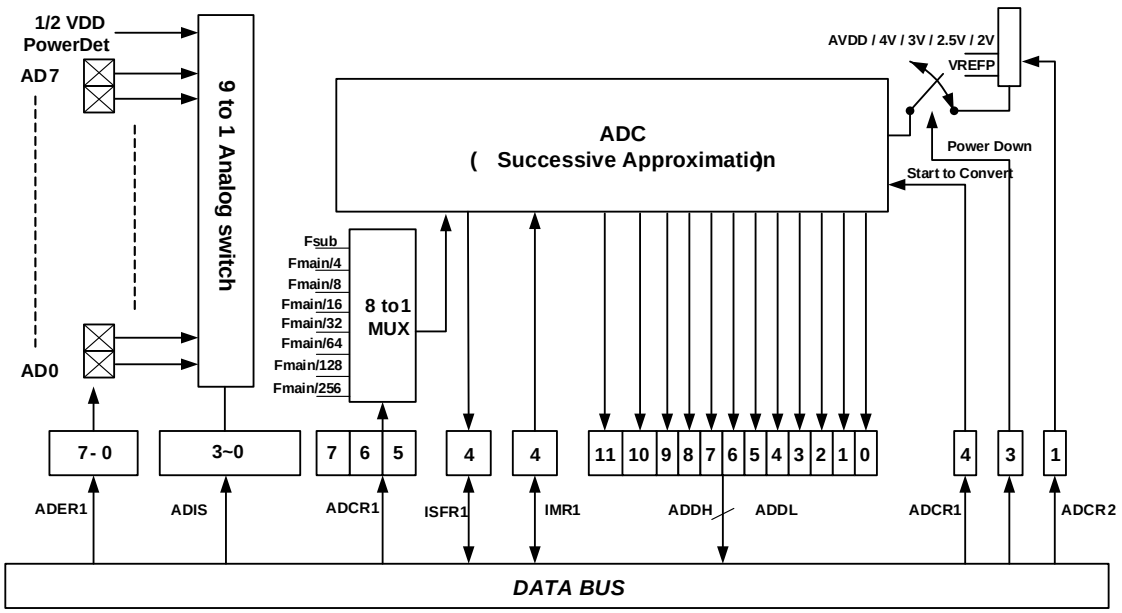


Figure 6-10 AD Converter Functional Block Diagram

This is a 12-bit successive approximation register analog-to-digital converter (SAR ADC). There are two reference voltages for SAR ADC. The positive reference voltage can select internal AVDD, internal voltage sources or external input pin by setting the VREFP and VPIS1~0 bits in ADCR2. Connecting to external positive reference voltage provides more accuracy than using internal AVDD.

6.6.1 ADC Data Register

When the AD conversion is completed, the result is loaded to the ADDH and ADDL. And the ADSF is set if ADIE is enabled.

6.6.2 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation AD converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample and hold capacitor. The application program controls the length of the sample time to meet the specified accuracy. The maximum recommended impedance for the analog source is 10kΩ at VDD = 5V. After the analog input channel is selected; this acquisition time must be done before AD conversion can be started.

6.6.3 A/D Conversion Time

CKR2~0 select the conversion time (TAD). This allows the MCU to run at maximum frequency without sacrificing the accuracy of AD conversion. The following tables show the relationship between T_{AD} and the maximum operating frequencies. The T_{AD} is 1μs for 3V~5.5V, T_{AD} is 4μs for 2.5V~3V and T_{AD} is 32μs for 2.2V~2.5V.

System Mode	CKR2~0	Clock Rate	Max. System Operation Frequency in 2.2~2.5V	Max. System Operation Frequency in 2.5~3V	Max. System Operation Frequency in 3~5.5V
Normal Mode	000	$F_{Main}/4$	-	-	-
	001	$F_{Main}/8$	-	-	8 MHz
	010	$F_{Main}/16$	-	-	16 MHz
	011	$F_{Main}/32$	-	8 MHz	16 MHz
	100	$F_{Main}/64$	-	12 MHz	16 MHz
	101	$F_{Main}/128$	-	16 MHz	16 MHz
	110	$F_{Main}/256$	8 MHz	16 MHz	16 MHz
	111	F_{Sub}	Fs	Fs	Fs
Green Mode	xxx	F_{Sub}	Fs	Fs	Fs

6.6.4 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all MCU operations will stop except for the Oscillator, TCC, TC1, PWM and AD conversion.

The AD Conversion is considered completed as determined by:

1. The ADRUN bit of the Bank 0-R3E register is cleared to “0”.
2. The ADSF bit of the Bank 0-R14 register is set to “1”.
3. The ADWK bit of the Bank 0-R10 register is set to “1”. Wakes up from ADC conversion (where it remains in operation during sleep mode).
4. Wake up and execution of the next instruction if the ADIE bit of the Bank 0-R1B is enabled and the “DISI” instruction is executed.
5. Wake up and enter into Interrupt vector if the ADIE bit of Bank 0-R1B is enabled and the “ENI” instruction is executed.
6. Enter into an Interrupt vector if the ADIE bit of the Bank 0-R1B is enabled and the “ENI” instruction is executed.

The results are fed into the ADDL and ADDH registers when the conversion is completed. If the ADWK is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADPD bit is.

6.6.5 Programming Process/Considerations

Follow these steps to obtain data from the ADC:

1. Write to the 8 bits (ADE7~0) on the Bank 0-R41(ADER1) register to define the characteristics of P80~P87 (digital I/O, analog channels, or voltage reference pin)
2. Write to the Bank 0-R3E~R41 register to configure the AD module:

a) Select the ADC input channel (ADIS4~0)
b) Define the AD conversion clock rate (CKR2~0)
c) Select the VREFS input source of the ADC
d) Set the ADP bit to “**1**” to begin sampling

3. Set the ADWK bit, if the wake-up function is employed
4. Set the ADIE bit, if the interrupt function is employed
5. Write “ENI” instruction, if the interrupt function is employed

6. Set the ADRUN bit to **"1"**
7. Write "SLEP" instruction or Polling.
8. Wait for either Wake-up or for the ADRUN bit to be cleared to "**0**" , and the Status flag (ADSF) is set "**1**", or ADC interrupt occurs.
9. Read the ADDL and ADDH conversion data registers. If the ADC input channel changes at this time, the ADDL and ADDH values can be cleared to "**0**".
10. Clear the status flag (ADSF).
11. For next conversion, go to Step 1 or Step 2 as required. At least two T_{AD} are required before the next acquisition starts. On the other hand, the timing setting ADRUN = 1 must be later than the timing setting ADPD=1, and the difference between the two timings is also two T_{AD}.

NOTE
In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion

6.6.6 Programming Process for Detecting Internal VDD

VDD is detected within the operation, as described in the previous section, the difference is that before starting the ADC conversion, the first detection of VDD is ready. Therefore in Detecting VDD:

It should be noted that before starting the AD conversion operation, the channel has to be switched to 1/2VDD channel, the voltage divider is started, then AD can be converted. Several points to note is that, precise conversion values can be added in the VDD Pin capacitance, or more than twice the conversion, taking the average or the last few strokes data in order to increase the reliability of the data.

Note that usually before VDD is detected, do not switch the channel to 1/2VDD channel. As it has always been a DC current consumption, it must be switched to another analog multiplexer channel, and will be shut out of the resistor divider, which requires user's attention.

6.7 Touch Key Sensor Function

The Touch Key Sensor provides multiple touch key sensing and calculating. The touch key function is fully integrated and does not require external components, allowing touch key functions to be implemented by the simple

6.7.1 Touch Key Function Block & Control Register

The Touch Key are pin shared with the P60~P67, P70~P73, P80~P83 I/O pins. Touch Key are organized into two groups. Each group supports 8 detected pins.

Touch Key group	Sensing I/O pins							
A	TK1	TK2	TK3	TK4	TK5	TK6	TK7	TK8
	P60	P61	P62	P63	P64	P65	P66	P67
B	TK9	TK10	TK11	TK12	TK13	TK14	TK15	TK16
	P70	P71	P72	P73	P80	P81	P82	P83

User can set the TKx Pin Control Register (TKAPC/TKBPC) to select this pin as Touch key function or GP I/O pin.

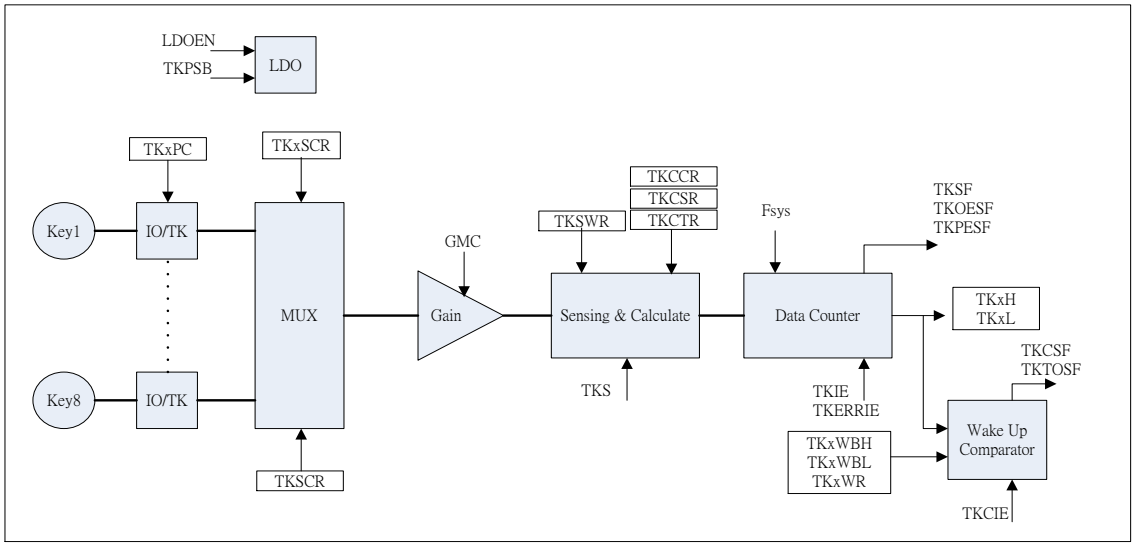
TKxEP7~0	Pin function
0	**GPIO or Other function**
1	**Touch Key Sensor**

Touch Key frequency table:

Internal RC Frequency	Touch Key Frequency
8MHz	24MHz
12MHz	24MHz
16MHz	16MHz

The following shows the touch key function block & control register

■ The Touch Key function Block:



X = A,B

■ Registers for Touch key circuit :

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	**0x19**	**SFR6**		-	-	TKTOSF	TKCSF	TKPESF	TKOESF	TKSF
				-	-	R/W	R/W	R/W	R/W	R/W
Bank 0	**0x20**	**IMR6**		-	-	-	TKC IE	-	TKERRIE	TKIE
				-	-	-	R/W	-	R/W	R/W
Bank 2	**0x0D**	**TKCR**	TKS	LDOEN	TKPSB	-	-	-	-	GMC
			R/W	R/W	R/W	-	-	-	-	R/W
Bank 2	**0x0E**	**TKCCR**	TCCY7	TCCY6	TCCY5	TCCY4	TCCY3	TCCY2	TCCY1	TCCY0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	**0x0F**	**TKCSR**	-	-	-	-	CS3	CS2	CS1	CS0
			-	-	-	-	R/W	R/W	R/W	R/W
Bank 2	**0x10**	**TKCTR**	TCT7	TCT6	TCT5	TCT4	TCT3	TCT2	TCT1	TCT0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	**0x11**	**TKSWR**	-	-	-	TSW4	TSW3	TSW2	TSW1	TSW0
			-	-	-	R/W	R/W	R/W	R/W	R/W
Bank 2	**0x16**	**TKSCR**	TKMCS1	TKMCS0	-	-	TKISE	TKST2	TKST1	TKST0
			R/W	R/W	-	-	R/W	R/W	R/W	R/W

■ **Registers for Touch key Group A :**

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 2	0x05	TKAPC	TKAEP7	TKAEP6	TKAEP5	TKAEP4	TKAEP3	TKAEP2	TKAEP1	TKAEP0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x07	TKASCR	TKAEN	-	-	-	-	TKASW2	TKASW1	TKASW0
			R/W	-	-	-	-	R/W	R/W	R/W
Bank 2	0x12	TKAH	TKA[15]	TKA[14]	TKA[13]	TKA[12]	TKA[11]	TKA[10]	TKA[9]	TKA[8]
			R	R	R	R	R	R	R	R
Bank 2	0x13	TKAL	TKA[7]	TKA[6]	TKA[5]	TKA[4]	TKA[3]	TKA[2]	TKA[1]	TKA[0]
			R	R	R	R	R	R	R	R
Bank 2	0x17	TKA1WBH	TA1WB[15]	TA1WB[14]	TA1WB[13]	TA1WB[12]	TA1WB[11]	TA1WB[10]	TA1WB[9]	TA1WB[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x18	TKA1WBL	TA1WB[7]	TA1WB[6]	TA1WB[5]	TA1WB[4]	TA1WB[3]	TA1WB[2]	TA1WB[1]	TA1WB[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x19	TKA1WR	TA1WR[7]	TA1WR[6]	TA1WR[5]	TA1WR[4]	TA1WR[3]	TA1WR[2]	TA1WR[1]	TA1WR[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x1A	TKA2WBH	TA2WB[15]	TA2WB[14]	TA2WB[13]	TA2WB[12]	TA2WB[11]	TA2WB[10]	TA2WB[9]	TA2WB[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x1B	TKA2WBL	TA2WB[7]	TA2WB[6]	TA2WB[5]	TA2WB[4]	TA2WB[3]	TA2WB[2]	TA2WB[1]	TA2WB[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x1C	TKA2WR	TA2WR[7]	TA2WR[6]	TA2WR[5]	TA2WR[4]	TA2WR[3]	TA2WR[2]	TA2WR[1]	TA2WR[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Registers for Touch key Group B :

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 2	0x06	TKBPC	TKBEP7	TKBEP6	TKBEP5	TKBEP4	TKBEP3	TKBEP2	TKBEP1	TKBEP0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x08	TKBSCR	TKBEN	-	-	-	-	TKBSW2	TKBSW1	TKBSW0
			R/W	-	-	-	-	R/W	R/W	R/W
Bank 2	0x14	TKBH	TKB[15]	TKB[14]	TKB[13]	TKB[12]	TKB[11]	TKB[10]	TKB[9]	TKB[8]
			R	R	R	R	R	R	R	R
Bank 2	0x15	TKBL	TKB[7]	TKB[6]	TKB[5]	TKB[4]	TKB[3]	TKB[2]	TKB[1]	TKB[0]
			R	R	R	R	R	R	R	R
Bank 2	0x1D	TKB1WBH	TB1WB[15]	TB1WB[14]	TB1WB[13]	TB1WB[12]	TB1WB[11]	TB1WB[10]	TB1WB[9]	TB1WB[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x1E	TKB1WBL	TB1WB[7]	TB1WB[6]	TB1WB[5]	TB1WB[4]	TB1WB[3]	TB1WB[2]	TB1WB[1]	TB1WB[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x1F	TKB1WR	TB1WR[7]	TB1WR[6]	TB1WR[5]	TB1WR[4]	TB1WR[3]	TB1WR[2]	TB1WR[1]	TB1WR[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x20	TKB2WBH	TB2WB[15]	TB2WB[14]	TB2WB[13]	TB2WB[12]	TB2WB[11]	TB2WB[10]	TB2WB[9]	TB2WB[8]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x21	TKB2WBL	TB2WB[7]	TB2WB[6]	TB2WB[5]	TB2WB[4]	TB2WB[3]	TB2WB[2]	TB2WB[1]	TB2WB[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0x22	TKB2WR	TB2WR[7]	TB2WR[6]	TB2WR[5]	TB2WR[4]	TB2WR[3]	TB2WR[2]	TB2WR[1]	TB2WR[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

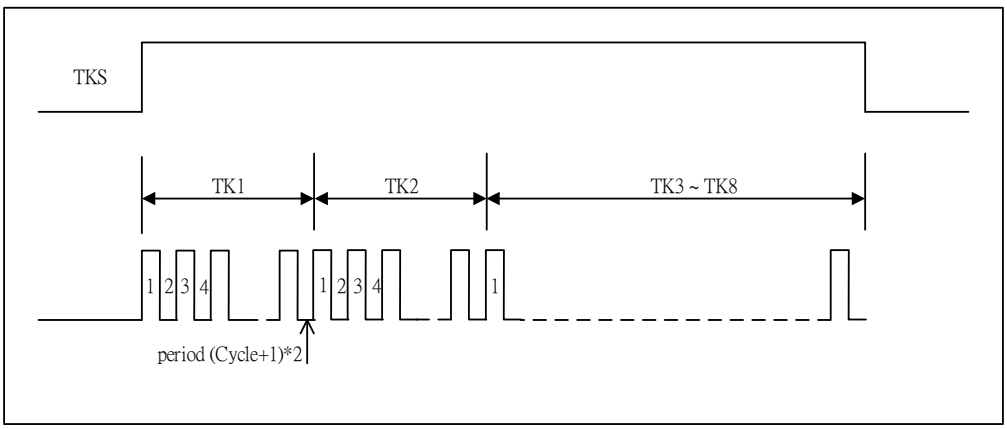
6.7.2 Touch Key Operation

When a finger touches, the capacitance of the pad will increase. By using sensing and calculate the capacitance variation to change to the counter data, user can set the sensed control register to get apposite counter data. touch actions can be sensed by measuring these counter data changes.

Each touch key group supports 8 detect pins. It senses pins by selecting TKx Select Pin Register (TKxSCR). User select the Touch pin one by one, then set the Start bit (TKxEN) to detect the capacitance.

TKxSW[2:0]	Sensing pin (TKA)	Sensing pin (TKB)
000	**TK1**	**TK9**
001	**TK2**	**TK10**
010	**TK3**	**TK11**
011	**TK4**	**TK12**
100	**TK5**	**TK13**
101	**TK6**	**TK14**
110	**TK7**	**TK15**
111	**TK8**	**TK16**

Each touch pin will sense (TKCCR+1)*2 periods. During each period, pin's capacitance is sensed and calculated. Accumulate multiple periods to get the counter data from register (TKAH_TKAL) or (TKBH_TKBL).

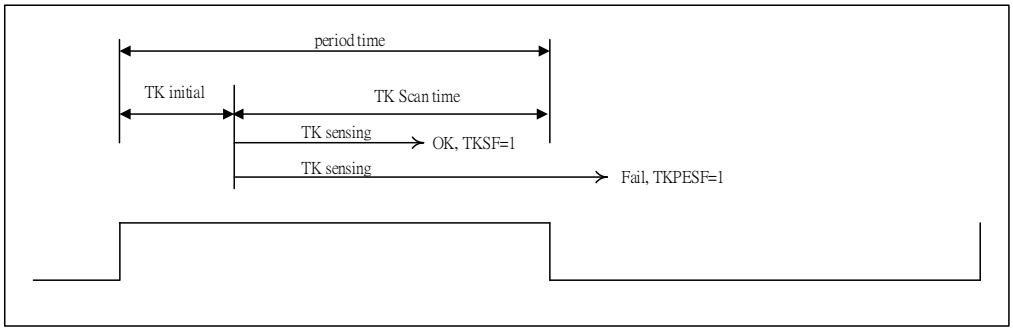


User can set the TKCTR register to control the Touch pin sensing frequency. If the TK scan time is less than the touch sensing time, TK Error Interrupt will happen, and the Touch Key Period Error status flag (TKPESF) will be set to 1.

Period time = TK initial time + TK scan time

= {[(TKCTR+1)*2+1] + [(TKCTR+1) * 16]} * 1/F_{TK}

Note: The TKCTR must be greater than 0x35.



Control the TKCSR register to adjust touch key sensitivity. TKCSR =0x00 has a higher sensitivity, whereas TKCSR= 0x0F has a lower sensitivity.

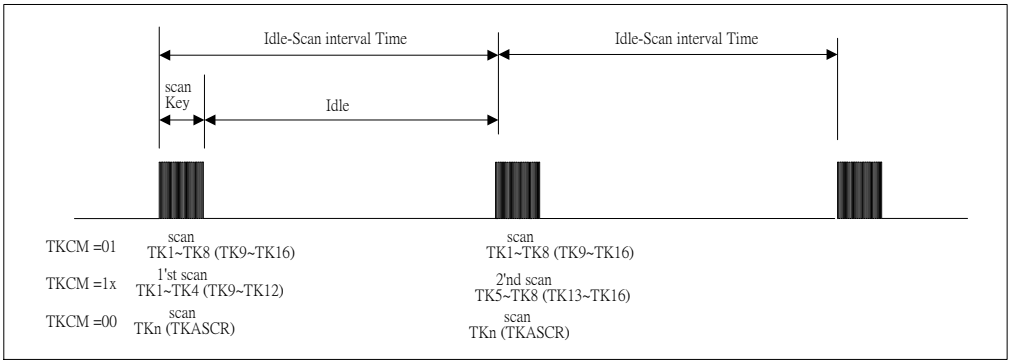
In some high noise environment or waterproof applications, user can adjust the TKSWR register to control the sensing detect window. TKSWR =0x00 is a small sensing window with less noise & sensing data. On the other hand, TKSWR =0x1F is a big sensing window with greater noise & sensing data.

6.7.3 Touch Key Idle-Scan mode

This body support Idle-Scan touch key in IDLE mode. User can enable it by setting the TKISE. In this mode, when the CPU enters into Idle mode, it will interval some time to scan the touch key automatically. Also, touch and pins will be combined to scan together.

TKST[2:0]	Idle-Scan interval Time (mS)
000	**12.5**
001	**25**
010	**50**
011	**100**
100	**200**
101	**400**
110	**800**
111	**1600**

TKMC[1:0]	Group A combine pins	Group B combine pins
00	**Not Combined, Only 1 Key with TKxSCR is selected**	
01	**TK1~ TK8**	**TK9~TK16**
10	**TK1~Tk4**	**TK9~TK12**
11	**TK5~TK6**	**TK13~TK16**



When the touch key scan data is greater than (TKxWBH_L + TKxWR) or less than (TKxWBH_L – TKxWR), the IC will wake up and TKCIE Interrupt will happen (TKCSF=1).

TKMC=01		Wakeup Base data	Wakeup Range data
Group A	TK1~TK8	TKA1WBH_L	TKA1WR
Group B	TK9~TK16	TKB1WBH_L	TKB1WR

TKMC=1x		Wakeup Base data	Wakeup Range data
Group A	TK1~TK4	TKA1WBH_L	TKA1WR
	TK5~TK8	TKA2WBH_L	TKA2WR
Group B	TK9~TK12	TKB1WBH_L	TKB1WR
	TK13~TK16	TKB2WBH_L	TKB2WR

In Idle scan mode, if no wake-up happens after scanning key for 16 times, it will automatically wake up one time and the TKTOSF=1. User can run the normal touch key scan to check the Touch level or go to Idle again.

6.8 Dual Set of PWM (Pulse Width Modulation)

6.8.1 Overview

In PWM mode, PWMA~B produce up to 16-bit resolution PWM outputs (see functional block diagram below). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The PWM baud rate is the inverse of the time period. Figure 6-7b *PWM Output Timing* below depicts the relationships between a time period and a duty cycle.

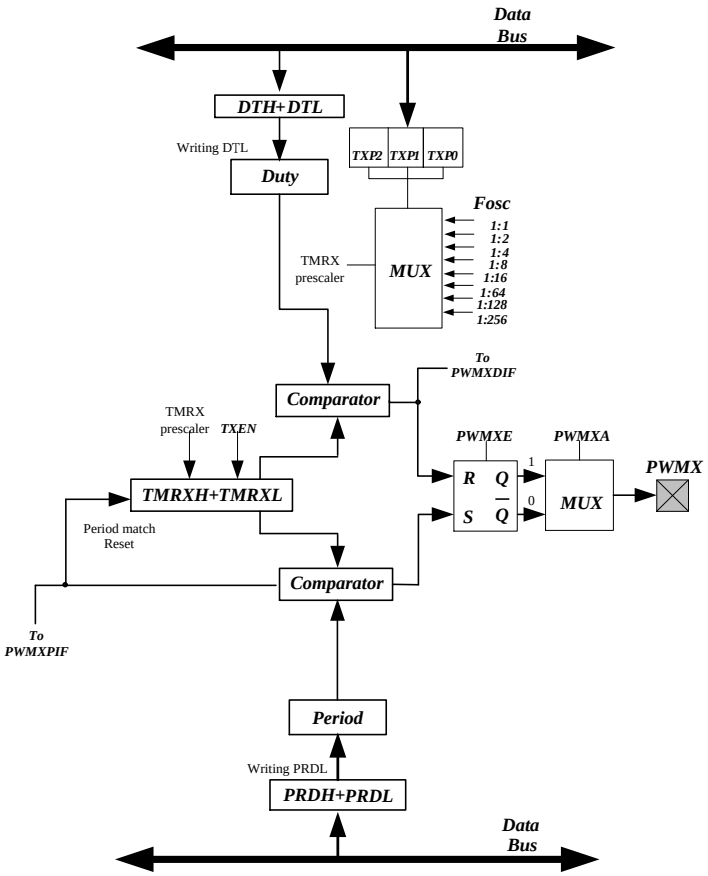


Figure 6-7a Dual PWMs Functional Block Diagram

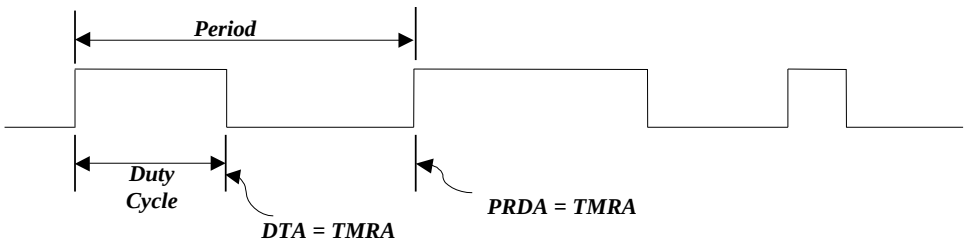


Figure 6-7b PWM Output Timing

6.8.2 Control Register

R_BANK	Addres	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x16	SFR3	-	-	-	-	PWMBPSF	PWMBDSF	PWMAPSF	PWMADSF
			-	-	-	-	F	F	F	F
Bank 0	0x1D	IMR3	-	-	-	-	PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
			-	-	-	-	R/W	R/W	R/W	R/W
Bank 1	0x16	PWMSCR	-	-	-	-	-	-	PWMBS	PWMAS
			-	-	-	-	-	-	R/W	R/W
Bank 1	0x17	PWMACR	PWMAE	-	-	-	TAEN	TAP2	TAP1	TAP0
			R/W	-	-	-	R/W	R/W	R/W	R/W
Bank 1	0x18	PRDAL	PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x19	PRDAH	PRDA15	PRDA14	PRDA13	PRDA12	PRDA11	PRDA10	PRDA9	PRDA8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1A	DTAL	DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1B	DTAH	DTA15	DTA14	DTA13	DTA12	DTA11	DTA10	DTA9	DTA8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1C	TMRAL	TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1D	TMRAH	TMRA15	TMRA14	TMRA13	TMRA12	TMRA11	TMRA10	TMRA9	TMRA8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1E	PWMBCR	PWMBE	-	-	-	TBEN	TBP2	TBP1	TBP0
			R/W	-	-	-	R/W	R/W	R/W	R/W
Bank 1	0x1F	PRDBL	PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x20	PRDBH	PRDB15	PRDB14	PRDB13	PRDB12	PRDB11	PRDB10	PRDB9	PRDB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x21	DTBL	DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x22	DTBH	DTB15	DTB14	DTB13	DTB12	DTB11	DTB10	DTB9	DTB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x23	TMRBL	TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x24	TMRBH	TMRB15	TMRB14	TMRB13	TMRB12	TMRB11	TMRB10	TMRB9	TMRB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.8.3 Increment Timer Counter (TMRX: TMRxH/TMRxL)

TMRXs are 16-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMR can be read only. If employed, they can be turned off for power saving by setting the TxEN Bit to "**0**". TMRA and TMRB are internal designs and cannot be read.

6.8.4 PWM Time Period (PRDX: PRDxL/H)

The PWM time period has a 16-bit resolution and is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

1) TMRX is cleared

2) The PWMX pin is set to "**1**"

NOTE

*The PWM output cannot be set if the duty cycle is "**0**."*

3) The PWMXPSF bit is set to "**1**"

To calculate PWM time period, use the following formula**:**

Example:

PRDX = 49; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1;

Then

$$Period = (49+1) \times \left(\frac{1}{4M}\right) \times 1 = 12.5\mu s$$

6.8.5 PWM Duty Cycle (DTX: DTxH/DT1L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at anytime, however it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula shows how to calculate the PWM duty cycle**:**

$$Duty\ cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX\ \ prescale\ value)$$

Example:

DTX = 10; **Fosc = 4 MHz;** **TMRX (0, 0, 0) = 1 : 1;**

Then

$$Duty\ cycle\ =\ (10)\ \times\ \left(\frac{1}{4M}\right)\ \times\ 1\ =\ 2.5\mu s$$

6.8.6 PWM Programming Process/Steps

1) Load the PWM duty cycle to DT
2) Load the PWM time period to PRD
3) Enable the interrupt function by writing Bank0-R1D, if required
4) Load a desired value for the timer prescaler
5) Enable PWMX function (i.e., enable PWMXE control bit)
6) Finally, enable TMRX function (i.e., enable TXEN control bit)

If the application needs to change PWM duty and period cycle at run time, refer to the following programming steps:

1) Load new duty cycle (if using dual PWM function) at any time.
2) Load new period cycle. You must take note of the order of loading period cycle. As the low byte of PWM period cycle is assigned a value, the new PWM cycle is loaded into a circuit.
3) The circuit will automatically update the new duty and period cycles to generate new PWM waveform at the next PWM cycle.

6.9 Timer

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x24	TC1CR1	TC1S	TC1RC	TC1SS1	-	TC1FF	TC1OMS	TC1IS1	TC1IS0
			R/W	R/W	R/W	-	R	R/W	R/W	R/W
Bank 0	0x25	TC1CR2	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x26	TC1DA	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x27	TC1DB	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x15	SFR2	-	-	-	-	-	-	-	TC1SF
			-	-	-	-	-	-	-	F
Bank 0	0x1C	IMR2	-	-	-	-	-	-	-	TC1IE
			-	-	-	-	-	-	-	R/W

6.9.1 Timer/Counter Mode

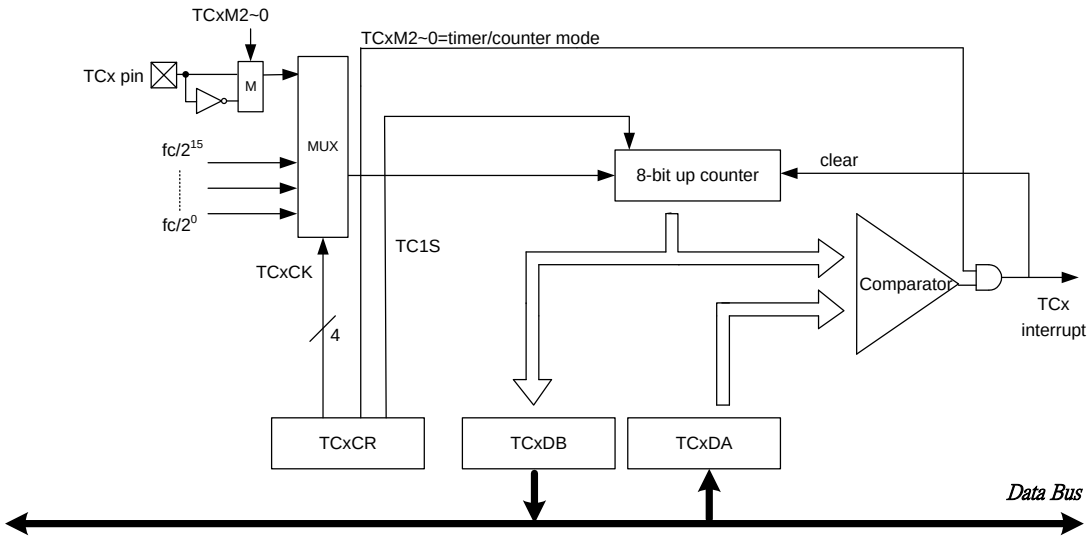


Figure 6-12a Timer/Counter Mode Block Diagram

In Timer/Counter mode, counting up is performed using internal clock or TCx pin. When the contents of the up-counter are matched with the TCxDA, an interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCxDB by setting TCxRC to “1”.

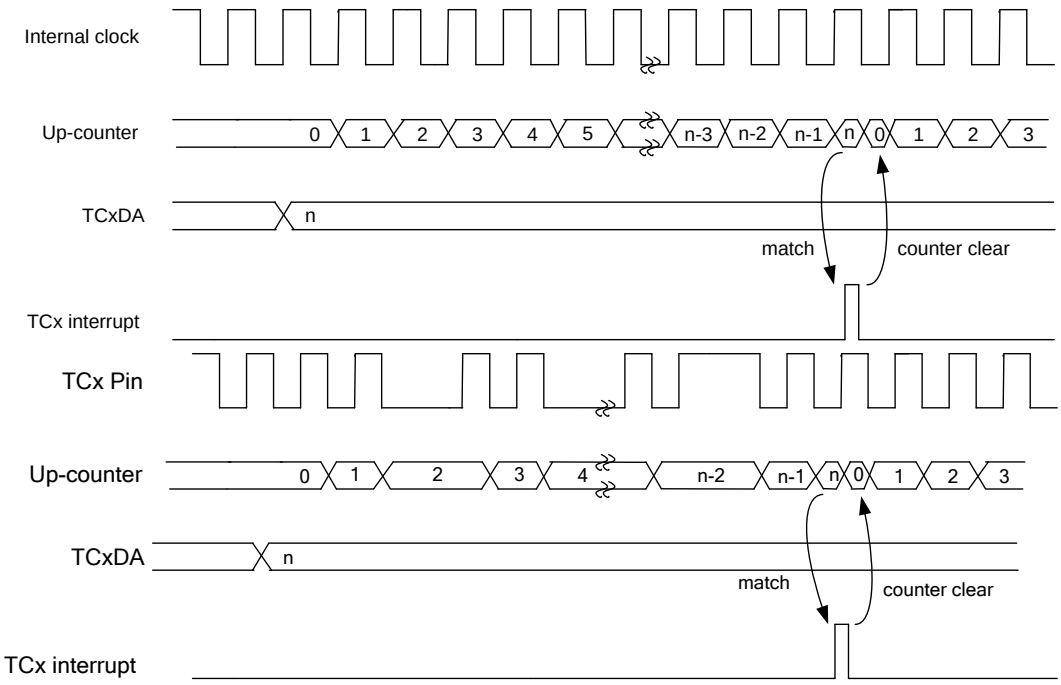


Figure 6-12b Timer/Counter Mode Waveform

6.9.2 Window Mode

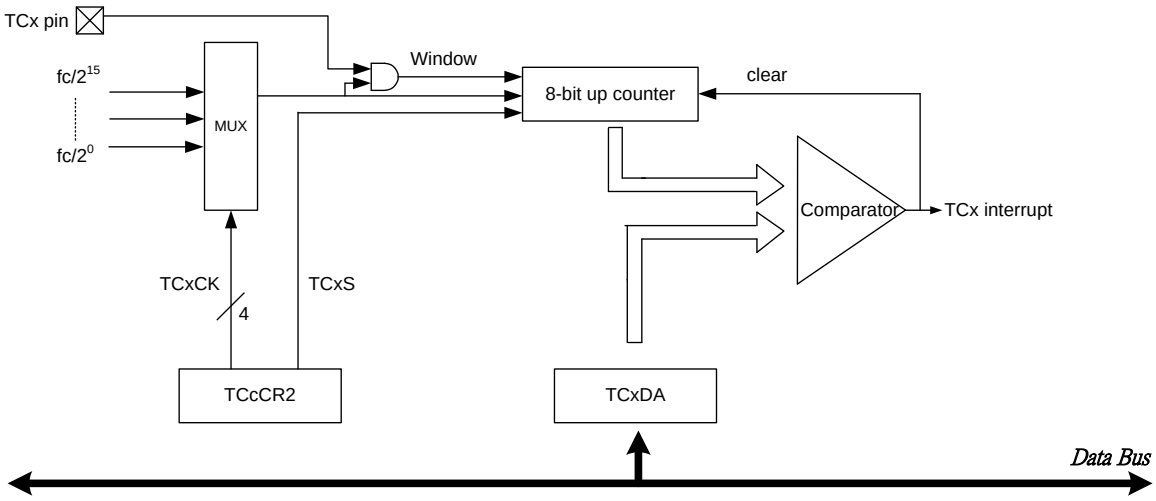


Figure 6-13a Window Mode Block Diagram

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TCx pin (window pulse). When the contents of the up-counter are matched with the TCxDA, interrupt is generated and the counter is cleared. The frequency (window pulse) must be lower than the selected internal clock.

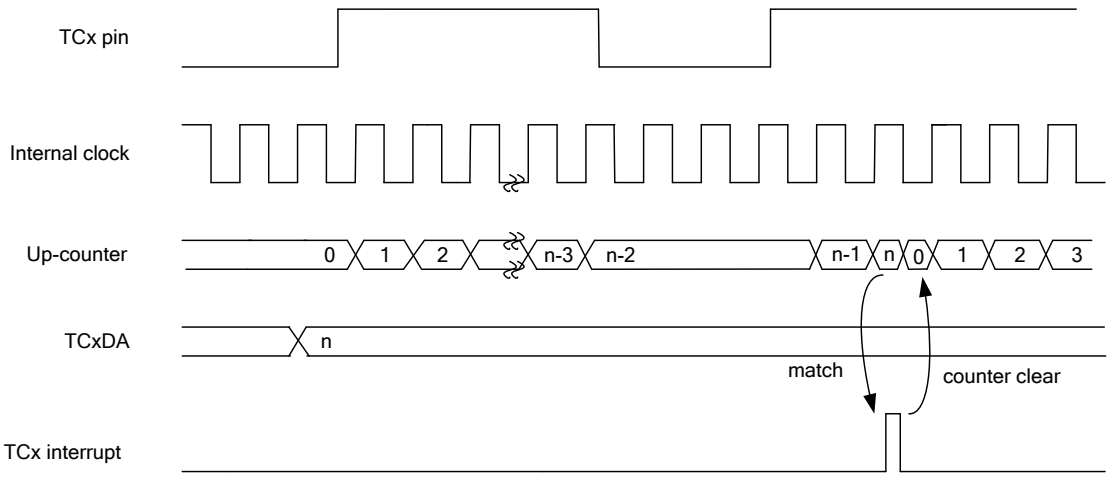


Figure 6-13b Window Mode Waveform

6.9.3 Capture Mode

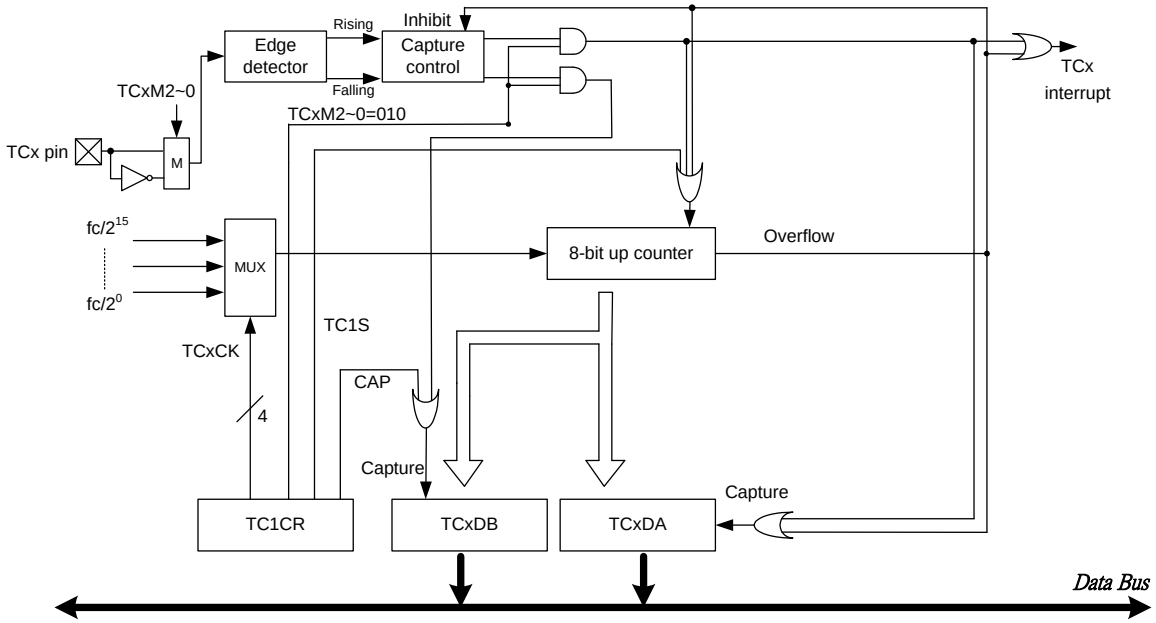


Figure 6-14a Capture Mode Block Diagram

In Capture mode, the pulse width, period and duty of the TCx input pin are measured and can be used to decode the remote control signal. The counter is free running by the internal clock. On a rising (falling) edge of TCx pin, the contents of the counter are loaded into TCxDA, then the counter is cleared and interrupt is generated. On a falling (rising) edge of TC1 pin, the contents of the counter are loaded into TCxDB. At this time, the counter is still counting. Once the next rising edge of TCx pin is triggered, the contents of the counter are loaded into TCxDA, the counter is cleared and interrupt is generated once again. If overflow before the edge is detected, the FFH is loaded into TCxDA and an overflow interrupt is generated. During interrupt processing, user can determine whether or not there is an overflow by checking if the TCxDA value is FFH. After an interrupt (capture to TCxDA or overflow detection) is generated, capture and overflow detection are halted until TCxDA is read out.

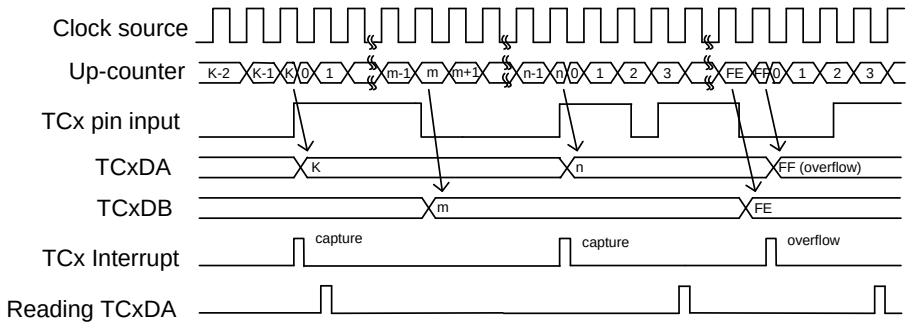


Figure 6-14b Capture Mode Waveform

6.9.4 Programmable Divider Output Mode and Pulse Width Modulation Mode

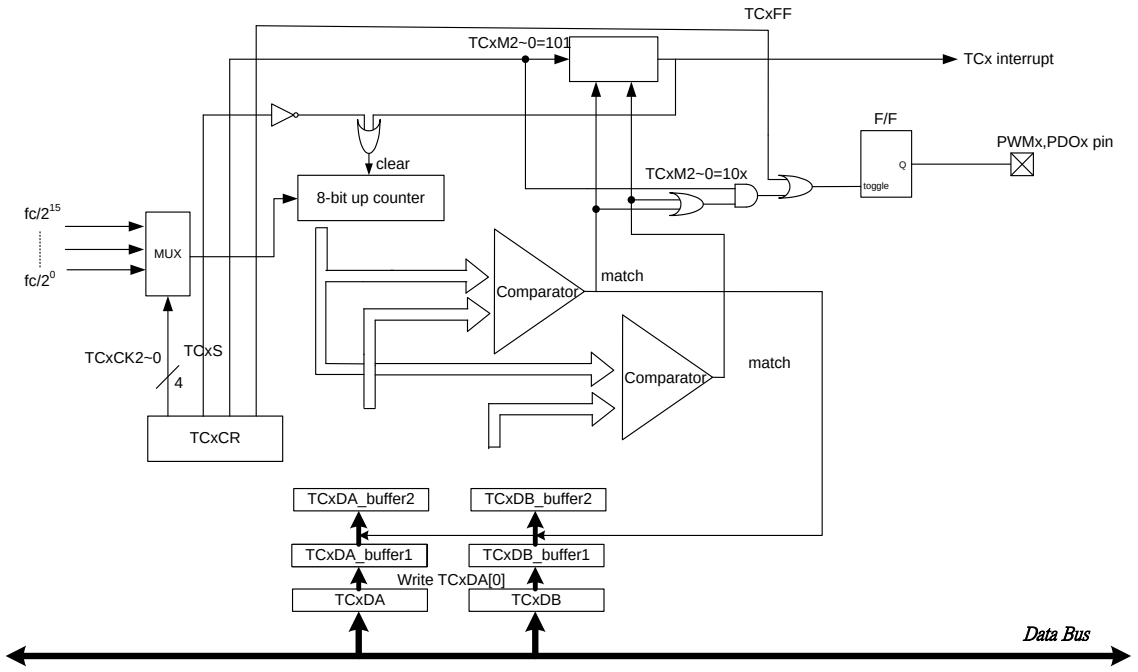


Figure 6-15a PDO/PWM Mode Block Diagram

■ **Programmable Divider Output (PDO)**

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCxDA are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to PDO pin. This mode can generate 50% of the duty pulse output. The PDO pin is initialized to "**0**" during reset. A TCx interrupt is generated each time the PDO output is toggled.

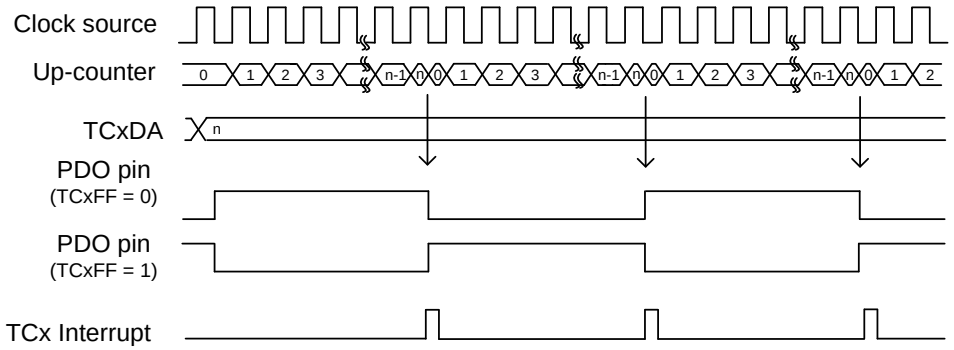


Figure 6-15b PDO Mode Waveform

- **Pulse Width Modulation (PWM)**

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock with prescaler. The Duty of PWMx is controlled by TCxDB, and the period of PWMx is controlled by TCxDA. The pulse at the PWMx pin is held to high levels as long as TCxS=1 or timerx matches TCxDA, while the pulse is held to low levels as long as Timerx matches TCxDB. Once TCxFF is set to 1, PWMx signal is inverted. A TCx interrupt is generated and defined by TCxIS. On the other hand, the TCxDA and TCxDB can be written anytime, but the data of TCxDA and TCxDB can only be latched when writing TCxDA0. Therefore, the new duty and new period of PWM appear at the PMW pin during the last period–match.

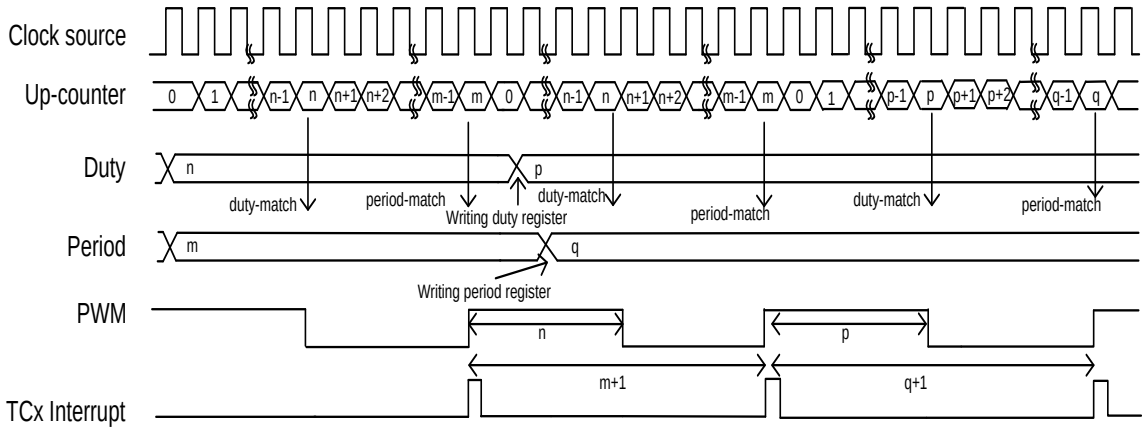


Figure 6-15c PWM Mode Waveform

6.9.5 Buzzer Mode

The TCx pin outputs the clock after dividing the frequency.

6.10 SPI (Serial Peripheral Interface)

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X36	SPICR	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
			R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Bank 0	0X37	SPIS	DORD	TD1	TD0	-	OD3	OD4	-	RBF
			R/W	R/W	R	-	R/W	R/W	-	R/W
Bank 0	0X38	SPIR	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
			R	R	R	R	R	R	R	R
Bank 0	0X39	SPIW	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X17	SFR4	-	-	-	-	SPISF	-	-	-
			-	-	-	-	R/W	-	-	-
Bank 0	0X1E	IMR4	-	-	-	-	SPIIE	-	-	-
			-	-	-	-	R/W	-	-	-

6.10.1 Overview and Features

■ **Overview:**

Figures 6-8a and 6-8b show how the eKTF5616/08 communicates with other devices through SPI module. If the eKTF5616/08 is the Master controller, it will send clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the eKTF5616/08 is defined as a Slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both clock rate and the selected edge. User can also set the –

- SPIS Bit 7 (DORD) to determine the SPI transmission order,
- SPICR Bit 3 (SDOC) to control SDO pin after serial data output status,
- SPIS Bit 6 (TD1) and Bit 5 (TD0) to determine the SDO status output delay times.

■ **Features:**

1) Operation in either Master mode or Slave mode
2) Three-wire or four-wire full duplex synchronous communication
3) Programmable baud rates of communication
4) Programmable clock polarity (Bank 0 R36 Bit 7)
5) Interrupt flag available for read buffer full
6) SPI transmission order
7) SDO status select after serial data output
8) SDO status output delay time
9) SPI handshake pin
10) Up to 8 MHz (maximum) bit frequency

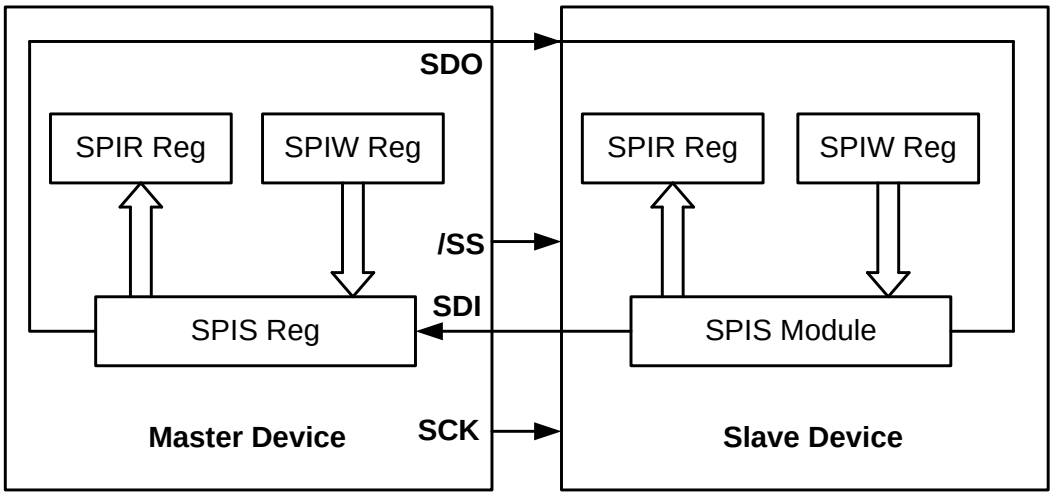


Figure 6-8a SPI Master/Slave Communication Block Diagram

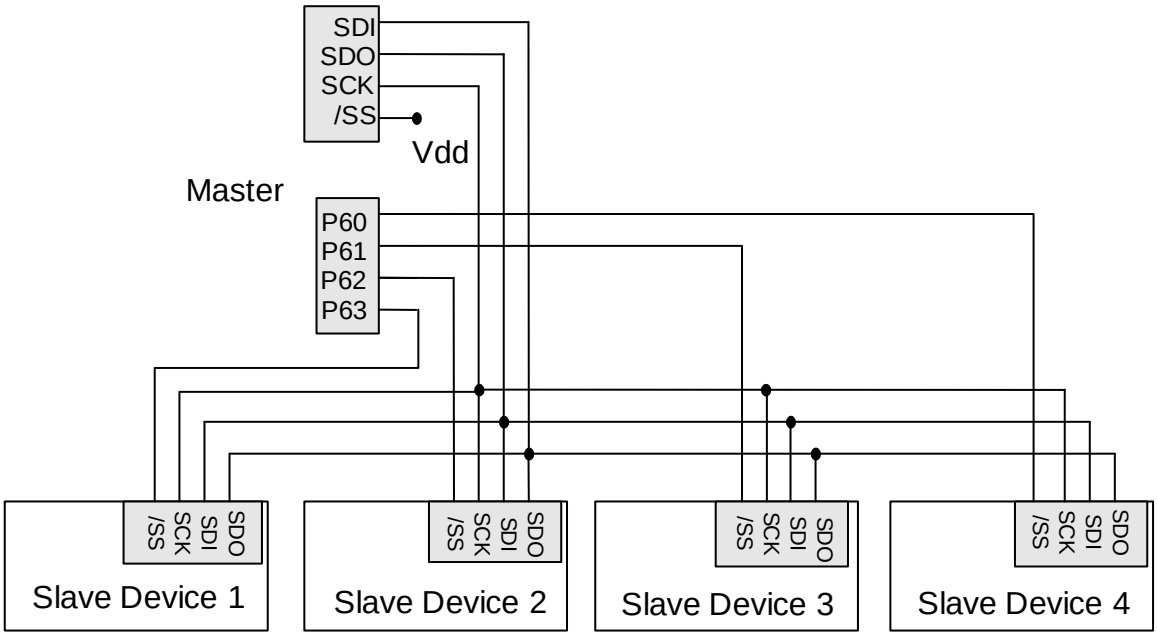


Figure 6-8b Single-Master and Multi-Slave SPI Configuration

6.10.2 SPI Function Description

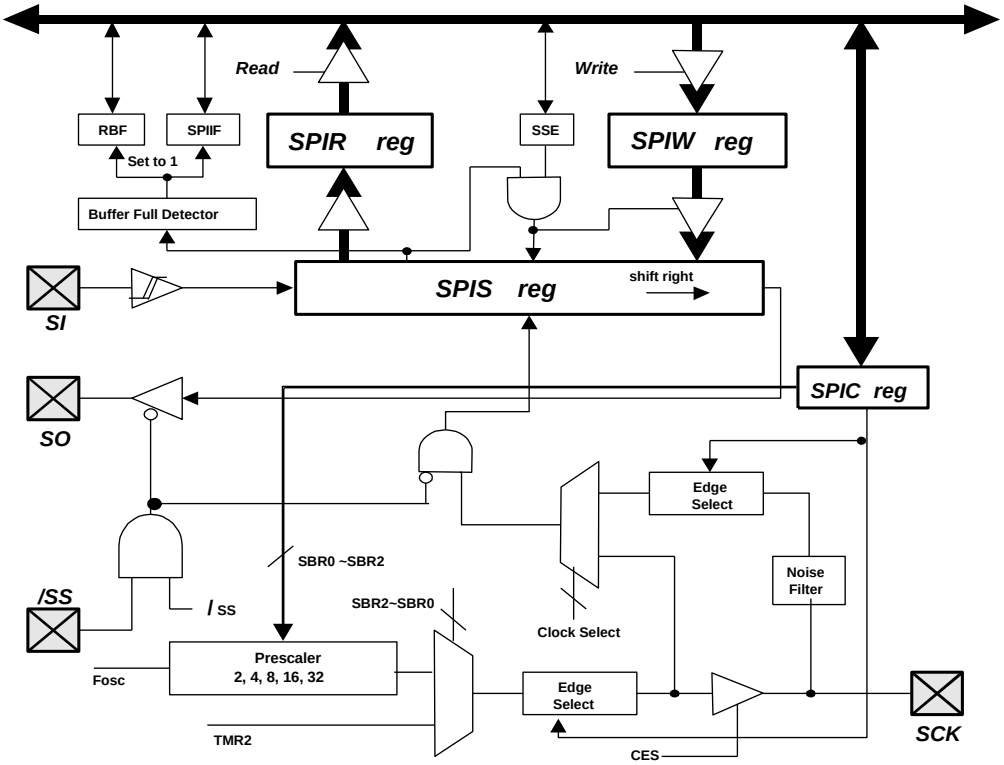


Figure 6-9a SPI Function Block Diagram

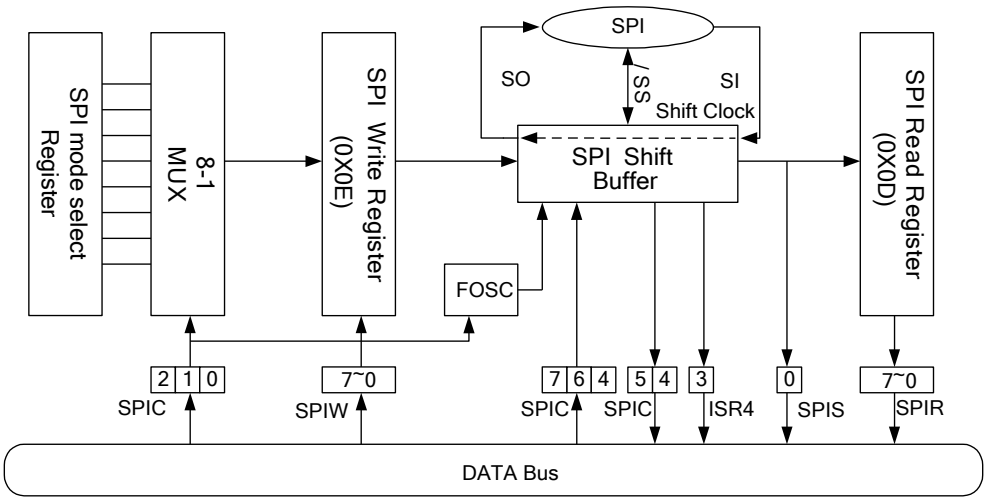


Figure 6-9b SPI Transmission Function Block Diagram

The following explains the functions of each block in the above figures as SPI carries out communication with the depicted signals:

- **P51/SI:** Serial Data In
- **P52/SO:** Serial Data Out
- **P53/SCK:** Serial Clock
- **P50//SS:** /Slave Select (Option). This pin (/SS) may be required during Slave mode.
- **RBF:** Set by Buffer Full Detector
- **Buffer Full Detector:** Set to 1 when an 8-bit shifting is completed.
- **SSE:** Load the data in SPIS register, and begin shifting. The SSE bit will be kept in "**1**" if the communication is still undergoing. This flag must be cleared as shifting is completed. You can determine if the next write attempt is available.
- **SPIS reg.:** Shifting byte in and out. The MSB is shifted first. Both the SPIR and the SPIW registers are shifted at the same time. Once data is written, SPIS starts transmitting/receiving. The received data will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPISF (SPI Interrupt) flag are then set.
- **SPIR reg.:** Read buffer. The buffer is updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- **SPIW reg.:** Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.
- **SBRS2~SBRS0:** Programming of the clock frequency/rates and sources.
- **Clock Select:** Select either the internal or the external clock as shifting clock.
- **Edge Select:** Select the appropriate clock edges by programming the CES bit

6.10.3 SPI Signal and Pin Description

The detailed functions of the four pins, SI, SO, SCK, and /SS are as follows**:**

- **P52/SI/TPA2:**

- Serial Data In
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Defined as high-impedance if not selected.

- Program the same clock rate and clock edge to latch on both Master and Slave devices.
- The byte received will update the transmitted byte.
- The RBF will be set as the SPI operation is completed.
- Timing is shown in Figures 6-10a and 6-10b below.

■ **P52/SO:**

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Program the same clock rate and clock edge to latch on both the Master and Slave devices.
- The received byte will update the transmitted byte.
- The CES bit is reset, as the SPI operation is completed.
- Timing is shown in Figures 6-10a and 6-10b.

■ **P53/SCK:**

- Serial Clock
- Generated by a Master device
- Synchronize the data communication on both the SI and SO pins.
- The CES is used to select the edge to communicate.
- The SBR0~SBR2 is used to determine the baud rate of communication.
- The CES, SBR0, SBR1, and SBR2 bits have no effect in Slave mode.
- Timing is shown in Figures 6-10a and 6-10b.

■ **P50//SS:**

- Slave Select; negative logic.
- Generated by a Master device to indicate the Slave(s) has to receive data.
- Go low before the first cycle of SCK occurs, and remain low until the last (8th) cycle is completed
- Ignore the data on the SI and SO pins when /SS is high, because SO is no longer driven
- Timing is shown in Figures 6-10a and 6-10b.

6.10.4 SPI Mode Timing

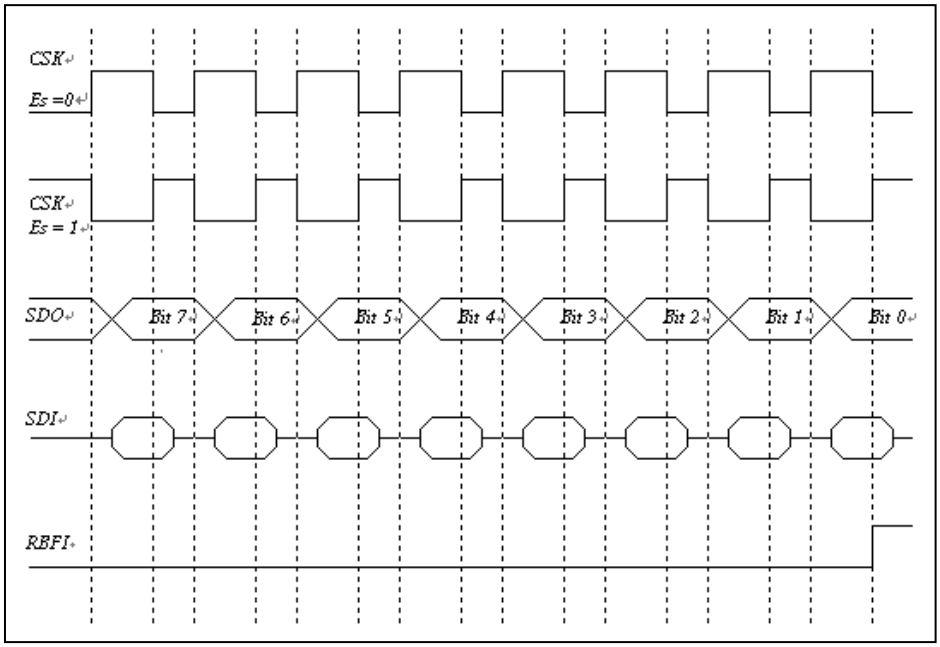


Figure 6-10a SPI Mode with /SS Disabled Timing Diagram

The SCK edge is selected by programming the bit CES. The waveform shown in Figure 6-10a above is applicable regardless of whether the eKTF5616/08 is in Master or Slave mode with /SS disabled. However, the waveform in Figure 6-10b below can only be implemented in Slave mode with /SS enabled.

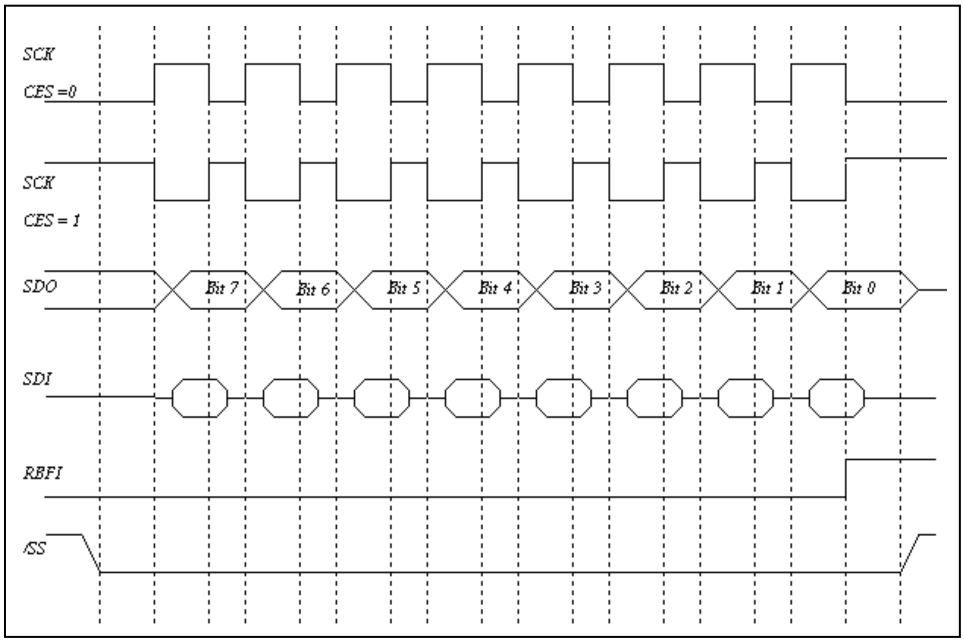


Figure 6-10b SPI Mode with /SS Enabled Timing Diagram

6.11 UART (Universal Asynchronous Receiver/Transmitter)

Registers for UART Circuit

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x15	SFR2	-	-	UERRSF	URSF	UTSF	-	-	-
			-	-	R/W	R/W	R/W	-	-	-
Bank 0	0x1C	IMR2	-	-	UERRIE	URIE	UTIE	-	-	-
			-	-	R/W	R/W	R/W	-	-	-
Bank 1	0X33	URCR	UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X34	URS	URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
			W	R/W	R/W	R/W	R/W	R/W	R	R/W
Bank 1	0x35	URTD	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
			W	W	W	W	W	W	W	W
Bank 1	0X36	URRDL	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
			R	R	R	R	R	R	R	R
Bank 1	0X37	URRDH	URRD8	-	-	-	-	-	-	URSS
			R	-	-	-	-	-	-	R/W

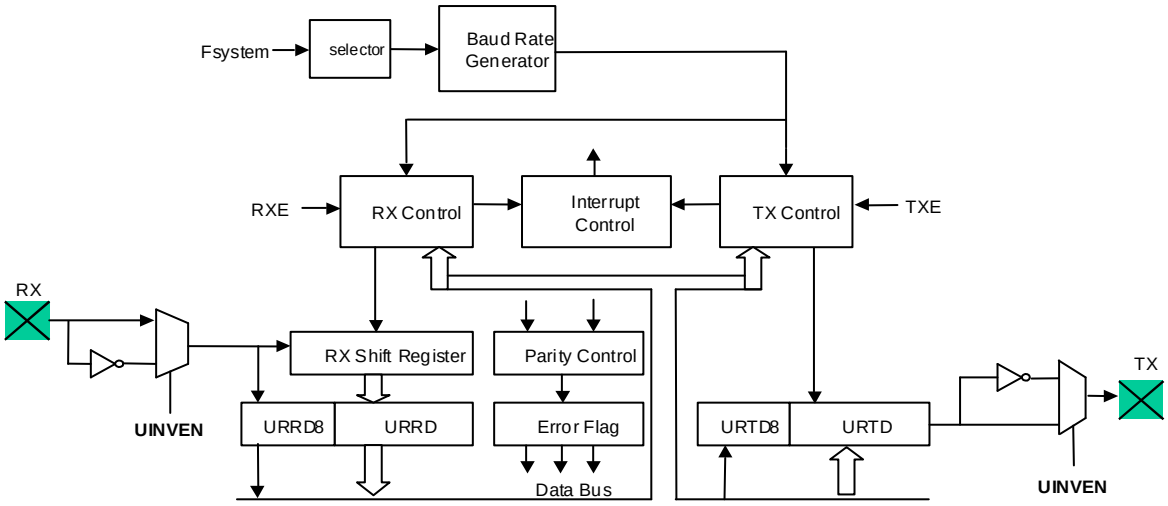


Figure 6-16 UART Functional Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and a stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on a falling edge of the start bit. When two or three “0”s are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

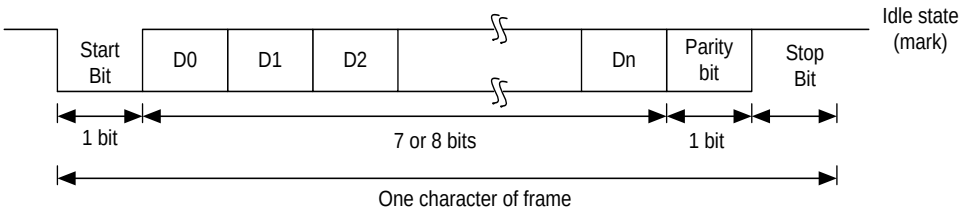


Figure 6-17 Data Format in UART

6.11.1 UART Mode

There are three UART modes. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. Figure 6-18a below shows the data format in each mode.

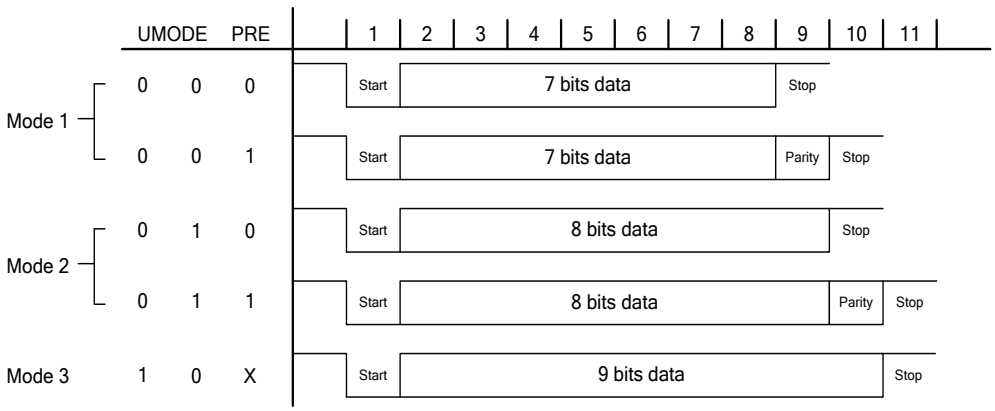


Figure 6-18a UART Model

6.11.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URCR1 register to enable the UART transmission function.
2. Write data into the URTD register and the UTBE bit of the URCR register will be cleared by hardware.
3. Then start transmitting.
4. Serially transmitted data are transmitted in the following order from the TX pin.
5. Start bit: one "**0**" bit is output.
6. Transmit data: 7, 8 or 9 bits' data are outputs from the LSB to the MSB.
7. Parity bit: one parity bit (odd or even selectable) is output.
8. Stop bit: one "**1**" bit (stop bit) is output.

Mark state: output "1" continues until the start bit of the next transmitted data.

After transmitting the stop bit, the UART generates a UTSF interrupt (if enabled).

6.11.3 Receiving

In receiving, the UART operates as follows:

1. Set the RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Received data is shifted into the URRD register in the order of LSB to MSB.
3. The parity bit and the stop bit are received. After one character is received, the URBF bit of the URS register will be set to "**1**". This means UART interrupt will occur.
4. The UART conducts the following checks:
   (a) Parity check: The number of "1" of the received data must match the even or odd parity setting of the EVEN bit in the URS register.
   (b) Frame check: The start bit must be "0" and the stop bit must be "1".
   (c) Overrun check: The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before the next received data is loaded into the URRD register.

   If any checks failed, the UERRSF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software, otherwise, UERRSF interrupt will occur when the next byte is received.
5. Read received data from URRD register. And URBF bit will be set by hardware.

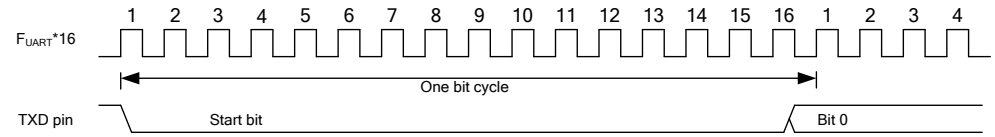
6.11.4 Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

The BRATE2~BRATE0 bits of the URC register can determine the desired baud rate.

6.11.5 UART Timing

1. Transmission Counter Timing:



2. Receiving Counter Timing:

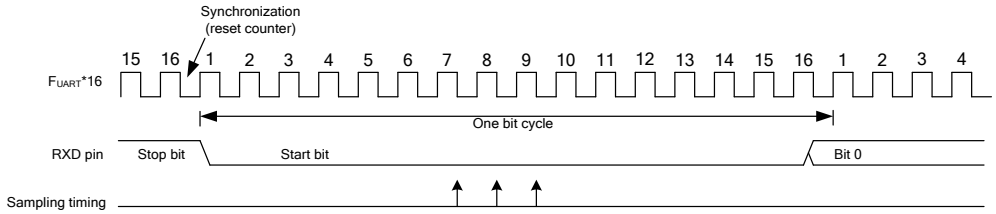


Figure 6-18b UART Timing Diagrams

6.12 I2C Function

The I^2C function and transmit/receive pin are enabled by default when eKTF5616/08 is powered-on.

■ **Registers for I^2C circuit:**

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x30	I2CCR1	Strobe /Pend	IMS	ISS	STOP	SAR_ EMPTY	ACK	FULL	EMPTY
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x31	I2CCR2	I2CBF	GCEN	I2COPT	BBF	I2CTS2	I2CTS1	I2CTS0	I2CEN
			R	R/W	R/W	R	R/W	R/W	R/W	R/W
Bank 0	0x32	I2CSA	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x33	I2CDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x34	I2CDAL	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x35	I2CDAH	-	-	-	-	-	-	DA9	DA8
			-	-	-	-	-	-	R/W	R/W
Bank 0	0x17	SFR4	-	-	-	-	-	I2CSTPIF	I2CRSF	I2CTSF
			-	-	-	-	-	R/W	R/W	R/W
Bank 0	0x1E	IMR4	-	-	-	-	-	I2CSTPIE	I2CRIE	I2CTIE
			-	-	-	-	-	R/W	R/W	R/W

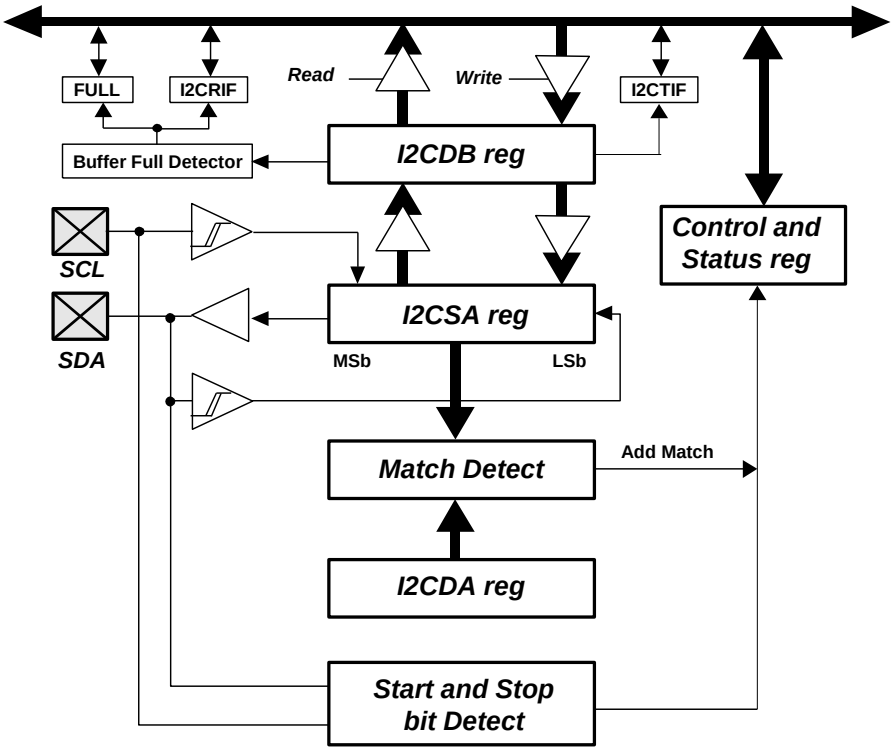


Figure 6-11 eKTF5616/08 I²C Block Diagram

The eKTF5616/08 supports a bidirectional, 2-wire bus, 7/10-bit addressing, and data transmission protocol. A device sending data to the bus is defined as transmitter, while a device receiving the data is defined as a receiver. The bus has to be controlled by a Master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions. Both Master and Slave can operate as transmitter or receiver, but the Master device determines which mode is activated.

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. The output stages of the devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I²C-bus can be transferred at the rates of up to 100 kbit/sec in Standard-mode or up to 400 kbit/sec in Fast-mode.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW.

The I^{2}C interrupt occurs as describe below**:**

Condition	Master/Slave	Transmit Address	Transmit Data	Stop
Master Transmitter (transmits to Slave-Receiver)	Master	Transmit interrupt	Transmit interrupt	NA
	Slave	Receive interrupt	Receive interrupt	Stop interrupt
Master Receiver (read Slave-Transmitter)	Master	Transmit interrupt	Receive interrupt	NA
	Slave	Transmit interrupt	Transmit interrupt	Stop interrupt

Within the procedure of the I^{2}C bus, unique situations could arise which are defined as START (S) and STOP (P) conditions.

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

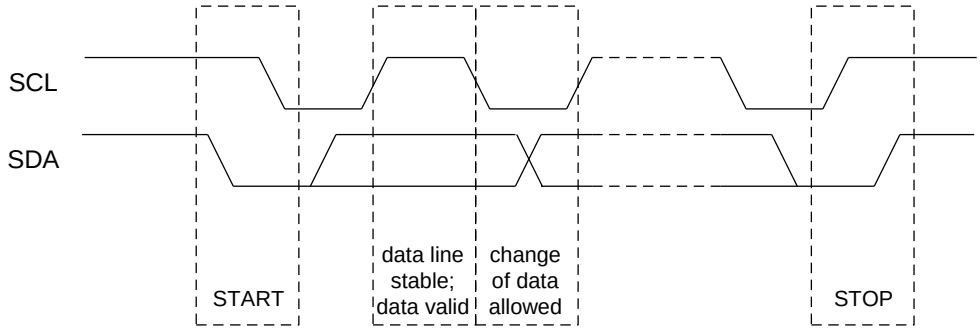


Figure 6-12 I^{2}C Transfer Condition

6.12.1 7-Bit Slave Address

Master-transmitter transmits to Slave-receiver. The transfer direction is not changed.

Master reads Slave immediately after the first byte. At the moment of the first acknowledgement, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave-transmitter. This first acknowledgement is still generated by the Slave. The STOP condition is generated by the Master, which has previously sent a Not-Acknowledge (A). The only difference between Master-transmitter and Master-receiver is their R//W bits. If the R//W bit is "**0**", the Master device would be a transmitter. Otherwise, the Master device would be a receiver (R//W Bit = "**1**").

Communications between the Master-transmitter/receiver and Slave-transmitter/receiver are illustrated in the following Figures 6-13a and 6-13b.

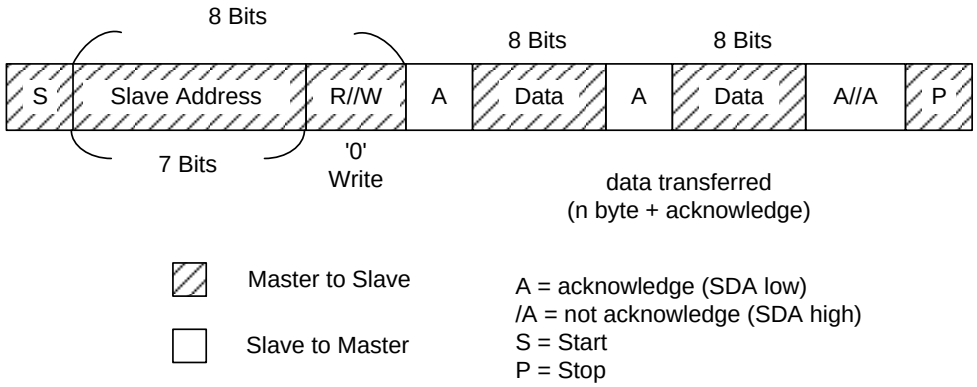


Figure 6-13a Master-Transmitter Transmits to Slave-Receiver with 7-Bit Slave Address

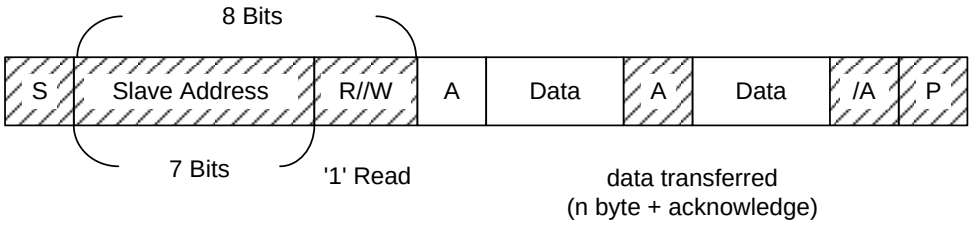


Figure 6-13b Master-Receiver Reads from Slave-Transmitter with 7-Bit Slave Address

6.12.2 10-Bit Slave Address

In 10-Bit Slave address mode, using 10-bit for addressing exploits the reserved combination 11110XX for the first seven bits of the first byte following a START(S) or repeated START (Sr) condition. The first seven bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits of the 10-bit address. If the R/W bit is "**0**", the second byte after acknowledge would be the eighth address bit of 10-bits Slave address. Otherwise, the second byte would just be the next transmitted data from a Slave to Master device. The first byte 11110XX is transmitted by using the Slave address register (I2CSA), and the second byte XXXXXXXX is transmitted by using the data buffer (I2CDB).

The possible data transfer formats for 10-bit Slave address mode are explained in the following paragraphs and Figures 6-14a ~ 6-14e.

■ Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address

When the Slave receives the first byte after START bit from Master, each Slave device will compare the first seven bits of the first byte (11110XX) with their own address and check the 8th bit (R//W). If the R//W bit is "**0**", a Slave or more, will return an Acknowledge (A1). Then all Slave devices will continue to compare the second address (XXXXXXXX). If a Slave device finds a match, that particular Slave device will be the only one to return an Acknowledge (A2). The matched Slave device will remain addressed by the Master until it receives the STOP condition or until a repeated START condition followed by the different Slave address is received.

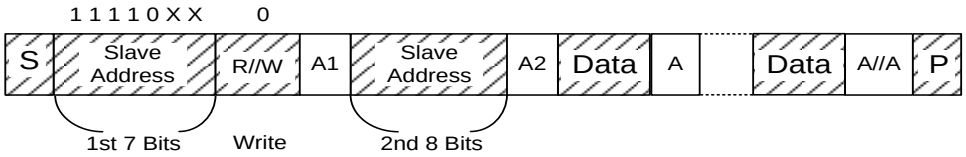


Figure 6-14a Master-Transmitter Transmits to Slave-Receiver with a 10-Bit Slave Address

■ Master-Receiver Read Slave-Transmitter with a 10-bit Slave Address

Up to, and including Acknowledge Bit A2, the procedure is the same as that described above for Master-Transmitter addressing a Slave-Receiver. After the Acknowledge (A2), a repeated START condition (Sr) takes place followed by seven bits Slave address (11110XX), but the 8th bit R//W is "**1**." The addressed Slave device will then return the Acknowledge (A3). If the repeated START (Sr) condition occurs and the seven bits of first byte (11110XX) are received by Slave device, all the Slave devices will compare with their own addresses and check the 8th bit (R//W). However, none of the Slave devices can return an acknowledgement because R//W=1.

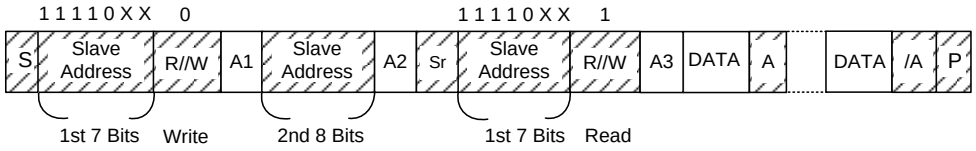


Figure 6-14b Master-Receiver reads Slave-Transmitter with a 10-Bit Slave Address

■ Master Transmits and Receives Data to and from the Same Slave Device with 10-Bit Addresses

The initial operation of this data transfer format is the same as explained in the above paragraph on "*Master-Transmitter transmits to Slave-Receiver with a 10-bit Slave Address.*" Then the Master device starts to transmit the data to the Slave device. When the Slave device receives the Acknowledge or None-Acknowledge that is followed by repeat START (Sr), the above operation under "*Master-Receiver Reads Slave-Transmitter with a 10-Bit Slave Address*" is repeatedly performed.

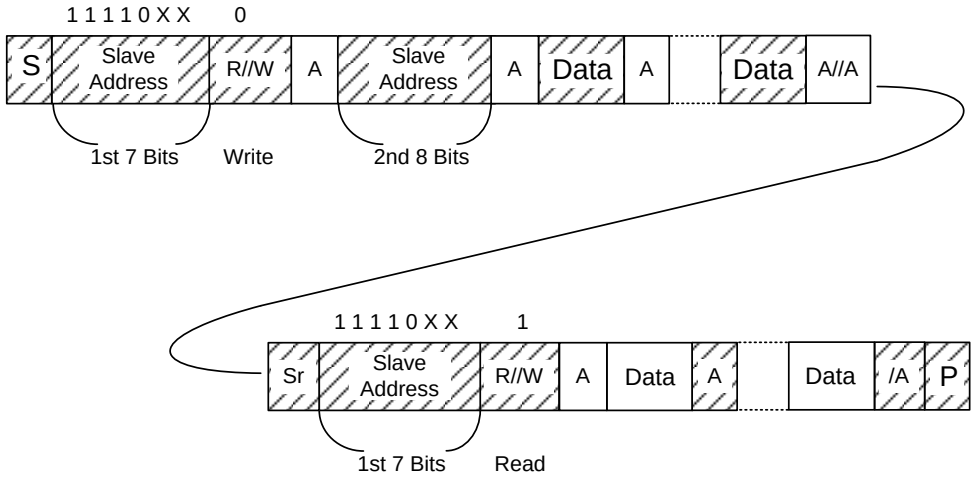


Figure 6-14c Master Addresses a Slave with 10-Bit Addresses Transmits and Receives Data with the Same Slave Device

■ Master Device Transmits Data to Two or More Slave Devices with 10 & 7 Bits Slave Address

For 10-bit address, the initial operation of this data transfer format is the same as the one explained in the above paragraph on "*Master-Transmitter transmits to Slave-Receiver with a 10-bit Slave Address*" describing how to transmit data to Slave device. After the Master device completes the initial transmittal, and wants to continue transmitting data to another device, the Master needs to address each of the new Slave devices by repeating the initial operation mentioned above. If the Master device wants to transmit the data in 7-bit and 10-bit Slave address modes successively, this could be done after the Start or repeat Start conditions as illustrated in the following figures.

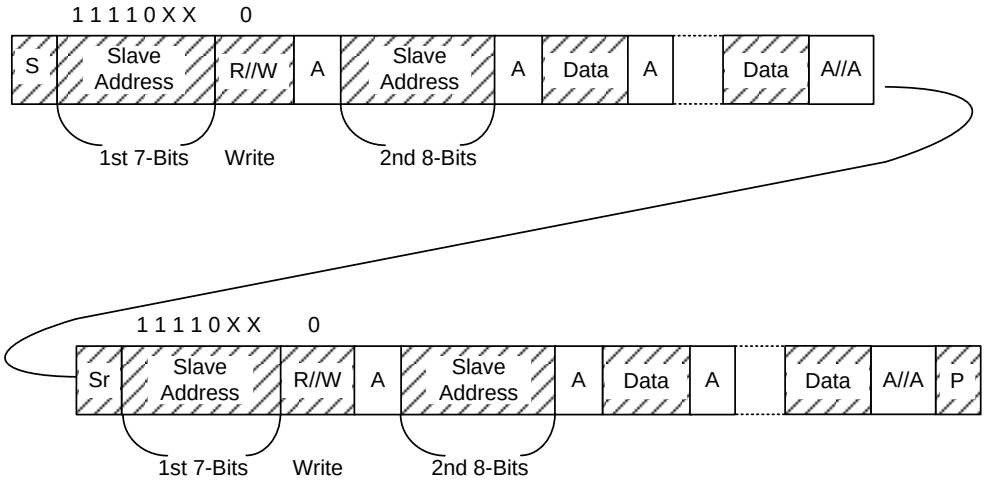


Figure 6-14d Master Transmitting to More than One Slave Devices with 10-Bit Slave Address

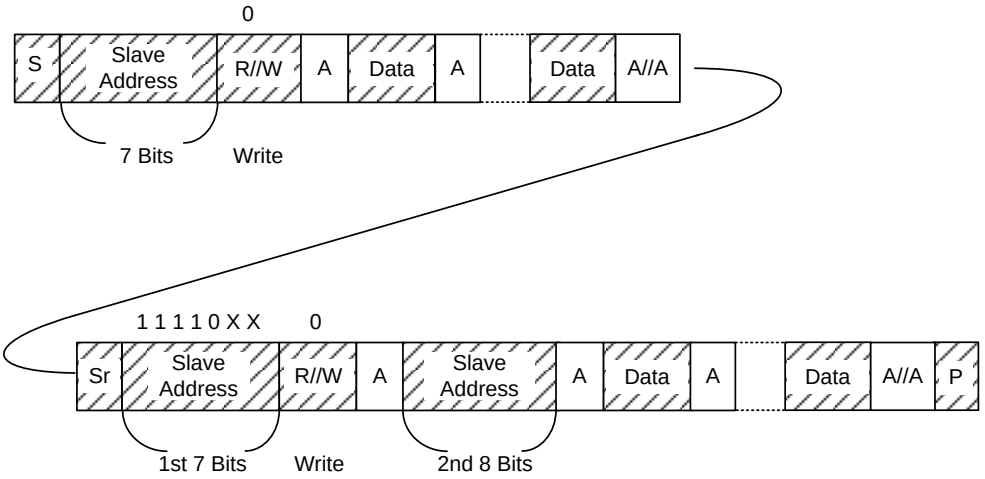


Figure 6-14e Master Successively Transmitting to 7-Bit and 10-Bit Slave Address

6.12.3 Master Mode

In transmitting (receiving) serial data, the I^2C is carried on as follows:

1) Set I2CTS1~0, I2CCS, and ISS bits to select I^2C transmit clock source.
2) Set I2CEN and IMS bits to enable THE I^2C Master function.
3) Write Slave address into the I2CSA register and IRW bit to select read or write.
4) Set strobe bit to start transmitting and then check I2CTSF (I2CTSF) bit.
5) Write 1st data into the I2CDB register, set strobe bit, and check I2CTSF (I2CRSF) bit.
6) Write 2nd data into the I2CDB register, set strobe bit, STOP bit, and check I2CTSF (I2CRSF) bit.

6.13.4 Slave Mode I2C Transmit

In receiving (transmitting) serial data, the I^2C is carried on as follows:

1) Set I2CTS1~0, I2CCS, and ISS bits to select I^2C transmit clock source.
2) Set I2CEN and IMS bits to enable I^2C Slave function.
3) Write device address into the I2CDA register.
4) Check I2CRSF (I2CTSF) bit, read I2CDB register (address), and then clear the Pend bit.
5) Check I2CRSF (I2CTSF) bit, read I2CDB register (1st data), and then clear the Pend bit.
6) Check I2CRSF (I2CTSF) bit, read I2CDB register (2nd data), and then clear the Pend bit.
7) Check the I2CSTPSF bit, end transmission.

6.13 HLVD (High / Low Voltage Detector)

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
Bank 1	0x49	HLVDCR	HLVDEN	IRVSF	VDSB	VDM	HLVDS3	HLVDS2	HLVDS1	HLVDS0
			R/W	R	R	R/W	R/W	R/W	R/W	R/W
Bank 0	0x14	SFR			LVDSF					
					R/W					
Bank 0	0x1B	IMR			LVDIE					
					R/W					
Bank 0	0x10	WUCR			LVDWK					
					R/W					

Under unstable power source condition, such as external power noise interference or EMS test condition, a violent power vibration could occur. At the time, the VDD could become unstable as it could be operating below working voltage. When the system supply voltage (VDD) is below operating voltage, the IC kernel will automatically keep all register status.

The following steps are needed to set up the HLVD function:

1. Set the HLVDEN to “1”, then use Bits 3~0 (HLVDS3~HLVDS0) of Register Bank R to set the HLVD interrupt level
2. Wait for HLVD interrupt to occur
3. Clear the HLVD interrupt flag

The internal HLVD module uses the internal circuit to fit. When user set the HLVDEN to enable the HLVD module, the current consumption will increase to μA.

During sleep mode, the HLVD module continues to operate. If the device voltage drops slowly and crosses the detect point. The LVDSF bit will be set and the device will not wake up from Sleep mode. Until another wake-up source wakes up eKTF5616/08, the HLVD interrupt flag is still set as the prior status.

When the system resets, the HLVD flag will be cleared.

The Figure 6-30 shows the HLVD module to detect the external voltage situation.

When VDD drops above V_{LVD}, LVDSF remain at “0”.

When VDD drops below VDB, LVDSF set to “1”. If global ENI enable, LVDSF will be set to “1”, the next instruction will branch to the interrupt vector. The HLVD interrupt flag is cleared to “0” by software.

Figure 6-30 HLVD Waveform Characteristics Showing Detection Point in an External Voltage Condition

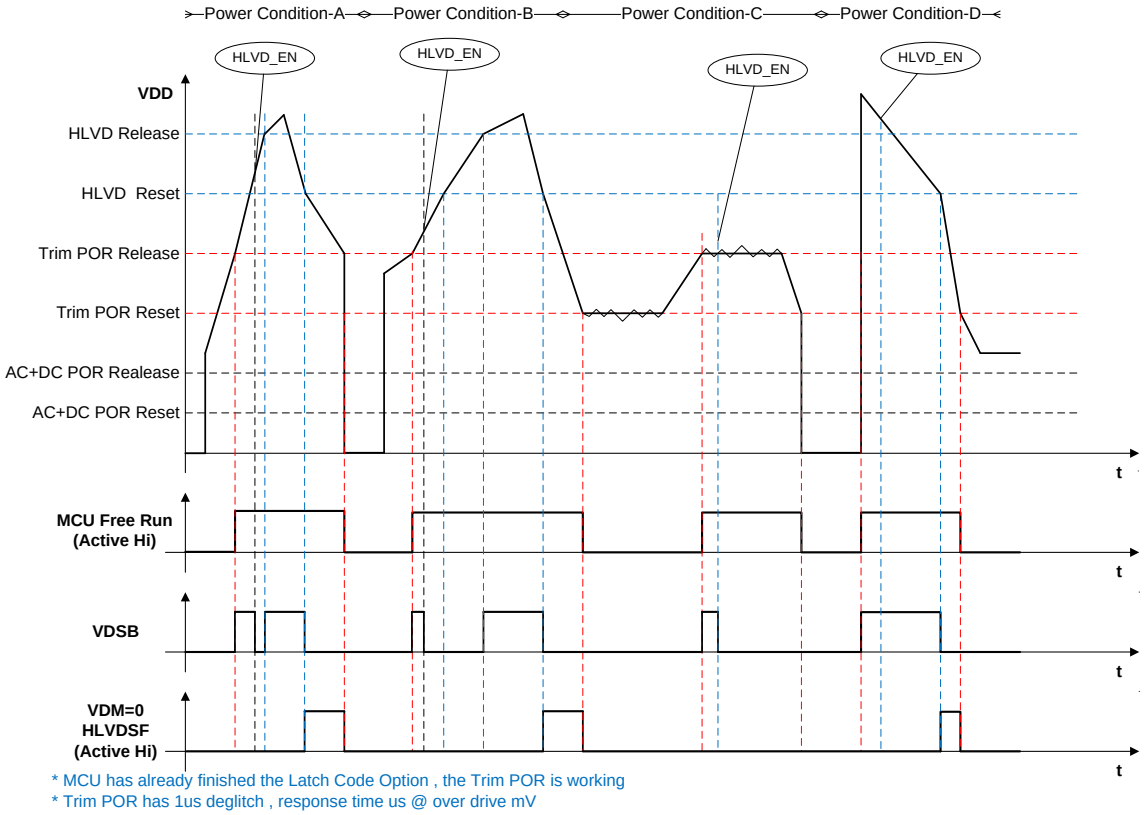


Figure 1.HLVD waveform situation

6.14 Oscillator

6.14.1 Oscillator Modes

The eKTF5616/08 can be operated in the one oscillator mode, i.e., Internal RC oscillator mode (IRC). Users need to set the main-oscillator modes by selecting the OSC0, and set sub-oscillator modes by selecting the FSS in the Code Option register to complete the overall oscillator mode setting.

■ **Main-Oscillator Modes Defined By OSC0**

Main-Oscillator Mode	OSC0
IRC (Internal RC oscillator mode; default) RCOUT (P55) acts as I/O pin	1
IRC (Internal RC oscillator mode) RCOUT (P55) acts as clock output pin	0

■ **Summary of Maximum Operating Speeds**

Conditions	VDD	Fxt Max. (MHz)
Two cycles with two clocks	2.1	8.0
	4	12.0
	5	16.0

6.14.2 Internal RC Oscillator Mode

The eKTF5616/08 offers a versatile internal RC mode with default frequency value of 8 MHz. The Internal RC oscillator mode has other frequencies (16 MHz, and 12 MHz) that can be set by Code Option; RCM1~RCM0. The Table below describes a typical drift rate of the calibration.

■ **Internal RC Drift Rate**

Internal RC Frequency	Touch Key Frequency	Drift Rate				
		Temperature(-40℃ ~+85℃) + Voltage(2V~5.5V)		Process (UWTR:±1% NUWTR: ±0.5%)	Total	
		VDD	Regulator		VDD	Regulator
8MHz	24MHz	±9.5%	±2%	±1%	±10.5%	±3%
12MHz	24MHz	±9.5%	±2%	±1%	±10.5%	±3%
16MHz	16MHz	±9.5%	±2%	±1%	±10.5%	±3%

Note: *These are theoretical values intended for reference only. Actual values may vary depending on actual conditions.*

6.15 Power-On Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply reaches its steady state. The eKTF5616/08 is equipped with a Power-on Voltage Detector (POVD) with a detection level of 1.9V. It will work well if Vdd rises fast enough (50 ms or less). However, in critical applications, extra devices are still required to assist in solving power-up problems.

6.16 External Power-on Reset Circuit

The circuits diagram in Figure 6-15 implements an external RC to generate the reset pulse. The pulse width (time constant) should be kept long enough for VDD to reach minimum operational voltage. Apply this circuit when the power supply has slow rise time. Since the current leakage from the /RESET pin is about ± 5 μA, it is recommended that R should not be greater than 40KΩ in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) functions as a short circuit at the instant of power down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (Rin) will prevent high current or ESD (electrostatic discharge) from flowing into /RESET pin.

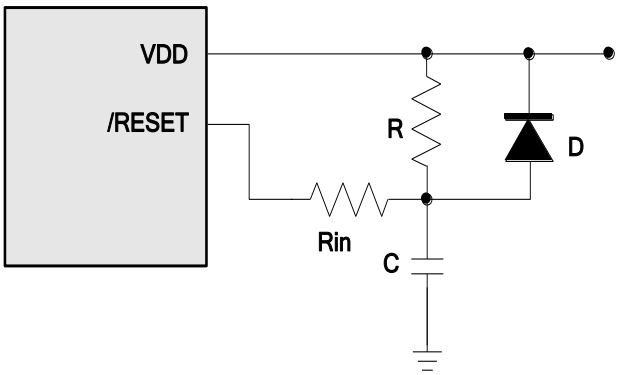


Figure 6-15 External Power-Up Reset Circuit

6.17 Residue-Voltage Protection

When the battery is replaced, device power (VDD) is taken off but residue-voltage remains. The residue-voltage may trip below VDD minimum, but not to zero. This condition may cause a poor power-on reset. Figures 6-16a and 6-16b show how to accomplish a proper residue-voltage protection circuit.

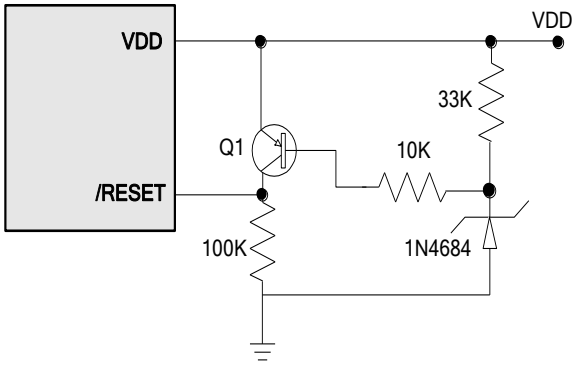


Figure 6-16a Circuit 1 for Residue Voltage Protection

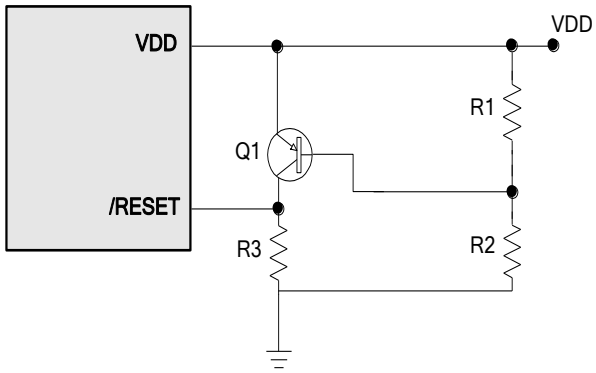


Figure 6-16b Circuit 2 for Residue Voltage Protection

6.18 Code Option

6.18.1 Code Option Register (Word 0)

Word 0								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Mnemonic	-	-	IRCWUT	IODG1	IODG0	HLFS	HLP	LVR1
1	High	High	32 clks	High	High	Green	Low	High
0	Low	Low	8 clks	Low	Low	Normal	High	Low
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	LVR0	RESETEN	ENWDT	NRHL	NRE	EEPR2	EEPR1	EEPR0
1	High	/RST	Enable	8/fc	Disable	High	High	High
0	Low	P50	Disable	32/fc	Enable	Low	Low	Low

Bits 15~14, 11: Not used, set to "0" all the time.

Bit 13 (IRCWUT): IRC Warm Up time (Support IRC Frequency 8MHz)

1: 32 clocks

0: 8 clocks (default)

CPU mode switch	IRC Frequency	POR/LVR	Waiting time before CPU starting to work	
			PERCS = 1	PERCS = 0
Sleep -> Normal Idle -> Normal Green -> Normal	12M, 16M	16ms + WSTO + 32 clocks (main frequency)	32 clocks (main frequency)	WSTO + 32 clocks (main frequency)
	8M	16ms + WSTO + 8/32 clocks (main frequency)	8/32 clocks (main frequency)	WSTO + 8/32 clocks (main frequency)
Sleep -> Green Idle -> Green	32KHz	16ms + WSTO + 8 clocks (sub frequency)	WSTO + 8 clocks (sub frequency)	WSTO + 8 clocks (sub frequency)

Bits 12~11 (IODG1~IODG0): I2C pin deglitch time select bits.

IODG1~0	SPI pin deglitch time	I2C pin deglitch time	UART pin deglitch time	OCD pin deglitch time
00	typical delay=8ns	50ns@5v,Min.(default)	50ns@5v,Min.(default)	20ns@5v,Typical(default)
01	typical delay=15ns	100ns@5v,Min.	200ns@5v,Min.	
10	typical delay=25ns	150ns@5v,Min.	400ns@5v,Min.	
11	no deglitch	no deglitch	no deglitch	no deglitch

Bit 10 (HLFS): Reset to Normal or Green Mode Select Bit

1: CPU is selected as Green mode when a reset occurs.

0: CPU is selected as Normal mode when a reset occurs (default)

Bit 9 (HLP): Power Consumption Selection

1: Low power consumption, apply to working frequency at 8 MHz or below

0: High power consumption, apply to working frequency above 8 MHz

Bits 8~7 (LVR1~LVR0): Low voltage reset enable bit.

LVR1, LVR0	*VDD Reset Level	VDD Release Level
00	NA (Power on reset) (default)	
01	2.5V	2.7V
10	3.6V	3.8V
11	4.2V	4.4V

Note *: If VDD < 2.5V and keep about 5μs, IC will be reset.
If VDD < 3.6V and keep about 5μs, IC will be reset.
If VDD < 4.2V and keep about 5μs, IC will be reset.

Bit 6 (RESETEN): P50//RESET pin selection bit

1: Enable, /RESET pin.

0: Disable, P50 pin (default)

Note *: When P50//RESET is /RESET pin, P50 must set input.

Bit 5 (ENWDT): WDT enable bit

1: Enable

0: Disable (default)

Bit 4 (NRHL): noise rejection high/low pulse defined bit.

1: pulses equal to 8/fc [s] is regarded as signal

0: pulses equal to 32/fc [s] is regarded as signal (default)

Bit 3 (NRE): noise rejection enable bit

1: Disable.

0: Enable (default)

Note *: In Green, Idle, and Sleep modes the noise rejection circuit is always disabled.

Bits 2~0(EEPR2~EEPR0): EEPROM Protect Bit. Each protect status is as follows:

EEPR2	EEPR1	EEPR0	Protect
1	0	1	Disable
Other Value			Enable

6.18.2 Code Option Register (Word 1)

Word 1								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Mnemonic	-	-	FSS					
1	High	High	32K	High	High	High	High	High
0	Low	Low	16K	Low	Low	Low	Low	Low
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	RCM1	RCM0			OSC0	RCOUT
1	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low

Bits 15~14: Not used, set to "0" all the time.

Bits 13 (FSS): Sub-oscillator mode selection bits

1: Fs is 32kHz

0: Fs is 16kHz

Note: *WDT frequency is always 16kHz whatever the FSS bits are set.*

Bits 12~6: Not used, set to "0" all the time.

Bits 5~4 (RCM1~RCM0): IRC frequency selection.

* Corresponding with control register Bank0 RE RCM1~RCM0

RCM1	RCM0	Frequency (MHz)
0	0	NA
0	1	8(default)
1	0	12*
1	1	16

***OCDS simulation 12MHz need select other frequency first, then set Bank0 RE bit1~0(RCM1~RCM0) change to 12MHz**

Bits 3~2: Not used, set to "0" all the time.

Bit 1 (OSC0): Main-oscillator mode selection bits.

Main-Oscillator Mode	OSC0
IRC (Internal RC oscillator mode) (default) RCOUT (P55) acts as I/O pin	0
IRC (Internal RC oscillator mode) RCOUT (P55) acts as clock output pin	1

Bit 0 (RCOUT): System Clock Output Enable Bit in IRC mode

1: OSCO pin is open-drain

0: OSCO output instruction cycle time (default)

6.18.3 Code Option Register (Word 2)

Word 2								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Mnemonic	-	SHEN	SHCLK1	SHCLK0	-	-	-	-
1	High	Disable	High	High	High	High	High	High
0	Low	Enable	Low	Low	Low	Low	Low	Low
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	IRCPSS	-	-	I2COPT	-	-	-	-
1	VDD	High	High	High	High	High	High	High
0	Int. Vref	Low	Low	Low	Low	Low	Low	Low

Bit 15: Not used, set to "0" all the time.

Bit 14 (SHEN): System hold enable bit.

1: Disable

0: Enable

Bits 13~12 (SHCLK1~SHCLK0): System hold clock selection bits (extra 32kHz source)

SHCLK1~0	System Hold Clock
00	4 clocks (default)
01	2 clocks
10	8 clocks
11	16 clocks

Bit 11~8: Not used, set to "0" all the time.

Bit 7 (IRCPSS): IRC Power Source Selection

1: VDD

0: Internal reference (default)

Bit 6: Not used, set to "0" all the time.

Bit 4 (I2COPT): I2C pin optional bit. It is used to switch the pin position of I2C function.

1: Placed I2C pins in P54 (SDA1) and P55 (SCL1).

0: Placed I2C pins in P52 (SDA0) and P53 (SCL0) (default)

*Corresponding with control register Bank 0 R31 I2COPT

Bits 3~0: Not used, set to "1" all the time.

6.18.4 Code Option Register (Word 3)

Word 3								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Mnemonic	-	EFTIM	-	-	-	-	-	-
1	High	Heavy	High	High	High	High	High	High
0	Low	Light	Low	Low	Low	Low	Low	Low
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	TBWEN	ID5	ID4	ID3	ID2	ID1	ID0
1	High	Enable	Customer ID					
0	Low	Disable						

Bits 15: Not used, set to "0" all the time

Bit 14 (EFTIM): Low Pass Filter

1: Pass ~ 10MHz (heavy LPS)

0: Pass ~ 25MHz (light LPS) (default)

Bits 13~7: Not used, set to "0" all the time

Bit 6 (TBWEN): Table write enable bit.

1: Enable.

0: Disable. (default)

Bits 5~0 (ID5~ID0): Customer's ID Code

6.19 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2, A", "ADD R2, A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A", "BS(C) R2, 6", "CLR R2", etc·). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

- "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Moreover, the instruction set has the following features:

1) Every bit of any register can be directly set, cleared, or tested.
2) The I/O register can be considered as general register. That is; the same instruction can operate on I/O register.

■ Instruction Set Table:

In the following Instruction Set table, the following symbols are used:

"**R**" *represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.*

"**b**" *represents a bit field designator that selects the value for the bit which is located in the register "**R**", and affects operation.*

"**k**" *represents an 8 or 10-bit constant or literal value.*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
SLEP	0 → WDT, Stop oscillator	T,P
WDTC	0 → WDT	T,P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
RESET	Software Device Reset	ALL Registers = Reset Value Flags* = Reset Value
TBWR	Table Writer Start instruction	None
INT k	PC+1 → [SP], k*2 → PC	None
BTG R,b	Bit Toggle R ; /(R<b>)->R<b> *Range R5~RA	None
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z,C,DC,OV,N
SUB R,A	R-A → R	Z,C,DC,OV,N
DECA R	R-1 → A	Z,C,DC,OV,N
DEC R	R-1 → R	Z,C,DC,OV,N
OR A,R	A ∨ R → A	Z,N
OR R,A	A ∨ R → R	Z,N
AND A,R	A & R → A	Z,N
AND R,A	A & R → R	Z,N
XOR A,R	A ⊕ R → A	Z,N
XOR R,A	A ⊕ R → R	Z,N
ADD A,R	A + R → A	Z,C,DC,OV,N
ADD R,A	A + R → R	Z,C,DC,OV,N

Mnemonic	Operation	Status Affected
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z,N
COM R	/R → R	Z,N
INCA R	R+1 → A	Z,C,DC,OV,N
INC R	R+1 → R	Z,C,DC,OV,N
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C, N
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C, N
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C, N
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C,N
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None <Note2>
BS R,b	1 → R(b)	None <Note3>
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
JE R	Compare R with ACC, Skip =	None
JGE R	Compare R with ACC, Skip >	None
JLE R	Compare R with ACC Skip <	None
OR A,k	A ∨ k → A	Z,N
JE k	Compare K with ACC, Skip =	None
TBRDA R	ROM[(TABPTR)] → R, A A ← program code (low byte) ; R ← program code (high byte)	None
AND A,k	A & k → A	Z,N

Mnemonic	Operation	Status Affected
SJC k	Short jump to K if Carry if C=1 PC+1+offset → PC *offset = -128≦k≦127	None
SJNC k	Short jump to K if Not Carry if C=0 PC+1+offset → PC *offset = -128≦k≦127	None
SJZ k	Short jump to K if Zero if Z=1 PC+1+offset → PC *offset = -128≦k≦127	None
XOR A,k	A ⊕ k → A	Z,N
SJNZ k	Short jump to K if Not Zero if Z=0 PC+1+offset → PC *offset = -128≦k≦127	None
RRA R	R(n) → A(n-1), R(0) → A(7)	N
RR R	R(n) → R(n-1), R(0) → R(7)	N
RETL k	k → A, [Top of Stack] → PC	None
XCH R	R ⟷ A	None
RLA R	R(n) → A(n+1), R(7) → A(0)	N
RL R	R(n) → R(n+1), R(7) → R(0)	N
SUB A,k	k-A → A	Z,C,DC,OV,N
SUBB A,R	R-A-/C → A	Z, C, DC, OV, N
SUBB R,A	R-A-/C → R	Z, C, DC, OV, N
SBANK k	K→R1(4)	None
GBANK k	K→R1(3:0)	None
LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→[SP], k→PC	None
LJMP k	Next instruction : k kkkk kkkk kkkk K→PC	None
TBRD R	ROM[(TABPTR)] → R	None
ADD A,k	k+A → A	Z,C,DC,OV,N
NEG R	2's complement, /R +1 → R	Z,C,DC,OV,N
ADC A,R	A+R+C → A	Z,C,DC,OV,N
ADC R,A	A+R+C → R	Z,C,DC,OV,N

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	VDD+0.3V
Output voltage	Vss-0.3V	to	VDD+0.3V
Working Voltage	2.1V	to	5.5V
Working Frequency	DC	to	16 MHz

8 DC Electrical Characteristics

(Ta=25 °C, VDD=5.0V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	IRC: VDD to 5 V	8 MHz, 12 MHz, 16 MHz		F		Hz
IRCE	Internal RC oscillator error per stage			±1		%
IRC1	IRC:VDD to 5V	RCM1~RCM0=01		8		MHz
IRC2	IRC:VDD to 5V	RCM1~RCM0=10		12		MHz
IRC3	IRC:VDD to 5V	RCM1~RCM0=11		16		MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	0.7 VDD		VDD +0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	-0.3V		0.3 VDD	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7 VDD		VDD +0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V		0.3 VDD	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC,INT	0.7 VDD		VDD +0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC,INT	-0.3V		0.3 VDD	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD-0.1VDD		-3.4		mA
IOH2	Output High Voltage (high drvie) (Ports 5, 6, 7, 8)	VOH = VDD-0.1VDD		-11		mA
IOH3	Output High Voltage (high drvie) (Ports 5, 6, 7, 8)	VOH = VDD-0.3VDD		-30		mA
IOL1	Output Low Voltage (Ports 5, 6, 7, 8)	VOL = GND+0.1VDD		18		mA
IOL2	Output Low Voltage (high sink) (Ports 5, 6, 7, 8)	VOL = GND+0.1VDD		34		mA
IOL3	Output Low Voltage (high sink) (Ports 5, 6, 7, 8)	VOL = GND+0.3VDD		80		mA
IPH	Pull-high current	Pull-high active, input pin at VSS		-43		μA
IPL	Pull-low current	Pull-low active, input pin at IO_VDD		14		μA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LVR1	Low voltage reset level	TA = -40~85℃	2.2	2.5	2.8	V
LVR2	Low voltage reset level	TA = -40~85℃	3.3	3.6	3.9	V
LVR3	Low voltage reset level	TA = -40~85℃	3.9	4.2	4.5	V
ISB1	Power down current (Sleep mode)	/RESET= 'High', Fm & Fs off All input and I/O pins at VDD, output pin floating, WDT disabled		1		μA
ISB2	Power down current (Sleep mode)	/RESET= 'High', Fm & Fs off All input and I/O pins at VDD, output pin floating, WDT enabled		5		μA
ISB3	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=32K/16KHz (IRC type) output pin floating, WDT disabled,		6		μA
ISB4	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=32K/16KHz (IRC type), output pin floating, WDT enabled		6		μA
ICC1	Operating supply current (Green mode, CPU only)	/RESET= 'High', Fm off, Fs=32K/16KHz (IRC type), output pin floating, WDT disabled		15		μA
ICC2	Operating supply current (Green mode, CPU only)	/RESET= 'High', Fm off, Fs=32K/16KHz (IRC type), output pin floating, WDT enabled		15		μA

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25°C. These data are for design reference only and have not been tested or verified.*

9 AC Electrical Characteristics

■ **(eKTF5616/08 Ta=-40° ~ 85°C, VDD=5.5V, VSS=0V)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time	RC type	500	-	DC	ns
Ttcc	TCC input period	-	(Tins+20)/N*	-	-	ns
Tdrh	Device reset hold time	-	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	-	-	ns
Twdt	Watchdog timer period	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	-	-	0		ns
Thold	Input pin hold time	-	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns

* ***N:*** *Selected prescaler ratio*

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25℃. These data are for design reference only and have not been tested or verified.*

Data EEPROM Characteristics (VDD=2.1V to 5.5V, VSS=0V, Ta = -40 to 85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.1V~ 5.5V Temperature = -40°C ~ 85°C	-	2	3	ms
Treten	Data Retention		-	10	-	Years
Tendu	Endurance time		-	100K	-	Cycles

Program Flash Memory Electrical Characteristics (VDD=2.1V to 5.5V, VSS=0V, Ta = -40 to 85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.1V~ 5.5V Temperature = -40°C ~ 85°C	-	1	1.5	ms
Treten	Data Retention		-	10	-	Years
Tendu	Endurance time		-	100K	-	Cycles

AD Characteristics (Vdd = 5.0V, Vss=0V, Ta=25°C)

Parameter	Symbol	Test Conditions	Type			Unit	Remark
			Min.	Typ.	Max.		
Operating Range	Vdd	For 5.5v Fs=100KHz, Fin=1KHz, For 2.5V Fs=25KHz, Fin=1KHz	2.5		5.5	V	
	V_{REFT}		2.5		Vdd	V	Top reference voltage
	V_{REFB}		Vss	-	V_{REFT}-ΔV_{REF}	V	Bottom reference voltage
	ΔV_{REF}		2.5			V	Reference Voltage Range
1/2 *VDD AD Input	$V_{1/2VDD}$	Vdd=5V	2.475	2.5V	2.525	V	1/2*VDD AD channel Input Voltage
	$T_{1/2VDD}$	Vdd=5V		2.8	4	uS	1/2*VDD Warn up time for ADC sample
	$I_{1/2VDD}$	Vdd=5V		35	42	uA	1/2*VDD Current Consumption
Current Consumption	Ivdd	V_{REFT}= Vdd=5.5V, SVREFT="00", Fs=100kHz, Fin=1kHz			1.4	mA	The ADC top reference voltage is internal Vdd
	Iref				10	uA	
Current Consumption	Ivdd	V_{REFT}= Vdd=5.5V, SVREFT="01"or"10", Fs=100kHz, Fin=1kHz			0.9	mA	The ADC top reference voltage is external VREF
	Iref				0.5	mA	
Standby Current	Isb				0.1	uA	Including voltage reference
ZAI	ZAI				10k	ohm	The external impedance of analog input channel.
SNR	SNR	V_{REFT}= Vdd=5.0V, Fs=100KHz, Fin=1kHz	70			dBc	Signal-To-Noise Ratio
THD	THD	V_{REFT}= Vdd=5.0V, Fs=100KHz, Fin=1KHz			-70	dBc	Total Harmonic Distortion
SNDR	SNDR	V_{REFT}= Vdd=5.0V, Fs=100KHz, Fin=1kHz	68			dBc	Signal-to-Noise & Distortion Ratio

Parameter	Symbol	Test Conditions	Type			Unit	Remark
			Min.	Typ.	Max.		
Worst Harmonic	WH	V_{REFT}= Vdd=5.0V, Fs=100KHz, Fin=1kHz			-73	dBc	
SFDR	SFDR	V_{REFT}= Vdd=5.0v, Fs=100KHz, Fin=1kHz	73			dBc	Spurious Free Dynamic Range
Offset Error	OE	V_{REFT}= Vdd=5.0v, Fs=100K Hz			+/-4	LSB	
Gain Error	GE	V_{REFT}= Vdd=5.0v, Fs=100kHz			+/-8	LSB	
DNL	DNL	V_{REFT}= Vdd=5.0v, Fs=100K Hz, Fin=1kHz			+/-1	LSB	Differential Nonlinearity
INL	INL	V_{REFT}= Vdd=5.0v, Fs=100K Hz, Fin=1kHz			+/-4	LSB	Integral Nonlinearity
Conversion Rate	Fs1	Vdd=3.0~5.5V, Fin=1kHz			100	K SPS	Including sampling & conversion phase
	Fs2	Vdd=2.5~3.0v, Fin=1kHz			25	K SPS	
Power Supply Rejection Ratio	PSRR	V_{REFT}=2.5v, SVREF="01"or"10", Vdd=2.5V ~ 5.5V, Fs=25K Hz, Vin=0v ~ 2.5v			2	LSB	The change in DC output code from the value with the supply at the Min. limit to the value with the supply at its Max. limit.

HLVD :

	Parameter	Condition	Min.	Typ.	Max.	unit
ILVD	LVD Operation current	LVD Enable,VDD=5V		17	20	μA
Temp.		Combine with VREF	-40	25	85	℃
ΔV1	VH,VL tolerance	VDD = 2.1v~4V		+/- 0.15		V
ΔV2	VH,VL tolerance	VDD = 4v~5.5V		+/- 0.2		V
VHYST	Hysteresis Voltage		50	100	150	mV
	VREF stable time	LVD Enable,VDD=5V		60	80	us
IPD	LVD power-down current	LVD disable,VDD=5V		52	62	nA

Vref(Vdd = 5.0V, Ta=25°C):

symbol	parameter	condition	Min.	Typ.	Max.	Unit	IC Verify	Teststation Verify
Vdd	power supply		2.7		5.5	V	Yes	Yes
Ivdd	DC supply current	Vref=4V, No load		220	270	uA	Yes	Yes
Ipd	Power down current				<0.1	uA	Yes	Yes
Tresponse	Response time	Trim bit and VREF select setting time		10	20	us	Yes	Yes
warn up time	time ready for voltage reference			15	50	us	Yes	Yes
Vref	Voltage reference output		2.028	2.048	2.068	V	Yes	Yes
			2.534	2.560	2.586			
			3.041	3.072	3.103			
			4.055	4.096	4.137			
Vref	Voltage reference output	Temp=-40℃~85℃	Typ.-3%	2.048	Typ.+3%	V	Yes	Yes
			Typ.-3%	2.560	Typ.+3%			
			Typ.-3%	3.072	Typ.+3%			
			Typ.-3%	4.096	Typ.+3%			
Vdd_min	Minimum power supply		Vref+0.1	Vref+0.2*		V	Yes	Yes
Vref_sensor	Vref for Sensor			GND		V	Yes	Yes
			0.1014	0.1024	0.1034			
			0.2028	0.2048	0.2068			
			0.4055	0.4096	0.4137			

APPENDIX

A Package Type

MCU	Package Type	Pin Count	Package Size
eKTF5616SOP28	SOP	28 pins	300 mil
eKTF5616QN24	QFN	24 pins	4x4x0.8 mm
eKTF5616SOP20	SOP	20 pins	300 mil
eKTF5608SOP16A	SOP	16 pins	150 mil
eKTF5616SSOP20A	SSOP	20 pins	150 mil
eKTF5616AQN24	QFN	24 pins	4x4x0.8 mm

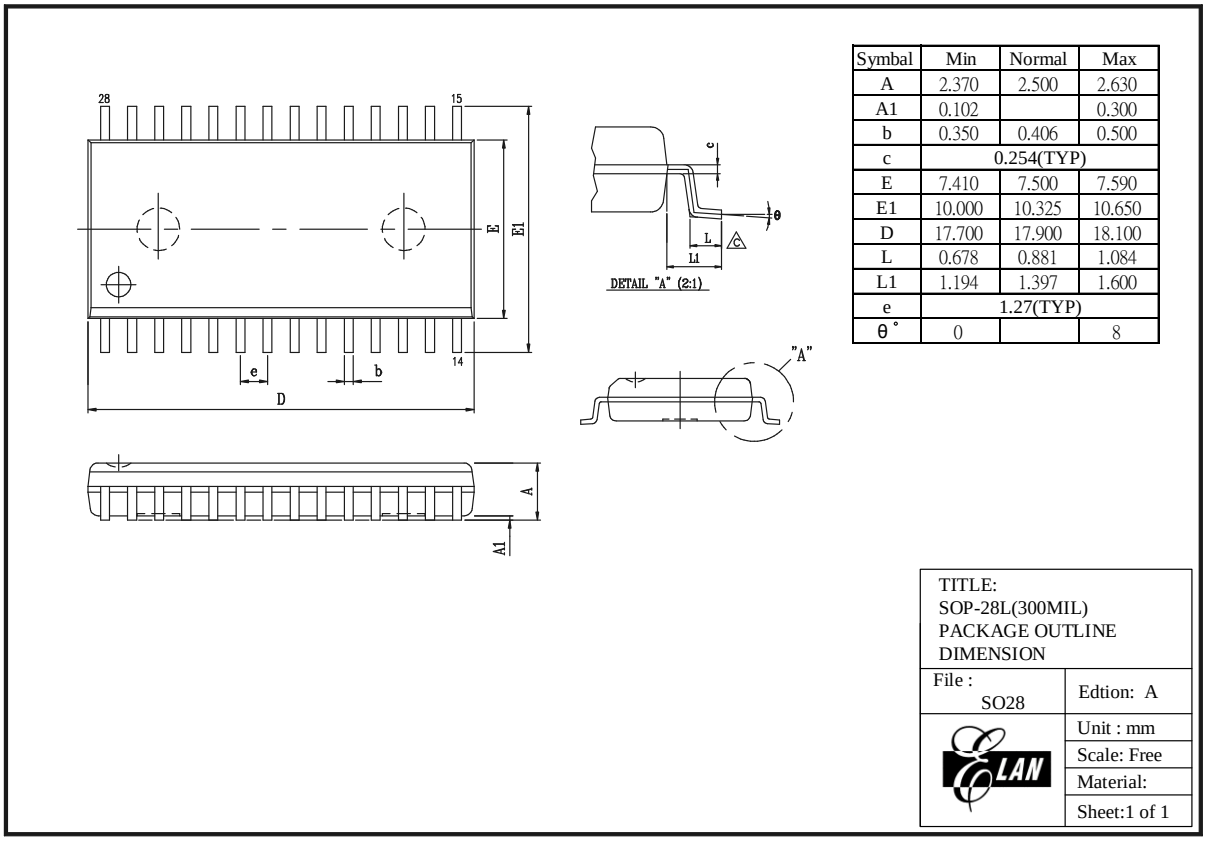
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

The Pb contents are less 100ppm and comply with Sony specifications.

Part No.	eKTF5616/08 S/J
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point(°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Package Information

B.1 eKTF5616SOP28

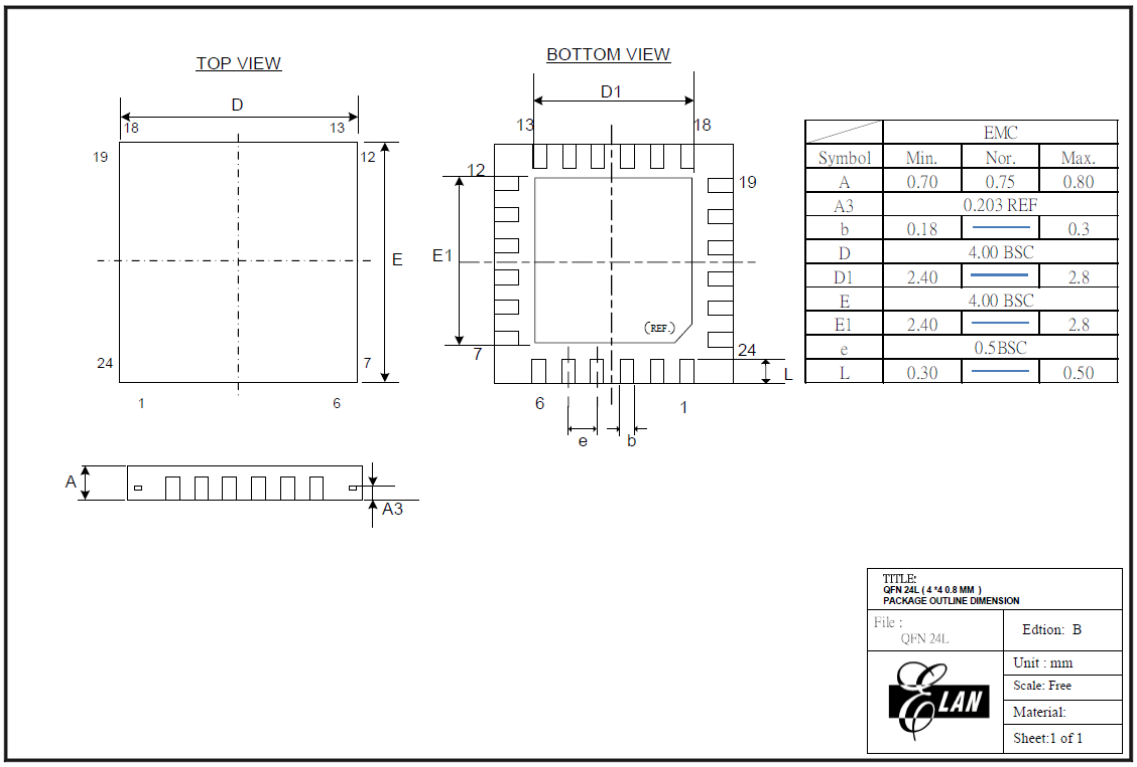


Symbal	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c	0.254(TYP)		
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e	1.27(TYP)		
θ °	0		8

TITLE: SOP-28L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 eKTF5616 28-pin SOP Package Type

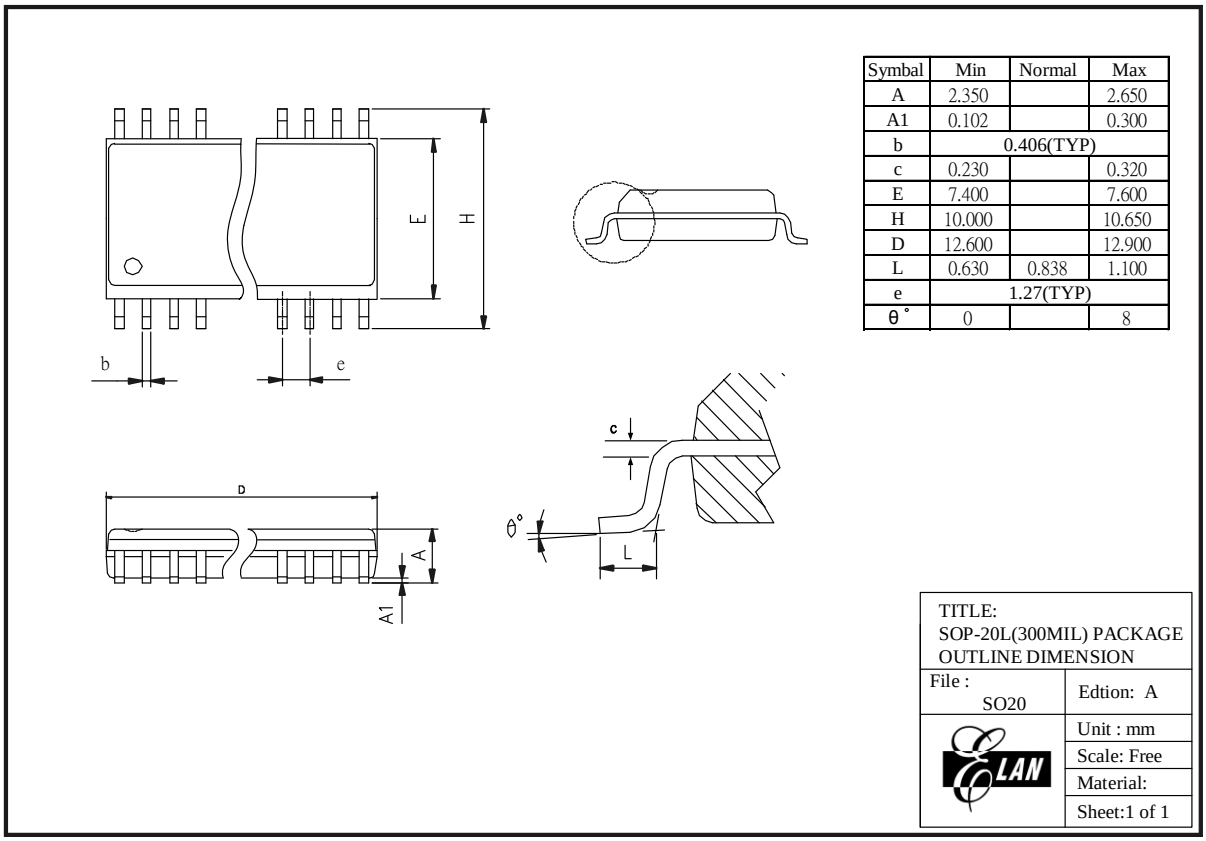
B.2 eKTF5616QN24



Symbol	EMC		
	Min.	Nor.	Max.
A	0.70	0.75	0.80
A3		0.203 REF	
b	0.18		0.3
D		4.00 BSC	
D1	2.40		2.8
E		4.00 BSC	
E1	2.40		2.8
e		0.5 BSC	
L	0.30		0.50

Figure B-2 eKTF5616 24-pin QFN Package Type

B.3 eKTF5616SOP20

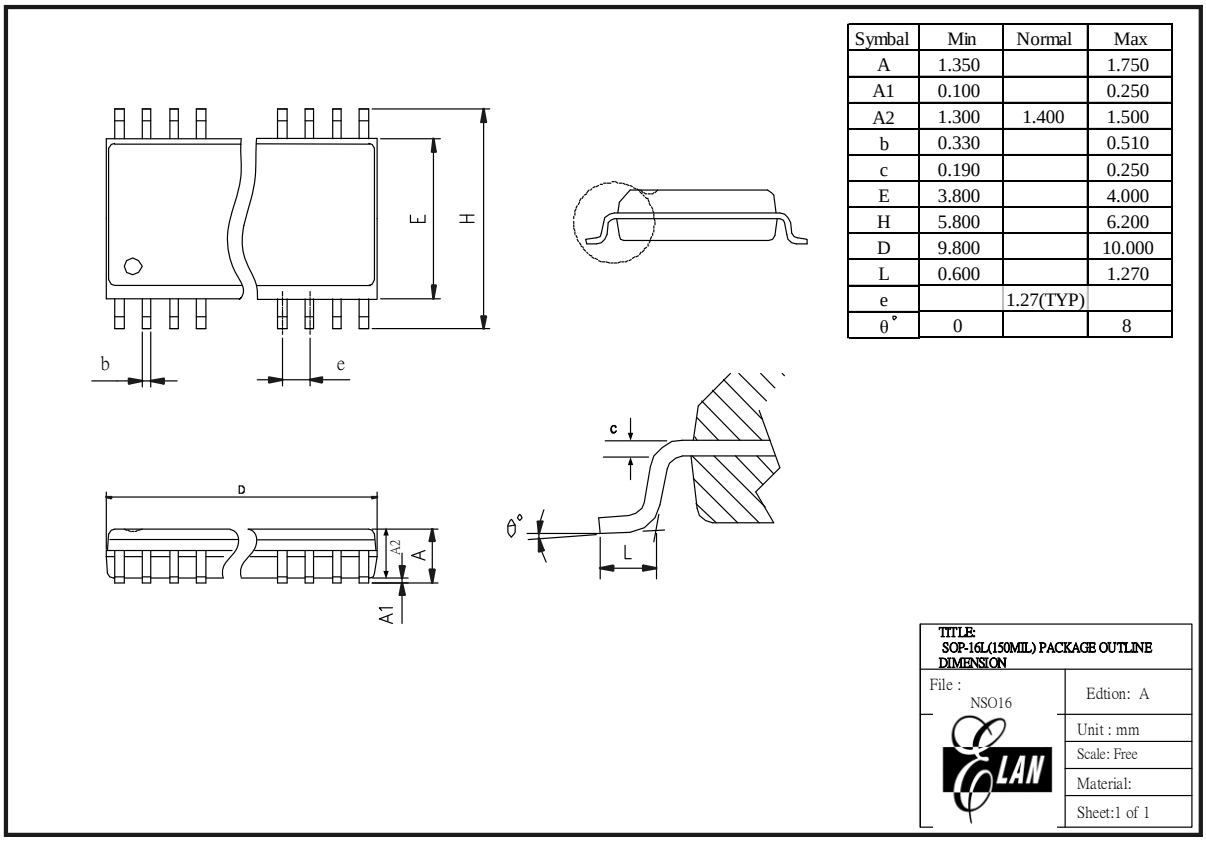


Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-3 eKTF5616 20-pin SOP Package Type

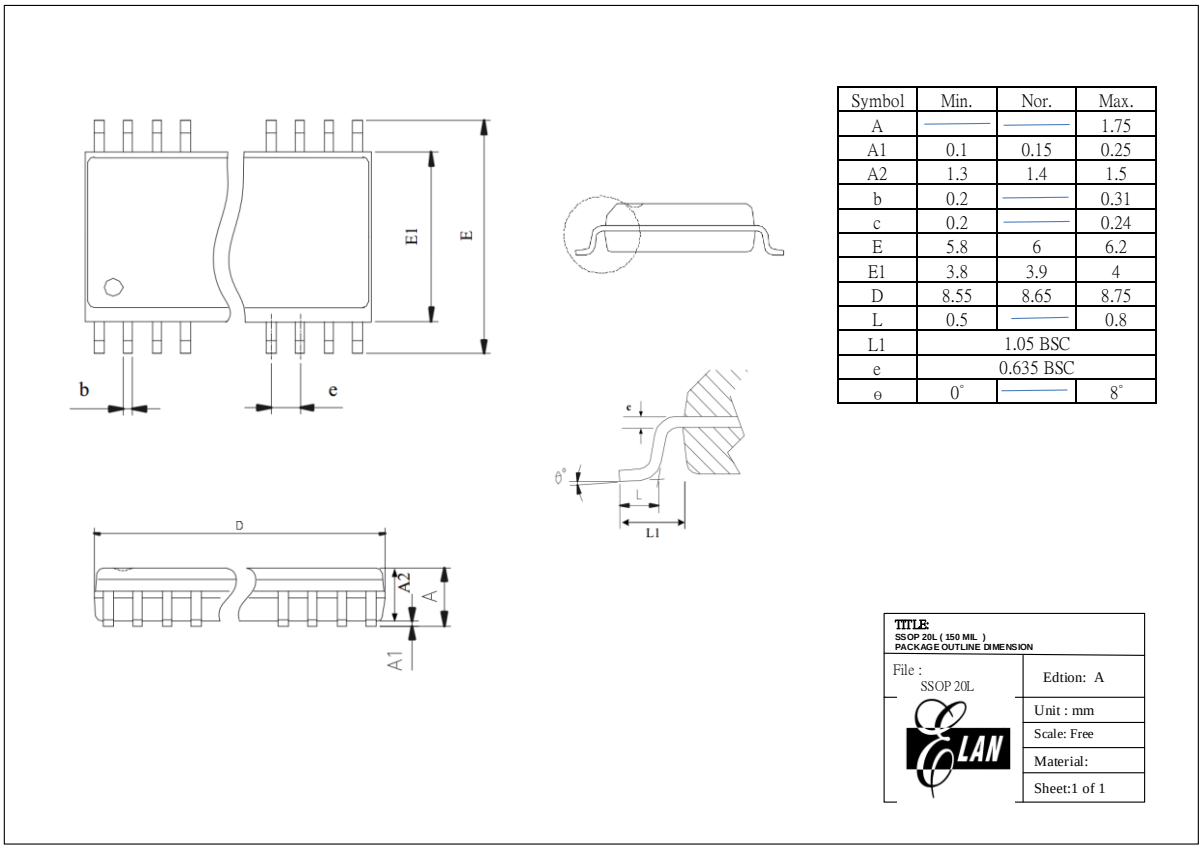
B.4 eKTF5608SOP16A



Symbal	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
A2	1.300	1.400	1.500
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	9.800		10.000
L	0.600		1.270
e		1.27(TYP)	
θ°	0		8

Figure B-4 eKTF5608 16-pin SOP Package Type

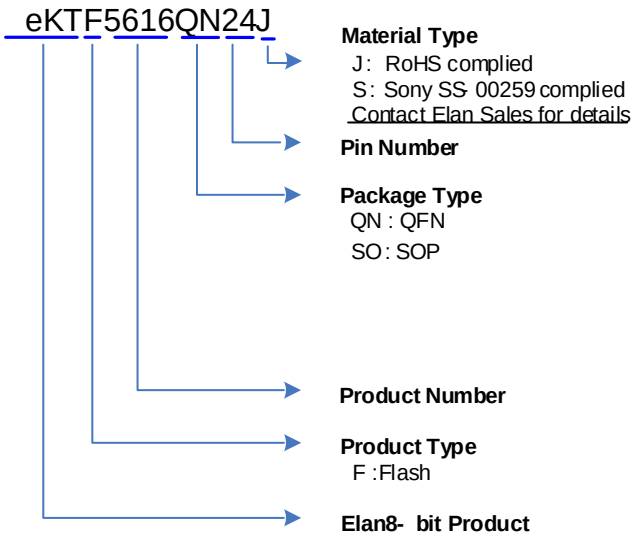
B.5 eKTF5616SSOP20A



Symbol	Min.	Nor.	Max.
A			1.75
A1	0.1	0.15	0.25
A2	1.3	1.4	1.5
b	0.2		0.31
c	0.2		0.24
E	5.8	6	6.2
E1	3.8	3.9	4
D	8.55	8.65	8.75
L	0.5		0.8
L1	1.05 BSC		
e	0.635 BSC		
θ	0°		8°

Figure B-5 eKTF5616 20-pin SSOP Package Type

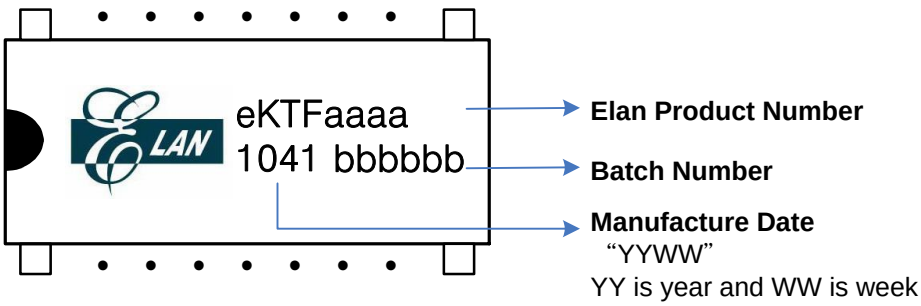
C Ordering and Manufacturing Information



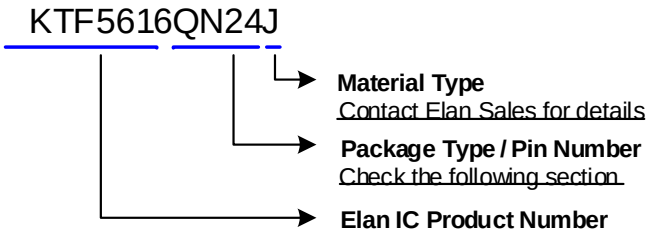
For example

eKTF5616QN24J

is eKTF5616 with Flash program memory , in 24 - pin QFN package



Ordering Code



D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225 ± 5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240 ± 5°C)	
Temperature cycle test	-65°C (15mins)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C, RH=85%，TD (endurance) = 168, 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥｜± 8KV｜	–

D.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.